intel

## INTELLEC® DOUBLE DENSITY DISKETTE OPERATING SYSTEM HARDWARE REFERENCE MANUAL

Alteriated conless of this manual or other land literative way be admonded from

Uthouses (high mess) (act Carporties) 208; Boress Armig Suda Char, CA 93941

- A line constant a second of restaurant book and a second s

bited Composition ended as reasonite of any bink trick paped to 125° orientics, as being, but and the to the inglifed contraction of manifestability and filmers for a minimum pagement well of spectrulon accursos to mappelificity for any errors that may represente this defice on their C up or the statement water to the term to collising our to base errors the term station constraints or the defice on the constraints of the second second

tadel Carpetrikov prestan ve vapetie bilizy (er ets ver er er er er er er er en er en er en er er er er er er e

ingel additions products not a particless by and stadi sectors the property of basis's approximation in the fraper addition are distribution in which is to presidential and its locally sufference fractions for a staffner to the restance in the sec

Not part of this department and the exercise or experienced in any form of 19 any mains with the Pol Sol evolution contend of Basil Comparations

First following are tradematics of brack Corporations and its officiality and stars he available to the environment

Order Number: 9800422-01

Copyright © 1977 Intel Corporation Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

Additional copies of this manual or other Intel literature may be obtained from:

Literature Department Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051

The information in this document is subject to change without notice.

Intel

Int\_

Intelevision Intellec

Intellink

iOSP iPDS

iRMX

Intel Corporation makes no warranty of any kind with regard to this material, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. Intel Corporation assumes no responsibility for any errors that may appear in this document. Intel Corporation makes no commitment to update nor to keep current the information contained in this document.

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied.

Intel software products are copyrighted by and shall remain the property of Intel Corporation. Use, duplication or disclosure is subject to restrictions stated in Intel's software license, or as defined in ASPR 7-104.9(a)(9).

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of Intel Corporation.

The following are trademarks of Intel Corporation and its affiliates and may be used to identify Intel products:

> BXP CREDIT ICE i<sub>m</sub> iMMX Insite

iCS

iSBC iSBX iSXM Library Manager MCS Megachassis Micromainframe Micromap

Multibus Multichannel Multimodule Plug-A-Bubble PROMPT RMX/80 System 2000 UPI

## PREFACE

This reference manual is the primary source of information for the hardware within the INTELLEC Double Density Diskette Operating System. It explains how the Diskette System is installed, how it communicates with the INTELLEC Microcomputer Development System, and how it functions internally.

Refer to the ISIS-II System User's Guide (order number 98-306) for complete instructions on how to operate the Diskette System. For information on the host system, refer to the INTELLEC Microcomputer Development System Hardware Reference Manual and to the INTELLEC Microcomputer Development System Operator's Manual.

## TABLE OF CONTENTS

Cha	pter	Title	Page
1	INTE	RODUCTION	1-1
	1.1	SYSTEM OVERVIEW	1-1
	1.2	RECORDING FORMAT	1-4
2	OPER	RATIONAL SUMMARY AND	
	PF	ROGRAMMING CONSIDERATIONS	2-1
	2.1	CHANNEL COMMANDS	2-2
	2.2	DISKETTE OPERATIONS	2-5
	2.3	I/O PARAMETER BLOCK	2-8
4	2.4	ERROR INDICATIONS	2-11
3	THE	CHANNEL BOARD	3-1
	3.1	FUNCTIONAL ORGANIZATION OF	
	3.2	THE CHANNEL BOARD THEORY OF OPERATION:	3-1
		CHANNEL BOARD	3-3
		3.2.1 CHANNEL COMMAND BLOCK . 3.2.2 MICBO CONTROL UNIT (MCU)	3-3
		BLOCK	3-5
		BLOCK	3-8
		3.2.4 CENTRAL PROCESSING ELEMEN	т
		(CPE) BLOCK	3-12
		BLOCK	3.15
			2 16
	3.3	SCHEMATICS/PIN LISTS: CHANNEL	3-10
		BOARD	3-17
4	THE	INTERFACE BOARD	4-1
	4.1	FUNCTIONAL ORGANIZATION OF	
	42	THE INTERFACE BOARD	4-1
	4.2	BOARD	4.3
		4.2.1 DISK DRIVE CONTROL	4.3
		4.2.2 WRITE DATA GENERATOR	4-5
		4.2.3 SERIAL DATA/CLOCK	4-0
		SYNCHRONIZATION 4.2.4 CYCLIC REDUNDANCY CHECK	4-10
		(CBC)	4-10
		4.2.5 BUS CONTROL	4-13
	4.3	SCHEMATICS/PIN LISTS:	2 00m
		INTERFACE BOARD	4-15

Cha	pter	Title	Page
5	THE	DISKETTE DRIVES	5-1
	5.1	FUNCTIONAL DESCRIPTION	5-1
	5.2	PERFORMANCE CHARACTERISTICS	5-2
		5.2.1 RECORDING CHARAC-	
		TERISTICS	5-2
		5.2.2 BIT TRANSFER RATE '	5-2
		5.2.3 DATA CAPACITY	5-2
		5.2.4 LATENCY TIME	5-3
		5.2.5 POSITIONING CHARAC-	
		TERISTICS	5-3
		5.2.6 FDD START AND STOP	F 0
			5-3
		5.2.7 ERROR RECOVERY	5-3
		5.2.0 ENVIRONMENTAL LIMITS · · ·	5-4
	5.2	5.2.9 WRITE PROTECT	5-4
	5.5		0-4
	5.4	AND HANDLING	5-9
	5.5	DISKETTE CARTRIDGE WRITE	00
		PROTECT NOTCH	5-11
	5.6	ADDITIONAL INFORMATION	5-11
6	DISK	ETTE SYSTEM MICROPROGRAM	6-1
	6.1	INTRODUCTION	6-1
	6.2	MICROPROGRAM MODULE	
		DESCRIPTION	6-1
7	UTI	IZATION	7-1
	7.1	ENVIRONMENTAL EXTREMES	7-1
	7.2	MOUNTING RECOMMENDATIONS	7-1
	7.3	ELECTRICAL CONNECTIONS	7-1
	7.4	BASE ADDRESS SELECTION	7-2
	7.5	INTERRUPT LEVEL SELECTION	7-2
8	OPE	RATING CHARACTERISTICS	8-1
	8.1	AC CHARACTERISTICS	8-1
	8.2	DC CHARACTERISTICS	8-9

## LIST OF ILLUSTRATIONS

Chapter	24	Title	Page
1	INTE	RODUCTION	1-1
	1-1	DISKETTE SYSTEM BLOCK DIAGRAM	1-2
	1-2	PHYSICAL DATA FORMAT	1-6
	1-3	BYTE REPRESENTATION	1-7
	1-4	DATA BYTES	1-7
	1-5	DATA BIT	1-8
	1-6	BIT CELL	1-8
	1.7	TRACK FORMAT	1.9
	1.8	INDEX ADDRESS MARK	1-10
	1.0	ID ADDRESS MARK	1.10
	1 10	DATA ADDRESS MARK	1.11
	1 1 1	DATA ADDRESS MARK	1 1 1
	1-11	DELETED DATA ADDRESS MARK	1-11
2	OPE	RATIONAL SUMMARY AND PROGRAMMING CONSIDERATIONS	2-1
	2-1	SECTOR FORMAT	2-7
	2.2	'DATA' ADDRESS MARK	2-7
	2.3	DELETED DATA' ADDRESS MARK	2.7
	2.4	I/O PARAMETER BLOCK (IOPB) FORMAT	2.9
	2-4	TANAMETER BEOCK (IOFB) FORMAT	2-0
3	СНА	NNEL BOARD	3-1
	2.1	CHANNEL POARD, EUNCTIONAL BLOCK DIACRAM	2.2
	2.2	2001 MICRORPOGRAM CONTROL LINUTY EUNCTIONAL PLOCK	3-2
	3-2	DIACRAM	26
	2.0		3-0
	3-3	3002 CENTRAL PROCESSING ELEMENT: FUNCTIONAL BLOCK	2.14
	~ .		3-14
	3-4	SCHEMATIC DRAWING: CHANNEL BOARD	3-21
4	INTE	ERFACE BOARD	4-1
	1-6	ADITEINE CHARACTERISTICS AND ADDITEINE TO ARREST ADITERS	10. 7
	4-1	INTERFACE BOARD: FUNCTIONAL BLOCK DIAGRAM	4-2
	4-2	HEAD MOVEMENT CONTROL TIMING	4-5
	4-3	READ INITIATE TIMING	4-6
	4-4	M <sup>2</sup> FM DATA ENCODING	4-7
	4-5	PRECOMPENSATION TIMING	4-8
	4-6	WRITE DATA TIMING	4-9
	4-7	PHASE LOCKED OSCILLATOR	4-11
	4-8	READ SYNCHRONIZATION TIMING	4-12
	4-9	BUS CONTROL TIMING	4-14
	4-10	CLK1/ AND CLK2/ TIMING	4-15
	4-11	SCHEMATIC DRAWING: INTERFACE BOARD	4-22
5	DISH	CETTE DRIVES	5-1
	<b>F</b> 4	EDD/EDGG INTERFACE LINES	FO
	5-1	FDD/FDCC INTERFACE LINES	5-6
	5-2	FDD DRIVER/RECEIVER CIRCUITS	5-7
	5-3	WRITE DATA TIMING	5-8
	5-4	READ DATA TIMING	5-10
	5-5	FLEXIBLE DISK CARTRIDGE	5-11

v

## LIST OF ILLUSTRATIONS (Continued)

Chapter	6	Title	Page
6	DISKE	TTE SYSTEM MICROPROGRAM	. 6-1
	6-1	INITIALIZATION	. 6-2
	6-2	MAINLINE	. 6-3
	6-3	LOAD MA LOWER	. 6-4
	6-4	LOAD MA UPPER AND START I/O	. 6-5
	6-5	READ RESULT BYTE	. 6-6
	6-6	IOPB LOADER/OP DECODE	. 6-7
	6-7	I/O FINISH	. 6-8
	6-8	SEEK	. 6-9
	6-9	FORMAT	. 6-10
	6-10	RECALIBRATE	. 6-12
	6-11	VERIFY/READ	. 6-13
	6-12	WRITE DELETED/WRITE	. 6-15
	6-13	ADDRESS PARAMETER CHECKER	. 6-16
	6-14	READ NEXT MEMORY WORD	. 6-17
	6-15	WRITE DATA FIELD	. 6-18
	6-16	WRITE CURRENT CHECK	. 6-19
	6-17	TIME_OUT	. 6-20
	6-18	ADDRESS MARK DETECT	. 6-21
	6-19	HEAD STEPPER	. 6-22
	6-20	READ DISK BYTE	. 6-23
	6-21	PROCESS ADDRESS FIELD	. 6-24
	6-22	WRITE ADDRESS FIELD	· 6-25
7	UTILI	ZATION	. 7-1
	7-1	CONNECTORS ON THE CHANNEL AND INTERFACE BOARDS	. 7-3
8	OPER	ATING CHARACTERISTICS	. 8-1
	8-1	SLAVE COMMAND TIMING – FDCC	. 8-2
	8-2	BUS EXCHANGE TIMING	. 8-3
	8-3	MASTER COMMAND TIMING	. 8-4
	8-4	STEP/SETTLING TIMINGS	. 8-6
	8-5	READ TIMING	. 8-7
	8-6	WRITE TIMING	. 8-7
	8-7	INDEX TIMING	. 8-8
	8-8	WRITE FAULT RESET TIMING	. 8-8

9

## LIST OF TABLES

Chapte	er	Title	Page
			584
1	INT	RODUCTION	
	1-1	DISKETTE DRIVE PERFORMANCE SPECIFICATIONS	1-3
2	OPE	RATIONAL SUMMARY AND PROGRAMMING CONSIDERATIONS	
	2-1	INTERRUPT CONTROL BITS	2-11
3	THE	CHANNEL BOARD	
	3-1 3-2 3-3 3-4 3-5 3-6 3-7	ACO INPUT SELECTION MICROINSTRUCTION BIT ASSIGNMENTS CONTROL PULSES AND LEVELS GENERATED BY MICROPROGRAM I-BUS SELECTION BY MASK FIELD BITS K-BUS INPUT SELECTION PIN LIST: P1 BUS CONNECTOR PIN LIST: P2 CONTROLLER CONNECTOR	3-7 3-9 3-10 3-12 3-13 3-17 3-19
4	THE	INTERFACE BOARD	
	4-1 4-2 4-3	PIN LIST: P1 BUS CONNECTOR	4-16 4-18 4-19
8	OPE	RATING CHARACTERISTICS	
	8-1 8-2 8-3 8-4	DISKETTE OPERATING SYSTEM/INTELLEC BUS AC CHARACTERISTICS DISKETTE OPERATING SYSTEM/DRIVE INTERFACE AC CHARACTERISTICS DISKETTE OPERATING SYSTEM DC CHARACTERISTICS (INTELLEC BUS) DISKETTE OPERATING SYSTEM DC CHARACTERISTICS (DRIVE/DISPLAY	8-1 8-5 8-9

#### 87.18AT 40-78H

	a.,

# CHAPTER 1

The INTELLEC Double Density Diskette Operating System provides a bulk storage capability for Intel's INTELLEC Microcomputer Development System. The Diskette System includes an intelligent controller and up to four diskette drives. Each drive provides 4,100,096 user-accessible data bits of storage with a data transfer rate of 500,000 bits/ second. The controller has been implemented with Intel's powerful Series 3000 Bipolar Computing Elements. The controller provides an interface to the INTELLEC System bus, as well as supporting the four diskette drives. The Diskette System records all data in the Intel soft-sectored format, described in Section 1.2.

#### **1.1 SYSTEM OVERVIEW**

In addition to two or four diskette drives, their enclosure(s) (two drives per enclosure) and power supplies, the Diskette System consists of the Channel Board and the Interface Board. These two printed circuit boards reside in the INTELLEC System cabinet and constitute the diskette controller. Each of the system components is shown in Figure 1-1, and described in the following paragraph:

The Channel Board is the primary control module within the Diskette System. The Channel Board receives, decodes and responds to channel commands from a Central Processor Unit (CPU) in the INTELLEC System. The Channel Board can access INTELLEC System memory to determine the particular diskette operations to be performed and to fetch the parameters required for the successful completion of the specified operations. The Channel Board also monitors Diskette System status and error conditions, and organizes these indications into 'result type' and 'result byte' words that can be read by a CPU in the INTELLEC System.

The control functions of the Channel and Interface Boards are provided by an 8-bit microprogrammed processor, implemented with Intel's Series 3000 Bipolar Computing Elements. The 8-bit controller includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit and 512 x 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. The processing and control capabilities of the Diskette System are achieved by execution of the microprogram.

The Interface Board provides the diskette controller with a means of communicating with the diskette drives, as well as with the INTELLEC System bus. Under control of the microprogram executed from the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), then cause the head to move to the proper track. The Interface Board accepts the data being read off the diskette, interprets certain synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and passes the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times. It also generates CRC characters which are appended to the data; this allows the data to be verified when it is subsequently read.



Figure 1-1

#### DISKETTE SYSTEM BLOCK DIAGRAM

1-2

When the diskette controller requires access to INTELLEC System memory, the Interface Board requests and maintains master control of the system bus, and generates the appropriate memory command.

When a CPU in the INTELLEC System issues a channel command to the Diskette System, the Interface Board acknowledges the command as required by INTELLEC System bus protocol.

Each diskette drive consists of read/write and control electronics (on a single printed circuit board), drive mechanism, read/write head, track positioning mechanism and the removable diskette platter. These components interact to perform the following functions:

- Interpret and generate control signals.
- Move read/write head to selected track.
- Read and write data.

Table 1-1 lists the performance characteristics for each diskette drive.

0	Separative (formatted)	Por Diale		E12 E12 butes
C	apacity (formatted)	Per Disk -		6 656 bytes
		Tel Track -		0,000 bytes
C	Data Transfer Rate:			500 kilobits/second
A	Access Time:	Track to Track -	10 ms	
		Settling Time -	10 ms	
1911 - A	is the late of given entered with the		000	
4	Average Access Time:		260 ms	
F	Rotational Speed:		360 RPM	
A	Average Latency:		83 ms	
F	Recording Mode:	(M <sup>2</sup> FM) Modified-	Modified Freque	ncy Modulation

#### TABLE 1–1 DISKETTE DRIVE PERFORMANCE SPECIFICATIONS

The remaining chapters of the manual deal with each of the system elements in detail. Chapter 2 describes the range of operations that can be performed by the Diskette System, and also provides specific information on how to program the system to execute each of the possible operations. Chapters 3 and 4 provide detailed information on the theory of operation for the Channel Board and the Interface Board, respectively. The final section in each of these chapters provides a complete schematic drawing of the board as well as a detailed pin list. The reader should continually refer to these schematic drawings in the course of reading the theory of operation sections.

NOTE: To avoid any confusion when referring to the schematics for the Channel and Interface Boards, or when reading the corresponding circuit descriptions, the following notation, concerning the active level of a signal, will apply:

Whenever a signal is active-low, its mnemonic is followed by a slash; for example MRDC/ means that the level on that line will be low when the memory read command is true (active). If the signal is subsequently inverted, thus making it active-high, the slash is omitted; for example, MRDC means that the level on that line will be high when the memory command is true.

Chapter 5 lists the manufacturer's information on the diskette drives. Chapter 6 provides the major state flow charts for the microprogram which is executed by the Series 3000 Bipolar Microcomputer Set (on the Channel Board), and which essentially controls operation of the Diskette System. Chapter 7 provides basic information on the installation and use of the Diskette System. Finally, Chapter 8 summarizes the AC and DC operating characteristics for the Diskette System.

Before proceeding to Chapter 2, however, we first provide a comprehensive review of the Intel soft-sectored recording format which is used by the Diskette Operating System.

#### 1.2 RECORDING FORMAT

This section summarizes the specifications for the soft-sectored recording format used by the Diskette Operating System.

#### Physical Data Format:

The physical data format is the format that the diskette controller circuitry must interact with. The elements of the physical data format are the hard index hole, index mark, sector address marks, sector headers, and data sectors. The index mark and sector address marks are recorded with unique clock patterns requiring the controller circuitry to accumulate the unique clock patterns for index and sector address mark identification. Figure 1-2 illustrates the general physical data format.

A 'byte', when referring to serial data (being written to or read from the diskette drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0 and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation bit cell 0 of each byte is transferred to the drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the diskette first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

Figure 1-3 illustrates the relationship of the bits within a byte and Figure 1-4 illustrates the relationship of the bytes for read and write data.

Data is recorded on the diskette using modified modified  $(M^2)$  frequency modulation as the recording mode. Data written on and read back from the disc takes the form shown in Figure 1-5. Clock bits are written only if there is no data bit in the bit cell and there was no data bit or clock bit written in the previous bit cell. By definition, a Bit Cell is the period (2 us) consisting of a clock bit time (1 us) and a data bit time (1 us). Figure 1-6 illustrates a Bit Cell.

#### Track Format:

Each track recorded on a diskette consists of 52 fixed length records along with necessary gaps for record updating. Figure 1-7 illustrates the format of one complete track.

Each field on a track is separated from adjacent fields by a number of bytes containing no data. These areas are referred to as gaps and are provided to allow the updating of one field without affecting adjacent fields. As can be seen from Figure 1-7, there are four different types of gaps on each track:

#### Gap 1 – Post-Index Gap

This gap is defined as the 28 bytes between Index Address Mark and the ID Address Mark for Sector one (excluding the address mark bytes). This gap is always 28 bytes in length and is not affected by any updating process.

#### Gap 2 - ID Gap

The 28 bytes between the ID Field and the Data Field are defined as Gap 2 (ID Gap). This gap does not vary in size.

#### Gap 3 – Data Gap

The 28 bytes between the Data field and the next ID field are defined as Gap 3 (Data Gap). The Data Gap may vary slightly in length after the adjacent Data field has been updated, due to differences in disk rotational speed between formatting and updating of individual data fields.

#### Gap 4 – Pre-Index Gap

The 338 bytes between the last Data field on a track and the Index Address Mark are defined as Gap 4 (Pre-Index Gap). Initially, this gap is nominally 338 bytes in length; however, due to write frequency tolerances and diskette speed tolerances this gap may vary slightly in length. Also, after the data field of record 52 has been updated this gap may again change slightly in length.

#### Address Marks:

Address Marks are unique bit patterns one byte in length which are used to identify the beginning of ID and Data fields and to synchronize the deserializing circuitry with the first byte of each field. Address Mark bytes are unique from all other data bytes in that each Address Mark contains an extra clock bit in bit cell 2. There are four different types of Address Marks used. Each of these is used to identify different types of fields:

#### Index Address Mark

The Index Address Mark is located at the beginning of each track and is a fixed number of bytes in front of the first record. The bit configuration for the Index Address Mark is shown in Figure 1-8.

#### **ID Address Mark**

The ID Address Mark byte is located at the beginning of each ID field on the diskette. The bit configuration for this Address Mark is shown in Figure 1-9.

#### Data Address Mark

The Data Address Mark byte is located at the beginning of each non-deleted Data Field on the diskette. The bit configuration for this Address Mark is shown in Figure 1-10.

#### **Deleted Data Address Mark**

The Deleted Data Address Mark byte is located at the beginning of each deleted Data field on the diskette. The bit configuration for this Address Mark is shown in Figure 1-11.

#### CRC Bytes:

Each field written on the diskette is appended with two Cyclic Redundancy Check (CRC) bytes. These two CRC bytes are generated from a cyclic permutation of the data bits starting with bit zero of the address mark and ending with bit seven of the last byte within a field (excluding the CRC bytes). This cyclic permutation is the remainder from the division of the data bits in the field (represented as an algebraic polynomial) by a generator polynomial G(X). For all fields recorded on a diskette, this generator polynomial is:

$$G(X) = X16 + X12 + X5 + 1$$

When a field is read back from a diskette, the data bits (from bit zero of the address mark to bit seven of the second CRC byte) are divided by the same generator polynomial G(X) and a non-zero remainder indicates an error within the data read back from the drive while a remainder of zero indicates the data has been read back correctly from the diskette or an undetectable error has been read back.











Figure 1-4 DATA BYTES





PATHO ALAS BATAS

2

10





1-9





















#### Figure 1-11 DELETED DATA ADDRESS MARK

#### CHAPTER 2

## OPERATIONAL SUMMARY AND PROGRAMMING CONSIDERATIONS

All diskette operations are initiated by a Central Processor Unit (CPU) within the INTELLEC System. Once initiated, however, the Diskette Channel completes the specified operation without further intervention on the part of the CPU. From the CPU's point of view, there are only three general steps required to complete any diskette operation:

- The CPU must prepare and store in system memory an I/O Parameter Block (IOPB) for each operation to be performed. An IOPB (seven bytes) specifies a particular diskette operation and provides all of the parameters required for execution of that operation.
- The CPU must then pass the memory address of the IOPB to the Diskette Channel.
- The CPU must process the result information from the Diskette Channel upon completion of the operation(s).

The preparation of the IOPB by the CPU, in itself, requires no interaction with the Diskette Channel. The passing of the memory address for the IOPB and the result processing, however, do require interaction. Six channel commands have been defined to allow the CPU to perform these interactive steps. Three of the channel commands are the result of the CPU executing an output instruction to a dedicated I/O port address, while the other three commands are the result of input instructions to dedicated ports. The six channel commands are:

- (1) Write memory address lower (output)
- (2) Write memory address upper and start the diskette operation (output)
- (3) Reset the channel (output)
- (4) Read subsystem status (input)
- (5) Read result type (input)
- (6) Read result byte (input)

The CPU outputs the memory address of the IOPB by executing channel commands 1 and 2. Upon execution of channel command 2, the Diskette Channel will request master control of the INTELLEC System bus, fetch the diskette instruction and associated parameters from the IOPB, and proceed to perform the specified diskette operation. The diskette instruction byte in the IOPB can specify any one of seven diskette operations:

- (1) Recalibrate (seek track 00)
- (2) Seek
- (3) Format a track
- (4) Write data (with data address marks)
- (5) Write data (with deleted address marks)
- (6) Read data
- (7) Verify CRC

The Diskette Channel can interrupt the CPU when the operation is completed or when the diskette ready status changes. The host system software can implement its CPU interrupt mechanism via this direct interrupt feature or it can 'poll' the Diskette Channel by executing channel command 4 (read subsystem status). When the CPU determines that the operation sequence has been completed (either by receiving an interrupt request or by reading

#### FORMAT TRACK

This operation initializes the track specified in byte 4 of the IOPB, by writing all address marks, gaps, address fields and data fields, as shown in Figure 2-1. The various address marks and fields are defined in Section 1.2.

The method of assigning logical sector addresses, which are written into the sector address fields, is specified by bit 6 of the first IOPB byte (the channel word). If this bit is equal to logical 0 the sequence of logical sector addresses will match the physical sequence on the diskette (i.e., sector address '01' is written into the first physical sector after the index mark, sector address '02' is written into the second physical sector, and so on). In addition, the data byte stored in the memory location specified by the 16-bit buffer address contained in bytes 6 and 7 of the IOPB will be written into the 128-byte locations of each sector's data field. No other data bytes need to be stored in this buffer.

If, on the other hand, the sequence of logical addresses being assigned to the sectors is 'random' (that is, do not match the physical sequence of sectors), bit 6 of the channel word will be equal to logical 1, and 104 bytes (52 pairs) of data will be stored in memory beginning at the 16-bit buffer address contained in bytes 6 and 7 of the IOPB. Each of the 52 pairs of data bytes will specify the logical sector address to be written into the sector address field of the corresponding physical sector, and the data character which will be written (128 times) into the data field portion of that sector. For example, if the first four bytes of the buffer are:

Byte	Contents (hex)
1	01
2	FF
3	0E
4	00
·	an remedition where this

Then, sector address '01' will be written into the sector address field of the first physical sector after the index mark, and 'FF<sub>16</sub>' (all ones) will be written into each of the 128 byte locations in the data field portion of this sector. The sector address '0E<sub>16</sub>' (14<sub>10</sub>) will be written into the sector address field of the second physical sector (i.e., the sector which is physically next to the first sector), and '00<sub>16</sub>' (all zeros) will be written into each of the 128 byte locations in the data field portion of this sector. And so on, until a logical sector address has been written into the sector address field of each of the 52 physical sectors on the track, and a data byte is written into each of the 128 byte locations in the data field portion of each of the 52 sectors.

The firmware implementation of the format command is such that in order to format track n ( $n\neq \emptyset$ ), track n-1 must already be formatted (i.e., already have readable address information written into it). Track 0 can always be formatted even if no valid address information is written on the disk.

During formatting, a 'data mark' (i.e., a character which has a clock pattern equal to  $70_{16}$  and a data pattern equal to  $0B_{16}$ ; see Figure 2–2) is written into the 'data/deleted data address marl ' character position of each sector (i.e., the character position immediately preceding the 128 byte date field.)

If, when the format track operation is initiated, the head is not already positioned over the track specified in byte 4 of the IOPB, the format track instruction will cause the head to move (seek) to the proper track before the actual formatting begins.

#### WRITE DATA

This operation transfers N x 128 bytes of contiguous data from memory to the diskette. N represents the number of sectors to be written. N is specified by the contents of byte 3 of the IOPB. The 16-bit buffer address stored in bytes 6 and 7 of the IOPB specifies the memory location containing the first data byte to be transferred. The contents of bytes 4 and 5 of the IOPB (track and sector addresses, respectively) specify the logical address of the first sector to be written into.

executed sequentially ('read result type' first), and should be executed only in response to an interrupt request from the Diskette Channel; execution at other times could produce erroneous result data.

The use and format of each of the six channel commands is described below:

#### WRITE MEMORY ADDRESS LOWER (OUTPUT)

This channel command outputs the low order byte of the 16-bit memory address that points to byte 1 ('channel word') of the IOPB.

System address bus: BASE + 1

System data bus:

Eight least significant bits of the 16-bit memory address that points to the first IOPB.

#### WRITE MEMORY ADDRESS UPPER AND START THE DISKETTE OPERATION (OUTPUT)

This channel command outputs the high order byte of the 16-bit memory address that points to byte 1 of the IOPB. This command also causes the Diskette Channel to begin executing the diskette operation specified in byte 2 (instruction byte) of the addressed IOPB.

System address bus:

System data bus:

Eight most significant bits of the 16-bit memory address

#### **RESET DISKETTE SYSTEM (OUTPUT)**

This output channel command causes all control logic in the Diskette Channel to be reset in an initialized state. If this command is issued while a 'write data' diskette operation is in progress, the data in the sector currently being written will be garbled. This command is intended to clear a 'hang up' in the Diskette Channel.

System address bus:

System data bus:

Not used.

BASE + 7

BASE + 2

#### READ SUBSYSTEM STATUS (INPUT)

This input channel command causes the Diskette Channel to return.

bit 0 - ready status of drive Ø

bit 1 - ready status of drive 1

bit 2 - state of the channel's interrupt flip-flop

bit 3 - controller presence indicator

- bit 4 double density controller presence indicator
- bit 5 ready status of drive 2
- bit 6 ready status of drive 3

Each 128 byte data field will be preceded by a 'data' address mark (see Figure 2–2) that is used for synchronization. Two bytes (16 bits) of CRC check bits will be generated and written after each data field; the CRC bytes are generated from the address mark, as well as the 128 data bytes.

A multi-sector operation (i.e.,  $N \ge 2$ ) may begin at any sector, but must not go beyond the last logical sector on a track (sector 52).

If the head is not already positioned over the track specified in byte 4 of the IOPB, the write data instruction will cause the head to move (seek) to the proper track before the actual writing begins.

#### WRITE 'DELETED' DATA

This operation is identical to the WRITE DATA operation, described above, except that each 128 byte data field is preceded by a 'deleted data' address mark, shown in Figure 2-3.

#### READ DATA

This operation transfers N sectors of data (128 bytes per sector) from diskette to memory. N is specified by the contents of byte 3 of the IOPB. The contents of bytes 4 and 5 of the IOPB (track and sector addresses, respectively) specify the logical address of the first sector to be read. The 16-bit buffer address stored in bytes 6 and 7 of the IOPB specifies the memory location into which the first data byte will be written.

Two bytes of CRC check bits will be generated as each sector is being read. When the 'data' address marks and all 128 data bytes of a sector have been read, the generated CRC bits are compared with the 16 CRC bits previously written. If there is a mismatch, a CRC error is indicated (see Section 2.4).

A multi-sector operation (i.e.,  $N \ge 2$ ) may begin at any sector, but must not go beyond the last logical sector on a track (sector 52).

If the head is not already positioned over the track specified in byte 4 of the IOPB, the read data instruction will cause the head to move (seek) to the proper track before the actual data reading begins.

#### VERIFY CRC

This operation is identical to the READ DATA operation, described above, except that no data is transferred to memory.

#### 2.3 I/O PARAMETER BLOCK

The CPU in the INTELLEC System initiates a diskette operation by outputting a 16-bit address that points to the beginning (the channel word) of the I/O Parameter Block (IOPB) in system memory. The Diskette Channel then accesses the IOPB. An IOPB specifies one of the diskette operations (see Section 2.2) and provides all of the parameters required for the completion of that operation. An IOPB consists of seven bytes, as shown in Figure 2-4.

#### Byte 1. Channel Word

This byte contains channel control information to be used by the Diskette System. Bit assignments in this byte are as follows:

	7 6 5 4 3 2 1 0					
	X			XX	X	X = Don't Care
Random Format Sequence -			1			 — Data Word Length
Interrupt Control	1990C	28. 4	100			

If the type code = 10, the controller has detected a change in the ready status of a drive and the contents of the result byte will indicate the current ready status of the diskette drives:



NOTE: A logical 1 means that the drive is currently ready; a logical 0 means the drive is not ready. It is the responsibility of the host system software to maintain appropriate tables to track these status changes. There is one instance in which a drive can appear 'not ready' to the host system, when in fact it is ready. For example, assume that while drive 0 is selected, drive 1 just goes not ready then returns to the ready state (perhaps the diskette platter was changed). When the drive 0 operation is completed, the diskette controller will return two consecutive status change interrupts, the first showing drive 1 not ready, the second showing drive 1 ready. The first interrupt, indicating drive 1 to be not ready, is returned even though the drive is now actually ready because it is important that the operator know that the ready status of the drive changed while the other drive was selected. For instance, this would protect against inadvertently accessing an 'unknown' disk, if the drive went not ready then ready again because someone changed disk platters.

#### 2.2 DISKETTE OPERATIONS

The Diskette System is capable of performing seven different operations: recalibrate, seek, format track, write data (with data marks), write data (with deleted data marks), read data, and verify CRC. To initiate any diskette operation, the CPU will output both bytes of the 16-bit memory address that points to the first byte of an I/O Parameter Block (IOPB). The second byte in the IOPB specifies one of the seven diskette operations (see Section 2.3 for IOPB format). After the Diskette System receives the upper byte of the 16-bit memory address, it accesses the IOPB to determine the operation to be performed and to acquire the various parameters that are necessary for execution of the diskette instruction. The Diskette System will perform the specified operation, then set its interrupt flip-flop.

NOTE: The Diskette Channel automatically unloads the read/write head after a fixed length of time following a diskette operation. This feature is meant to reduce head wear. The feature is implemented by counting index pulses after a 'read result byte' channel command is executed. When the specified count is achieved, the head is unloaded, and the count is re-initialized. At present, the count is set for 6; that is, the head will remain loaded for at least five complete revolutions following each diskette operation or group of linked diskette operations.

The seven diskette operations are defined in the following paragraphs:

#### RECALIBRATE

This operation causes the head of the selected diskette unit to be moved over track 00. The diskette drive's track 0 sensor is sampled to determine successful completion of this operation. This is often the first instruction executed after a diskette is loaded, or when a seek error occurs (see Section 2.4).

#### SEEK

This operation causes the head of the selected diskette unit to be moved over the track specified in byte 4 of the IOPB. The Diskette Channel will verify the head position by reading the track address from the diskette platter before completing the operation. If at the completion of the head movement, the head is not over the expected track, a 'seek error' will be indicated (see Section 2.4).

0	DA05 . 4		
System address bus:	BASE + Ø	(1 CD)	
Sustam data busi	76512	(LSB)	
System data bus.	10543 10111		
agical 1 = drive 3 ready			Logical 1 - drive 0 reader
$p_{i}$ $r_{i}$ $r_{i$	T ↑ ↑ ↑ ↑	Υ Υ <b>Έ</b>	logical 0 = drive 0 ready
	naven of stress	a alactada Y	Lingical 0 - drive 0 hot ready
prical 0 = drive 2 ready			logical I = drive I ready
	ST PERSONAL PROPERTY.	NAS CREAT PARTS	Liogical 0 – drive i not ready
ogical I = double density preser		L	logical 1 = interrupt pending
bgical U = double density not p	resent		logical U = no interrupt pending
	L		logical 1 = controller present
			logical 0 = controller not present
nis input channel command cau ast significant bits specify one	uses the Diskette Cha of four different typ	annel to return o bes of result byt	eight bits of information to the CPU. The two e (see next paragraph) associated with diskette
perations.			
the second s			
System address bus:	BASE + 1		
	7 0 5 4 0 4	(LSB)	
System data bus:			
			Tues Cada
		$\uparrow$ $\uparrow$	
			10 – Result byte contains diskette
			ready status
			01,11 - Reserved
	READ	RESULT BYTE	(INPUT)
his input channel command cau retation of these bits is depende he 'read result byte' channel co	uses the Diskette Cha ent upon the type co ommand should only	onnel to return ode returned in be executed af	eight bits of information to the CPU. The inter- the result type word (see previous paragraph). ter a 'read result type' command has been executed
System address bus:	BASE + 3		
	If the type cod	le in the result	type word = 00 the result byte input on the data
System data bus:	in the type cou		e Section 2.4 for error explanations) and will be
System data bus:	bus will contai	n error hits (see	
System data bus:	bus, will contai formatted as fo	in error bits (see	and standard of million breakings and as a second standard
System data bus:	bus, will contai formatted as fo	In error bits (see Ilows: (LSB)	ic report obtained, dominative contains the Oldardte Ona
System data bus:	bus, will contai formatted as fo 7 6 5 4 3 2	In error bits (see blows: (LSB) 2 1 0	ne man stander sommende seiner von Orslandte Gen sonder von en
System data bus:	bus, will contai formatted as fc	In error bits (see blows: (LSB) 2 1 0	nen of much Standard Commence Standard Oldardte Centre s much Standard Commence State s autore where = 1 set
System data bus: ot ready	bus, will contai formatted as fc	In error bits (see ollows: (LSB) 2 1 0	Deleted record
System data bus: ot ready	bus, will contai formatted as fc	(LSB)	Deleted record CRC error
System data bus: ot ready rite error rite protect	bus, will contai formatted as fc	(LSB)	Deleted record CRC error Seek error
System data bus: ot ready rite error rite protect	bus, will contai formatted as fo	(LSB)	Deleted record CRC error Seek error Address error



the interrupt status), the CPU should execute channel commands 5 and 6 (read result type and read result byte) to determine whether the diskette operations were successfully completed, and if not which type of error occurred.

Thus, in summary, we see that certain channel commands are executed by the CPU to point the Diskette Channel to an IOPB in system memory, and initiate the operation sequence. The Diskette Channel, then, accesses the IOPB to perform the diskette operation specified by the instruction byte of the IOPB. The Diskette Channel will, if enabled by the IOPB, generate an I/O complete interrupt request upon completion of each diskette operation or detection of an error. The CPU, then, executes other channel commands to determine the result of the diskette operation.

In the preceding paragraphs, we have mentioned the channel commands, diskette operations and the IOPB without defining them explicitly. That is because up until now, our primary intention has been to identify clearly the function of each in the overall operation of the Diskette Channel. In the subsequent sections of this chapter, however, we will provide detailed information on the use and format of the channel commands (Section 2.1), the diskette operations (Section 2.2) and the IOPB (Section 2.3). Section 2.4 will define each of the error conditions that can be indicated when the 'read result byte' channel command is executed by the CPU.

#### 2.1 CHANNEL COMMANDS

There are six channel commands to which the Diskette Channel will respond. Three of the channel commands are issued when a CPU in the INTELLEC System executes output (I/O write) instructions with the appropriate eight-bit I/O addresses. The other three commands are issued when the CPU executes input (I/O read) instructions with the appropriate I/O addresses.

When the CPU executes one of the output channel commands, it activates the I/O write (IOWC/) line and duplicates the appropriate 8-bit I/O address on address lines ADRO/ - ADR7/ and ADR8/ - ADRF/ of the INTELLEC System bus. Depending on the particular channel command, the CPU may also place relevant data on data lines DATO/ - DAT7/ of the INTELLEC System bus. The CPU maintains the data lines until the Diskette Channel returns the transfer acknowledge (XACK/) signal.

When the CPU executes one of the input channel commands, it activates the I/O read (IORC/) line and duplicates the appropriate I/O address on both halves of the INTELLEC System bus. The CPU expects the Diskette Channel to activate the transfer knowledge (XACK/) line when it has placed the requested data on data lines DAT0/ – DAT7/.

The Diskette Channel differentiates between the different channel commands by interrogating the I/O read (IORC/) and I/O write (IOWC/) lines and the three least significant address lines (ADRO/ - ADR2/). The five most significant I/O address lines (ADR3/ - ADR7/) define the switch-selectable BASE address for the Diskette Channel.

If the Diskette Channel is not busy, it will respond to an output channel command within 3 microseconds. If it is busy, the 'write MA lower' and 'write MA upper' commands are ignored; no acknowledge is returned. (Note: Because no acknowledge is returned in this case, it could be possible to 'hang up' the host system if the system does not include a Fail Safe time-out provision, as is provided on the Front Panel Control Module in the INTELLEC System). The 'reset' command, however, is acknowledged even if the Diskette Channel is busy. 'Reset' is executed immediately (if issued during a data write operation, garbled data will be written).

The Diskette System responds to 'read subsystem status' and 'read result type' input channel commands within 1 microsecond. The information returned in response to a 'read subsystem status' command is always valid. The eight bits of data returned in response to a 'read result type' command, however, are only valid if the Diskette Channel had previously issued an interrupt request to the CPU. The Diskette Channel will, if not busy, respond to a 'read result byte' input command within 3 microseconds. If the Diskette Channel is busy, however, it ignores the 'read result byte' command (i.e., no acknowledge is returned). The 'read result type' and 'read result byte' commands must be

The 'random format sequence' bit (6) specifies the method of assigning logical sector addresses when formatting a track. If this bit is reset (logical 0), sector addresses are assigned in sequential order. If this bit is set (logical 1), sector addresses are assigned in random order according to the pattern listed in the 52 byte memory buffer, which begins at the location addressed by the contents of IOPB bytes 6 and 7. (Refer to the description of the FORMAT TRACK operation in Section 2.2.)

The 'interrupt control' bits (4 and 5) enable or disable Diskette Channel interrupts according to the scheme shown in Table 2–1.

The 'data word length' bit (3) must be reset (logical 0) when the Diskette Channel is being used with 8-bit systems, or set (logical 1) when being used with 16-bit systems. This bit must be logical 0 when being used with the INTELLEC System (an 8-bit system).

ВҮТЕ	IOPB FORMAT
*1	Channel Word
2	Diskette Instruction
3	Number of Records
4	Track Address
5	Sector Address
6	Buffer Address (Lower)
7	Buffer Address (Upper)

Figure 2-4 I/O PARAMETER BLOCK (IOPB) FORMAT

ſ	able	2-1	INT	ERRUPT	CONTROL	BITS

BIT:	5	4	FUNCTION
	0	0	I/O complete interrupt request to be issued
			(a) upon completion of diskette operation,
			(b) upon detection of an error in any operation.
	0	1	All I/O complete interrupts are disabled.
	1	1	Illegal code
	1	0	The Arguide study provides the define mentalishes reals white any routed

#### Byte 2. Diskette Instruction



The 'unit select' bits (4 - 5) specify the drive address as follows:

00	=	drive	0
01	=	drive	1
10	=	drive	2
11	=	drive	3

The 'data word length' must contain the same value as the corresponding bit in the channel word (byte 1).

The 'op code' bits (0-2) specify one of the seven diskette operations (refer to Section 2.2):

BIT:	3	2	1	OPERATION	
	0	0	0	No operation	
	0	0	1	Seek	
	0	1	0	Format Track	
	0	1	1	Recalibrate	
	1	0	0	Read data	
	1	0	1	Verify CRC	
	1	1	0	Write data	
	1	1	1	Write 'Deleted' Data	

#### Byte 3. Number of Records

This binary number specifies the number of sectors to be transferred. Multi-sector operations are allowed, but they must not go beyond the last sector on a track (sector 52); that is, an address error (see Section 2.4) will be indicated if (starting sector address) + (number of records) >  $52_{10}$ . Therefore, the maximum block transfer is 52 sectors (from sector 1 to sector 52).

#### Byte 4. Track Address

This binary number identifies the track. Acceptable values are 0 to  $4C_{16}$  (76<sub>10</sub>), inclusive.

#### Byte 5. Sector Address

Bits 5 through 0 of this byte contain a binary number which specifies the first sector to be accessed during transfer operations. Acceptable values are 1 to  $34_{16}$  ( $52_{10}$ ), inclusive. Bits 6 and 7 are not used.

#### Byte 6. Buffer Address (Lower)

This byte contains the eight least significant bits of the 16-bit buffer memory address.

#### Byte 7. Buffer Address (Upper)

This byte contains the eight most significant bits of the 16-bit buffer memory address. Bytes 6 and 7 together contain the 16-bit address of the first word of the buffer in system memory. During read data operations, the data from the

diskette is transferred to the buffer. During write operations, data from the buffer is written to diskette. During format track operations, the address assignment pattern and/or the data field 'format characters' are stored in the buffer.

#### 2.4 ERROR INDICATIONS

If the CPU executes a 'read result byte' channel command (in response to a 'read result type' channel command which returned a code of 00), the Diskette Channel will return the following result word on the system data bus:



The bits are defined as follows:

NOT READY. This bit (7) indicates that the selected unit was not ready or that the selected unit changed to a not ready state during an operation.

WRITE ERROR. This bit (6) indicates that, during a write operation, a condition existed which precluded data integrity. This error is detected by the drive and monitored by the Diskette Channel controller. An example of a condition that could cause this error is an attempt to write through an unloaded head.

WRITE PROTECT. This bit (5) indicates that the selected drive contains a diskette platter which is in the 'read only' mode. This condition is checked on format track, write data (with data address marks) and write data (with deleted data address marks) operations.

DATA OVERRUN/UNDERRUN ERROR. This bit (4) indicates that the Diskette System controller was not able to service a byte transfer request from the drive before the next request occurred. The data byte is 'lost'.

ADDRESS ERROR. This bit (3) indicates that the disk address received from the CPU is invalid; that is:

- track address >7610,
- sector address = 00,
- sector address > 52<sub>10</sub>, or
- sector address + number of records > 5210

SEEK ERROR. This bit (2) indicates that, at the completion of a head movement sequence, the head is not positioned over the expected track. This bit indicates the Diskette System controller and/or drive are malfunctioning, and a recalibrate diskette operation (see Section 2.2) should be performed. Because all of the diskette operations may implicitly cause the head to move, a seek error can occur during any diskette operation.

CRC ERROR. This bit (1) indicates that the two CRC characters generated during a read data or verify CRC operation were not the same as the two CRC characters appended to the data field (see Section 1.2) when it was written on diskette.

DELETED RECORD. This bit (0) indicates that a sector addressed during a read data or verify CRC operation was preceded by a deleted data address mark.

Three other error conditions are indicated when more than one error bit is true:

ID CRC ERROR. If the address error (3) and CRC error (1) bits are true, it indicates that the CRC characters generated

during the reading of an ID field (see Section 1.2) were not the same as the CRC characters appended to the field when it was written by a format track operation.

NO ADDRESS MARK. If the address error (3), seek error (2) and CRC error (1) bits are true, it indicates that no address mark (see Section 1.2) was encountered for a full revolution of the diskette. This usually indicates that the track has not been formatted.

DATA MARK ERROR. If the address error (3), seek error (2), CRC error (1), and deleted record (0) bits are true, it indicates that the data field of a particular sector was not preceded by either a data mark or a deleted data mark.

The life are defined as fallower.

NOT READY. "Flucture (7) indicating that the velocited and user not reach as that the released of the second of th

WRITE ERROR. This for the Indiana flat, during a write optighter a condition events when reached the set pily. This error is thereight by the this and manismatch by the Destered Science Controls. An exercise of condumn interested entitie the error is an atomistic to territe character or unitediat tests.

shull TE PROTECT. Tele uit 18: hubdates that the sciented doors contained a prostories which in the bank with reads. This emplition is charted an format track, write data work data advines charter and and this reall indefen data addicts methors, constitutes.

**Barth Overeneide Athlese Break Erenine - This in: 14** millions and the Deballine System along the test start of the law of the source of the law of the second start without start without a start

Contract of 1955 and more forwards which the old and sold with the 201 rate of 1 1000 45 States of 1

- Anti- synthesis that the
- All + sector writes a
- to as \$8. Sector as a sector a
- er?" < driver a month + dender adde 🔹

SECULARIADAL This bit ("B indicates that, at the abailitien of a fault-increment security is to do not concernaand thereigned a logic, for the indicate the B-sector System and encrements are an information of a logic sector signs attacked within the Sector 12 shalled to perform 4. Brows all of the distribution of an environment of an distribution the media is inside, it has end accordance and the literate attack in distorts device of an environment distribution the media is inside, it has end accordance of the literate attack in the sector of an environment of the media is inside, it has end accordance of the literate attack of the distribution of the sector of the literate attack of the sector of the sec

GNG ERMON, The bit (1) inducing this did to a GNC attaceptic generation indugts with due to worky CRC to Classes were not the articless till tool CRC displaying in the term field like Station 1.7 when it was were the the disparts

**DELETVID RECORD** This bit (D) redicates that a stream who specificates a read a stator who who term

Thirde entries store that a second method when more than a store and the second

The raise are another than and the search of the search of

#### CHAPTER 3

### CHANNEL BOARD

The Channel Board is the primary control module within the Diskette System. The Channel Board receives, decodes and responds to channel commands from a Central Processor Unit (CPU) in the INTELLEC System. The Channel Board can access INTELLEC System memory to determine the particular diskette operations to be performed and to fetch the parameters required for the successful completion of the specified operations. The Channel Board also monitors subsystem status and error conditions, and organizes these indications into 'result type' and 'result byte' words that can be read by a CPU in the INTELLEC System.

The control functions of the Channel and Interface Boards are provided by an 8-bit microprogrammed processor, implemented with Intel's Series 3000 Bipolar Microcomputer Set. The 8-bit controller includes four 3002 Central Processing Elements (2-bit slice per CPE), a 3001 Microprogram Control Unit and 512 x 32 bits of 3604 programmable-read-only-memory (PROM) which stores the microprogram. The processing and control capabilities of the diskette controller are achieved by execution of the microprogram.

The Channel Board resides within the INTELLEC System cabinet. The Channel Board, together with the Interface Board, constitute the Diskette Channel.

#### 3.1 FUNCTIONAL ORGANIZATION OF THE CHANNEL BOARD

For description purposes, the circuitry on the Channel Board can be divided into six functional blocks (see Figure 3-1):

- Channel command block
- Micro control unit (MCU) block
- Microprogram memory block
- Central processing element (CPE) block
- Data/clock shift register (SR) block
- Data flow control block

The CHANNEL COMMAND BLOCK is responsible for recognizing and decoding channel commands being executed by a CPU in the INTELLEC System. When the channel command block recognizes the switch-selectable BASE address of the Diskette System on the INTELLEC System address bus, it decodes the three least significant address bits (ADR0/ – ADR2) to determine which of the six channel commands is being executed (see Section 2.1). The three address bits are also latched and made available to the MCU block, which is ultimately responsible for controlling the diskette controller's response to a channel command. The channel command block also includes the interrupt latch which stores the fact that an interrupt request has been issued to the CPU by the microprogram.

The MICRO CONTROL UNIT (MCU) BLOCK accepts and decodes the three address bits from the channel command block (ADR0/ – ADR2/) specifying a channel command or the three least significant data outputs from the CPE block (D0 – D2) specifying one of the seven diskette operations. The two groups of 3 bits select one of the ten routines which implement the channel commands and I/O operations. Having determined the microprogram routine to be executed, the MCU block then generates and outputs the appropriate nine-bit memory address from the microprogram memory. The MCU continuously examines the two flag control lines and the seven address control lines (ACO – AC6) from the microprogram memory block to determine the address of the next microinstruction to be fetched and executed.

#### E GETTALD.

#### CHARREL BOARD

(b) Crannel Joans 1 Malgaments cannot medale within the Differing System. The Chornel Arris 1 weight data will express to example generating from a Carquet Program Unit (GPO) in the 1976 F. 2017, data. The control lored can gains (INTELLEC Systems at more to determine the particular differing to extra the control of feed with an example of the the distribution of the reaction of the reaction determine. For a second control window extra provide and other conditions and require these militances are from the data with a control of the provide with an extra second control for a second line and the reaction of the re



Self CROTEROL USAT HELL BLOCK respect to decode the domestic to the term the term the state of the term the state of the term is a self of the term is the term is a self term in the term.
Self CROTEROL ADDEC, anothers a channel comment of the term even self term rate which is from the UPD is a term in the term is a self term in the term is a self term in the term is a self term.
Self CROTEROL ADDEC, anothers a channel comment of the term even self term rate which is from the UPD is a self term in the term is a self term in term in the term is a self term in term in the term is a self term in term in term is a self term in term in the term is a self term in term in term is a self term in term in term is a self term in term in term in term in term is a self term in term in term in term is a self term in ter

Figure 3-1 CHANNEL BOARD: FUNCTIONAL BLOCK DIAGRAM

The MICROPROGRAM MEMORY BLOCK, as its name implies, stores the microprogram. The microprogram memory is organized into 512 words of 32 bits each. The nine address bits from the MCU block determine which 32-bit micro-instruction will be output from the microprogram memory. Nine bits of the microinstruction (the address control and flag control bits) are applied to the MCU block, as mentioned above, while the seven function bits (F0 – F6) are applied to the CPE block and specify the operation to be performed by the processing elements. The other sixteen bits of the microinstruction words perform a variety of control functions, that will be described in Section 3.2.

The CPE BLOCK includes four Intel 3002 Central Processing Elements, which form an 8-bit processor. The CPE block receives data from the data flow control block and the data/clock shift register block and receives status information from the Interface Board. The CPE can operate on these various types of input data under the direction of the function and mask control bits from the microprogram memory. The results of these arithmetic/logical operations can then be output onto the eight most significant system address lines (ADR8/ – ADRF/) or the eight CPE data lines (D0 – D7). D0 – D7 are, in turn, made available to the MCU block, the data/clock shift register block and the data flow control block.

The DATA/CLOCK SHIFT REGISTER BLOCK includes the shift registers that accept the serial data bits and the serial clock bits and input them, in parallel, to the CPE block during read operations. During write operations, the data and clock bytes are (parallel) loaded into the shift registers from the CPE block and shifted out (serially) to the Interface Board.

The DATA FLOW CONTROL BLOCK routes data from the CPE data lines (D0 - D7) to the eight least significant INTELLEC System address lines (ADR0/ - ADR7/) or to either the lower or upper eight lines of the INTELLEC System data bus (DATA0/ - DATA7/ or DATA8/ - DATAF/). This block also routes data from either half of the INTELLEC System data bus onto the memory data input lines (MD0/ - MD7/) that feed the CPE block.

#### 3.2 THEORY OF OPERATION: CHANNEL BOARD

In this section we will describe the circuitry on the Channel Board. We will divide this theory of operation discussion into six subsections, each dealing with one of the functional blocks defined in Section 3.1.

The Channel Board accepts/transmits signals, data and power through three different PC edge connectors:

- P1 Bus connector (to/from INTELLEC System bus)
- P2 Controller connector (to/from Interface Board)
- J1 Test points only

To avoid any ambiguity when referring to connector pins in subsequent paragraphs, we will always list the connector as well as the pin whenever such references are required; for example, P1-57 refers to pin 57 on connector P1. Pin lists for the three connectors are provided in Section 3.3.

The schematic drawing (4 sheets) for the Channel Board is also provided in Section 3.3.

#### 3.2.1 Channel Command Block

The channel command block recognizes and decodes all channel commands directed to the diskette controller. This block includes an eight position switch (S1) for BASE address assignment, eight 74LS86 EXCLUSIVE–OR gates for address recognition, two 3205 three-to-eight decoders, two 7474 D-type flip-flops, a 74175 quad latch, and other assorted gating circuits, as shown on sheet 1 of the board schematic (Section 3.3).

TABLE 3-3 (CONTINUED)

CONTROL FUNCTION DEFINITIONS (CONTINUED)				
RDYRS	1	This pulse resets the Drive Ready flip-flops on the Interface Board.		
WFLRS	-	This level generates the write fault reset pulse to the selected drive.		
GTR43	-	This pulse sets the low current mode for writes on tracks greater than 4310.		
NGT43	1	This pulse resets the low current mode for writes on tracks equal to or less than 4310.		

#### TABLE 3-4 I-BUS SELECTION BY MASK FIELD BITS

	INPUT FIELDS*						
MASK BITS	DATA SHIFT REGISTER (A36 and A29) OUTPUTS	CLOCK SHIFT REGISTER (A34 and A27) OUTPUTS	ERROR LINES (DOR, WRT PROT, WRT ERR, SEL DR NRDY)	STATUS LINES (DRO, DR1, STOP, TRACK00)			
				22 (27) (27) (27) (27) (27) (27) (27) (2			
M7 =	1	1	1	1			
M6 =	0	0	ATEC - 197AG .N	1			
M5 =	0	0 - 00 - 000	0	1/0/18			
M4 =	1	1	0	0			
M3 =	0	- AROT/ 1	0	0			

An input field will be multiplexed into the I inputs of 3002 CPE array if the mask bits reflect the values listed for that field and if the K-Bus select line, S0 (bit 9 of the current microinstruction) is high (logical 1). Refer to Section 3.2.4 for a more complete description of the 3002 CPE array inputs.

3) Providing generalized inputs to the K-bus inputs of the 3002 CPE array. The mask bits are multiplexed through two 8234 multiplexer devices and into K-bus inputs of the CPE array. The selection bits are provided by S0 and S1 (bits 9–10 of the current micro-instruction). Table 3–5 correlates the levels on the S0 and S1 lines with the K-bus inputs.

#### 3.2.4 Central Processing Element (CPE) Block

The central processing element (CPE) block executes the function indicated by each microinstruction output from the microprogram memory. The CPE block includes an array of four Intel 3002 Central Processing Elements, as well as four 8234 and one 8233 eight-to-four multiplexers that provide various inputs to the CPE array, as shown on sheet 4 of the board schematic (Section 3.3).
If a 'stop diskette operation' command is being received, output 3 from the decoder goes true, asserting a low level on the SET STOP/ line (pin P2-31). The subsequent low-to-high transition on SET STOP/ clocks the stop latch reset (i.e., the active-low state). After the stop latch is sampled, the microprogram presets (i.e., clears to the non-active-high state) the latch.

If a 'reset channel' command is being received, output 7 from the decoder goes true, asserting a low level on the RESET/ line to the Interface Board (pin P2-49).

#### 3.2.2 Micro Control Unit (MCU) Block

The micro control unit (MCU) block provides the addresses for the microprogram memory. Since the microinstructions which are fetched from microprogram memory and executed by the central processing elements define the specific functions performed by the Channel Board, the MCU block can be considered the primary source of control for the diskette controller. In addition to an Intel 3001 Microprogram Control Unit device, the MCU block includes an 8234 eight-to-four multiplexer, a 74151 eight-to-one multiplexer and a few gating circuits, as shown on sheet 3 of the board schematic (Section 3.3).

The Intel 3001 Microprogram Control Unit controls the sequence in which microinstructions are fetched from the microprogram memory. Its functions include the following:

(A functional block diagram of the 3001 MCU is shown in Figure 3-2.)

- Maintenance of the microprogram address register
- Selection of the next microinstruction based on the contents of the microprogram address register
- Decoding and testing of data supplied via several input busses to determine the microinstruction execution sequence
- Saving and testing of carry output data from the central processor (CPE) array
- Control of carry/shift input data to the CPE array
- Control of microprogram interrupts

Address control information is supplied to the 3001 at inputs ACO - AC6. AC1 - AC6 are provided directly from bits 27 - 32 of the microinstruction currently being fetched from microprogram memory (see Section 3.2.3). The ACO input, however, is supplied by the output of the 74151 eight-to-one multiplexer.

Five control lines from the Interface Board (AZ, INDEX, XFER REQ, TIME OUT and F), one line from the CPE block (CO) and one line from the channel command block (BUSY START) are applied to the 74151 inputs along with the ACO bit (bit 26) from the microinstruction currently being fetched. The three select lines applied to the A, B and C inputs on the 74151 section specify which of the eight lines are actually multiplexed through to the ACO input on the 3001 device. The three select lines are supplied by bits 14, 15 and 16 (INO, IN1 and IN2) of the current microinstruction. Table 3–1 correlates the values in bit positions 14, 15 and 16 of the current micro-instruction with the control line which is multiplexed into the ACO input on the 3001 section.

The 'flag logic' input (F1) to the 3001 device (pin 17) is also provided by CO. The level on the CO line will reflect the 'Carry out' output from the 3002 Central Processing Element (CPE) at A21 or the 'shift right' output from the 3002 CPE at A23.

The 'clock' input (CLK) to the 3001 device (pin 19) is supplied by CLK1/ (pin P2-3) which is one of the two clock pulses generated on the Interface Board (see Chapter 4).

The load input (LD) to the 3001 (pin 36) is fed by the master reset (MR) signal from the Interface Board (pin P2-56).

Recall from Chapter 2, that the CPU specifies channel operations for the Diskette System by executing one of the seven channel commands. A channel command may be the result of either an input or output instruction to a dedicated I/O port address on the Channel Board:

- ) Write MA Lower (output to 'BASE+1')
- Write MA Upper and start I/O (output to 'BASE+2')
- 3) Stop Diskette Operation (output to 'BASE+3')
- 4) Reset Channel (output to 'BASE+7')
- 5) Read Subsystem Status (input to 'BASE+0')
- Read Result Type (input to 'BASE+1')
- Read Result Byte (input to 'BASE+3')

The three least significant bits (ADR0/ – ADR2/) of the 8-bit I/O address (received at pins P1-51 through P1-58) differentiate between the various input or output channel commands. The five most significant address bits (ADR3/ ADR7/) select the Channel Board if they match the BASE address that is assigned by setting five positions of switch S1. These five switch positions each feed one input on five EXCLUSIVE–OR gates. If ADR3/ – ADR7/ match the switch-selected BASE address, the 7410 NAND gate (A31-8) is activated and, in turn, enables one of the two 3205 decoders.

If an input channel command is being received, the RD CMD line (pin P2-60) will be true, and the 3205 decoder at A20 will be enabled. Address bits ADR0 – ADR2 (once inverted) are applied to the three data inputs on the 3205 section (A0 – A2), and activate one of three inverted outputs ( $\overline{O}_0$ ,  $\overline{O}_1$  or  $\overline{O}_3$ ), depending on the channel command. If it is 'read subsystem status' command, output 0 goes true and READ INT/ is asserted at pin P2-57. (On the Interface Board, READ INT/ is used to gate the device Ø and device 1 ready indicators onto system data bus lines Ø and 1, DATØ/ and DAT1/.) The low level on READ INT/ also enables two 8093 circuits, one of which transmits the output of the interrupt latch (INT/) to the data bit 2 line (DAT2/) of the system data bus. The other 8093 circuit transmits a low-level to the data bit 3 line (DAT3/), indicating that the diskette controller is present. INT/ is also passed to the Interface Board via pin P2-40.

If a 'read result type' command is being received, output 1 from the decoder goes true, and the RD RI/ signal is generated (pin P2-37). The low level on RD RI/ pre-sets the interrupt latch (A37-10), thus removing the active-low system interrupt request (INT/).

The interrupt latch can subsequently be clocked reset (i.e., reset to the active-low state) by a pulse on the CLK line, when the central processing element block (Section 3.2.4) determines that an 'I/O complete' or 'ready status change' interrupt should be issued (also refer to Chapter 2).

If a 'read result byte' command is being received, output 3 from the decoder will go true, and the 74175 quad latches are clocked, latching up address bits ADR0 – ADR2. The three most significant quad latch outputs are made available to the micro control unit block (Section 3.2.2), which responds to this command via a routine stored in microprogram memory. Either read result command will generate the RD RES/ signal which is used by the data flow control block (Section 3.2.6) to gate the appropriate status word onto the system data bus.

If an output channel command is being received, the WRT CMD line (pin P2-53) will be true, and the other 3205 decoder will be enabled. Address bits ADR0 – ADR2 are applied to inputs A0 – A2, causing one of the eight inverted decoder outputs to go true. If outputs 0, 1 or 2 go true, the WSUB1/ line (pin P2-48) is activated. If outputs 4, 5 or 6 from the decoder go true, the WSUB2/ line (pin P2-47) is activated. Either WSUB1/ or WSUB2/ will cause the 74175 quad latches to be clocked and latch up address bits ADR0 – ADR2, just as a 'read result byte' command did. The three most significant outputs of the quad latches are made available to the micro control unit block which responds to the 'write MA lower', the 'write MA upper and start I/O' and the 'read result byte' channel commands, using routines stored in microprogram memory. The response mechanisms for the other channel commands are implemented in hardware, not microcode.

The four 'flag logic control' inputs (FC0 – FC3) to the 3001 device are provided by bits 17 and 18 of the current microinstruction. Bit 17 is applied to both FC0 (pin 15) and FC1 (pin 16) while bit 18 is applied to FC2 (pin 13) and FC3 (pin 12).

The 'enable' (EN) and 'enable row address' (ERA) inputs to the 3001 (pins 25 and 35, respectively) are held high.

Unless the active-low master reset (MR/) signal from the Interface Board is true (low), the 'secondary instruction bus' inputs (SX0 - SX3) to the 3001 device (pins 10, 8, 6 and 5, respectively) will reflect the complement of the level on the four least significant memory address outputs (MA0 - MA3). That is, SX0 = MA0, SX1 = MA1, SX2 = MA2 and SX3 = MA3 if MR/ is false (high). If MR/ is true (low), the four SXn inputs will all be high, regardless of the state of the MAn outputs.

The four 'primary instruction bus' inputs (PX4 - PX7) to the 3001 device are fed by the four inverting outputs of the 8234 eight-to-four multiplexer (A5). The multiplexer outputs are controlled by the levels on the S0 and S1 inputs.

The A1, A2 and A3 inputs to the 8234 section are the three least significant data outputs from the central processing element (CPE) block that have been buffered and inverted; the A0 input is always high. After having fetched the diskette instruction byte from the I/O Parameter Block in system memory (see Section 2.3), the CPE block will output the three bits that specify one of the seven diskette operations onto its three least significant data outputs (D0 - D2).

e ine order veri Sine order veri	Select Lines	nto (1710) – 611 Materia Statel	AC0 Input At 3001 MCU
(Bit 14)	(Bit 15)	(Bit 16)	(Pin 39)
0	0	0	Bit 26 of current microinstruction (AC0)
0	0	1	CO: The carry out output from the 3002 CPE at A21 or the shift right output from the 3002 CPE at A23.
0	84 – 0 <b>1</b> end 88 8 Gi thelege ser 84 972.0 – 070 1005.8052.89	0	BUSY START: Indicates that a 'write MA lower', 'write MA upper' or 'read result byte' channel command has been received.
0	.1 .1 .1	CARL (or dation in Interview of the of the context of the of the	F (pin P2-58): Indicates that data/clock shift registers are full during read or empty during write.
1	0	0	AZ (pin P2-41): Indicates a valid CRC check (all zeros).
1	0	1	INDEX (pin P2-42): Indicates that an index mark has been detected (i.e., the beginning of a track).
1 sela as ess abov atriation shianno	ng vi namen 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	0	XFER REQ (pin P2-39): Indicates that Interface Board has requested use of the INTELLEQ MDS system bus.
1 18 19	konst Angle sidsi Hostori konseksi	a condi sicolo ste ortofic filico	TIMEOUT (pin P2-38): Ten millisecond pulse that is used by the microprogram for general timeouts.

Table 3-1 ACO INPUT SELECTION

H.a. Same database operation's committed is bailed invested compared 3 trace due competer next true, car is a set in SET aTOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization lowers light interval on SET 3TOP line (per P3/91). The scientization line (per P3/91) line (per P3/91).



Figure 3-2 3001 MICROPROGRAM CONTROL UNIT: FUNCTIONAL BLOCK DIAGRAM

2) Driving the input multiplexers to the 3002 Central Processing Element (CPE) array. Four fields (data shift register, clock shift register, errors and status) are multiplexed through 8234 and 8233 multiplexer devices (see sheet 4 of the schematic) and into the I-bus inputs of the CPE array. The selection bits for the multiplexers are provided by the mask field bits, as listed in Table 3-4.

MICROINSTRUCTION BIT	SIGNAL	DEFINITION	PROM LOCATION - PIN
01 02 03	MASKO (MO) MASK1 (M1) MASK2 (M2)	10	A13- 9 A13-10 A12-11
04	MASK2 (M2) MASK3 (M3)	Mask field	A13-11 A13-13
05	MASK4 (M4) MASK5 (M5)	10	A13-14 A13-15
07 08	MASK6 (M6) MASK7 (M7)		A13-16 A13-17
09	SLK0 (S0)	K-bus select	A12- 9
11	OUTO	Deceder output	A12-10 A12-11
12 13	OUT1 OUT2	select	A12-13 A12-14
14	INO		A12-15
15 16	IN1 IN2	AC0 Select	A12-16 A12-17
*17	FC0	or which listochics off, share	A11- 9
*17 *18	FC1 FC2	Flag control	A11- 9 A11-10
*18	FC3	and the second	A11-10
19 20	F0 F1		A11-11 A11-13
21	F2	na natur gana yang sangangan Ni na galahin kataning mili	A11-14
22	F3 F4	Function field	A11-15
24	F5		A11-10 A11-17
25	F6	and the second second second	A10- 9
20	ACI		A10-10 A10-11
28	AC2		A10-13
29 30	AC3 AC4	Address control	A10-14 A10-15
31	AC5		A10-16

### TABLE 3-2 MICROINSTRUCTION BIT ASSIGNMENTS

When the determed office study representent any prophy that good process both the least transon the study loaded with full presention that we like any shifted one to the instance of and their to the distance. Used to generate PEI-read WHT & P -represe At this time, the mask and output bits of the current microinstruction being output from the microprogram memory block (see Section 3.2.3) will produce a high level on the S0 input to the 8234 section and a low level on the S1 input, multiplexing the inverted levels of the 8234's A inputs (specifying a particular diskette operation) into the PX4 – PX7 inputs on the 3001 MCU. This allows the 3001 MCU to subsequently access those microinstructions which will effect the appropriate diskette operation.

The B1, B2 and B3 inputs to the 8234 multiplexer are the three least significant system address bits that were buffered and inverted in the channel command block (see Section 3.2.1); the B0 input is always held low. Recall that these three address bits specify one of the seven channel commands. At this time, the mask and output bits of the current microinstruction being output from the microprogram memory block (see Section 3.2.3) will produce a low level on the S0 input to the 8234 section, multiplexing the inverted levels of the 8234's B inputs (specifying a particular channel command) into the PX4 – PX7 inputs on the 3001 MCU. This allows the 3001 MCU to subsequently access those microinstructions which will produce the proper Diskette System response to the channel command received.

The MCU outputs the 9-bit address of the next microinstruction to be fetched on MA0 – MA8. MA0 – MA8 are applied to the nine address inputs on each of the 3604 PROM's that constitute the microprogram memory (see Section 3.2.3).

### 3.2.3 Microprogram Memory Block

The microprogram memory block stores the microinstructions which direct the operation of the diskette controller. The microprogram memory block consists of four 3604 programmable-read-only-memory devices (512 x 8 bits each), which store 32 bit microinstructions; a 3205 three-to-eight decoder, which generates eight timing control pulses (DEC OUT0 – DEC OUT7) based on bits 11, 12 and 13 (OUT0 – OUT2) of the current microinstruction; and a 3404 six-bit high speed latch, which provides various control signal levels based on the decoder outputs mentioned above and the mask bit field of the current microinstruction; as shown on sheet 3 of the board schematic (Section 3.3).

The 9-bit memory address (MA0 - MA8) for the four 3604 PROM's is provided by the 3001 Microprogram Control Unit. MA0 - MA8 cause the addressed microinstruction to appear on the 32 output lines from the four PROM's.

Table 3-2 summarizes bit definitions for the 32-bit microinstructions. The address control bits, ACO - AC6 (bits 26–32), the flag control bits (bits 17 and 18), and the input control bits used for ACO select (bits 14–16) are fed to the micro control unit block as described in Section 3.2.2. The function field bits, FO - F6 (bits 19–25), the mask bits MO - M7 (bits 1–8) and the K-bus select bits SO and S1 (bits 9–10) are applied to the central processing element (CPE) block, as described in Section 3.2.4. The output bits OUTO – OUT2 (bits 11–13) are applied to the three address inputs on a 3205 decoder. The enable inputs to this 3205 section are provided by the CLK2/ pulse from the Interface Board (pin P2–30), the seventh mask bit M7 (bit 8 of the current microinstruction) and S0, one of the two K-bus select bits mentioned above (bit 9 of the current microinstruction). The eight decoder outputs, DEC OUTO – DEC OUT7, provide timing control pulses that, when used with the mask bits, provide overall control for the diskette controller (see Table 3–3).

The mask field bits MO - M7 (bits 1-8 of the current microinstruction) are actually used for three disjoint functions in the Diskette System:

1) Generating control signals for the hardware. These control signals are pulses (positive or negative and of 50-75 nsec. duration) or levels. The pulses are generated by gating the appropriate mask bit with one of the 3205 decoder outputs (DEC OUTn). The levels are derived by using the DEC OUTn outputs to strobe 3404 six-bit latches. The DEC OUTn outputs provide the write enable strobes to the 3404 latches, while the mask bits provide the data inputs and, consequently, the actual controls. Refer to Table 3-3 for a summary of the control pulses and levels generated by the DEC OUTn strobes and mask field bits.

		CONTROL FUNCTION DEFINITIONS (CONTINUED)
SROUT	-	This level enables data bits from data register (when high) or from 9401 CRC device (when low) to be sent to the selected diskette.
LDADM	-	This level is used to load clock shift register with the bit patterns required to write the different address marks onto a diskette.
CRCMD	an es	This level indicates the operating mode for the 9401 CRC device on the Interface Board.
DIREC	-	This level indicates the direction of head movement for the selected diskette drive.
AMWRT	-	This level enables writing of an extra clock pulse and is activated during writing of an address mark.
LOWEN	1.60	This level drives the GATE LOWER line that enables data onto the memory data inputs $(MO/ - M7/)$ to the CPE array.
MEMWT	-	This level indicates when the Diskette System wishes to write data to memory.
SMREQ	-	This pulse initiates the bus request sequence intended to gain master control of the INTELLEC MDS system bus.
STBDU	-	This pulse loads CPE data outputs (D0 $-$ D7) into the latch which drives the system data lines, DATA8/ $-$ DATAF/.
STBDL	-	This pulse loads CPE data outputs (D0 $-$ D7) into the latch which drives the system data bus lines, DATA0/ $-$ DATA7/.
LDADD	-	This pulse loads CPE data outputs (D0 $-$ D7) into the latch which drives the system address bus lines, ADR0/ $-$ ARD7/.
SINTR	-	This pulse is used to generate a signal which clocks the interrupt latch on the Channel Board.
CINBS	o.av s ,j <del>≒</del> ,ł	This pulse is used to latch data from the system data bus into the latches which drive $M\emptyset - M7/$ of the CPE array.
CSYNC	-	This pulse initializes the synchronization logic prior to detecting an address mark.
RSAMD	- And	This pulse resets the synchronization logic prior to initializing the logic with the CSYNC pulse.
UNLHD	- 675 - 67 - 1881	This pulse clears the LOAD latch on the Interface Board, and ultimately causes the read/ write head on the selected drive to be unloaded.
RSTST	-	This pulse is used to generate CLR START STOP signal which resets the STOP latch and the 74145 latch at A8–1 on the Channel Board.
RNDX	17. 17. 19.	This pulse resets the INDEX latch on the Interface Board.
LDOPC		This pulse latches diskette operation code (D0–D5) and makes latched code available to 'primary instruction bus' multiplexer.

# TABLE 3-3 (CONTINUED)

# TABLE 3–3 CONTROL PULSES AND LEVELS GENERATED BY MICROPROGRAM

OUT CODE (DEC OUT n) MASK BIT	000 (0)	001 (1)	010 (2)	011 (3)	100 (4)	101 (5)	110 (6)	111 (7)
мо	CSTEP		NSUB0			AMWRT	SMREQ	CSYNC
M1	SSCLK	RDYRS	NSUB1	No an A TRA IC	601 14 3.1	WFLRS	STBDU	RSAMD
M2	LDHD			LDNXM		1.2	STBDL	UNLHD
M3	2017 I 5108	RINH	ONTINE ROLD		SIGMAL	LOWEN	LDADD	RSTST
M4	55A 51A	SINH		WTGTN	(0%) (0) (194) -12	MEMWT	GTR43	NGT43
M5		SACK	tites fight	SR OUT	CRC MD	e Ada	SINTR	RNDX
M6		RDOR		LDADM	DIREC	CAN CAU SAU	CINBS	LDOPC
	1			-	(34) 12	DAME		

		CONTROL FUNCTION DEFINITIONS	
CSTEP		This pulse triggers the one-shot which drives the STEP/ line to the diskette drives. STEP/ causes the selected drive to move its head one track.	
SSCLK		This pulse triggers the TIMEOUT one-shot. TIMEOUT provides a 10 msec. pulse for use by the microprogram.	
LDHD	11-5 11-6 12-4	This pulse sets the LOAD latch on the Interface Board which causes the read/write head on the selected unit to be loaded.	
RINH	- 번 A · · · · · · · · · · · · · · · · · ·	This pulse resets the inhibit memory write latch (A48–1).	
SINH	<u>8</u>	This pulse sets the inhibit memory write latch (A48–4).	
SACK		This pulse sets the transfer acknowledge (XACK/) latch on the Interface Board.	
RDOR	9 <del>1</del> .).	This pulse resets the data overrun latch on the Interface Board.	
NSUB0 and	d NSUB1	<ul> <li>These levels select 'primary instruction bus' inputs to 3001 MCU.</li> </ul>	
LDNXM	-	This level is used to load the clock shift register with the bit patterns required to write the different address marks onto a diskette.	
WTGTN	-	When the data and clock shift registers are empty, this level allows both shift register be parallel loaded with information that will be serially shifted out to the Interface I and then to the diskette. Used to generate PE/ and WRT GT/ signals.	rs to Board

An Intel 3002 Central Processing Element contains all of the circuits that represent a 2-bit wide slice through the data processing section of a digital computer. When wired together in an array, a set of CPE's provide the following capabilities:

- Two's complement arithmetic
- Logical AND, OR, NOT and EXCLUSIVE—OR
- Incrementing and decrementing
- Shifting left or right
- Bit testing and zero detection
- Carry look-ahead generation
- Multiple data and address busses

A functional block diagram of a 3002 CPE is shown in Figure 3-3.

K-BUS SEL	ECT LINES		k	-BUS II	NPUTS T	0 3002	CPE ARI	YAF	
S1 (Bit 10)	S0 (Bit 9)	КО	К1	К2	КЗ	K4	К5	К6	К7
0	0	MO	M1	M2	M3	M4	M5	M6	M7
0	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0

#### TABLE 3-5 K-BUS INPUT SELECTION

Note that only when S0 and S1 equal zero will the K-bus inputs be supplied by the mask bits; otherwise, the K-bus inputs will be all ones or all zeros.

During each micro-cycle, the function field of the current microinstruction is applied to the F-bus inputs (F0 - F6) of each 3002 CPE. The function bits are decoded, the operands are selected by the internal multiplexers, and the specified operation is performed. Within each CPE, data is stored in eleven scratchpad registers or the accumulator.

Data being output from the CPE array is carried on the address bus (A0 - A7) or the data out bus (D0 - D7). The address outputs drive the eight most significant lines of the INTELLEC System address bus, ADR8 – ADRF. The data outputs are made available to the data flow control block (Section 3.2.6) and the micro control unit block (Section 3.2.2).

Data is brought into the CPE array on three separate input buses, the memory data bus (M0 - M7), the I-bus (I0 - I7) and the K-bus (K0 - K7). The memory data inputs are supplied by the data flow control block (Section 3.2.6) which routes data from the system data bus to the CPE array. The latter two buses are driven by five multiplexers.

The K-bus inputs (K0 - K7) are driven by two 8234 eight-to-four multiplexers (located at A33 and A26). The S0 and S1 outputs from the microprogram memory (bits 9 and 10 of the current microinstruction) determine the four outputs on each of the two 8234 sections. If S0 = 1 and S1 = 0, all eight inverted outputs will be low. If S0 = 1 and S1 = 1,

An hais 2001 Cannel Procession Element germins of Grandmain Fost moneter of the test of the second of the form of the fold processing externed a **Signal Compare**s. What would applied to an answer of the COS of the Low Processing would be addressed.



Figure 3-3 3002 CENTRAL PROCESSING ELEMENT: FUNCTIONAL BLOCK DIAGRAM

all eight outputs will be high. If S0 = 0, however, the eight mask bits, MO - M7, from the microprogram memory (bits 01 - 08 of the current microinstruction) will be inverted and applied to the K-bus inputs of the CPE array (see Table 3-5).

The I-bus inputs (10 - 17) are driven by two 8234 (inverting outputs) and one 8233 (non-inverting outputs) eight-tofour multiplexers (located at A28, A45 and A35). Mask bits M3 - M7 from the microprogram memory (bits 04 - 08 of the current microinstruction) determine the I-bus inputs as listed in Table 3-4 of Section 3.2.3. These mask bits will enable the eight outputs from the two 4-bit data shift registers (at A36 and A29), or the eight outputs from the two clock shift registers (at A34 and A27) through the 8233 section and one of the 8234 sections and into the 10 - 17inputs on the CPE array. The mask bits can also enable the four error lines (DOR, WRT PROT, WRT ERR and SEL DR NRDY) or the four status lines (DR0, DR1, STOP and TRACK 00) from the Interface Board (see Chapter 4) through the other 8234 section (at A45) and into the 14 - 17 inputs on the CPE array.

The clock input to the 3002 CPE's is provided by the CLK1/ pulse generated on the Interface Board. The enable address inputs (EA), which enable the address outputs (A0 – A7), are fed by the SELECTED line from the Interface Board (pin P2–43). When true, SELECTED indicates that the diskette controller has master control of the INTELLEC MDS bus (see Chapter 4). The enable data input (ED) to each 3002 CPE is permanently held low (active).

The carry output (CO) from each 3002 CPE feeds the carry input (CI) of the adjacent 3002 CPE. Likewise, the shift right output (RO) feeds the shift right input (LI) of the adjacent 3002 CPE. The carry output (CO) from the most significant CPE (A21-7) feeds its own shift right input (LI) and is wire-ORed with the shift right output (RO) from the least significant CPE (A23-8) to form the CO line, which is applied to the flag control input (FI) on the 3001 Microprogram Control Unit. CO is also inverted and applied to the D1 input on the 74151 multiplexer (A30-3) which provides the least significant address control bit, ACO, to the 3001 MCU. The carry input (CI) to the least significant 3002 CPE (A23-10) is provided by the flag control output (FO) from the 3001 MCU.

#### 3.2.5 Data/Clock Shift Register Block

During read operations, the data/clock shift register (SR) block accepts serial data and clock bits that the Interface Board has received from the selected diskette drive and converts them into eight bit bytes that are input, in parallel, to the CPE array. During write operations, the shift registers are parallel loaded with data and clock bytes which are then shifted out to the Interface Board. This block includes four 9300 four-bit shift registers, as shown on sheet 4 of the board schematic (see Section 3.3).

Recall from Section 1.2 that data and clock bits are interspersed when information is written on disk. When that information is later read, the diskette drive separates the data and clock pulses before passing them to the Interface Board (see Chapter 4).

The Interface Board, in turn, sends the data bits to the Channel Board via the SR DATA IN/ line (pin P2-22) along with the data strobe SR DATA STB (pin P2 – 24). SR DATA IN/ feeds the J and  $\overline{K}$  inputs on the first data shift register at A36. The Q3 output from this first shift register then feeds the J and  $\overline{K}$  inputs on the shift register at A29. When the data shift registers are full, the eight data bits are transferred in parallel to the CPE array. The four outputs from the first data shift register (A36) are applied to the 'A' inputs on the 8233 multiplexer that feeds the four least significant I-bus inputs to the CPE array. The first two outputs are also made available to the Interface Board via the ID0/ (pin P2-26) and ID1/ (pin P2-23) lines (see Chapter 4). The four outputs from the second data shift register (A29) are applied to the 8234 multiplexer (A28) that feeds the four most significant bits of the I-bus inputs to the CPE array. Both data shift registers are clocked by SR DATA STB.

During write operations, both data shift registers can be parallel loaded when the PE/ input is low. PE/ will go low when the shift register is empty and the WTGTN signal is true (see Table 3-3).

The parallel inputs to the first data shift register (A36) are supplied by the four least significant data outputs from the CPE array, as follows:

D0	>	PO
D1	>	P1
D2	>	P2
D3	$\longrightarrow$	P3

The parallel inputs to the second data shift register (A29) are supplied by the four most significant CPE array data outputs:

D4		->	PO
D5	_	->	P1
D6		->	P2
D7		->	P3

The data bits can then be shifted out, in serial, to the Interface Board via the SR DATA OUT line (pin P2-25) which is driven by the  $\overline{O3}$  output on the second data shift register.

During read operations, the Interface Board sends the clock bits (that were interleaved with the data bits on the diskette) to the Channel Board via the SR CLK IN/ line (pin P2–6) along with the clock strobe, CLK SR STB (pin P2–8). SR CLK IN/ feeds the J and  $\overline{K}$  inputs on the first clock shift register at A34. The Q3 output of this first clock shift register then feeds the J and  $\overline{K}$  inputs on the shift register at A27. When the clock shift registers are full, the eight clock bits can be transferred in parallel to the CPE array. The four outputs from the first clock shift register that feeds the J' inputs on the 8233 multiplexer that feeds the four least significant bits of the I-bus to the CPE array. The four outputs from the second clock shift register (A27) are applied to the 8234 multiplexer that feeds the four most significant bits of the I-bus. Both clock shift registers are clocked by CLK SR STB.

During write operations, both clock shift registers can be parallel loaded when the PE/ signal (described above) is low. The P0, P1 and P2 inputs to the first clock shift register and the P2 and P3 inputs to the second clock shift register are tied to ground. The P3 input to the first shift register and the P1 input to the second are both fed by the output of a 7408 AND gate (A7–6) shown on sheet 3 of the schematic. The inputs to this gate are the LDNXM and LDADM control levels which have been set in the 3404 latches at A16 by the microprogram (refer to Table 3–3). The P0 input to the second clock shift register is fed by the LDADM control output. LDNXM and LDADM allow the microprogram to produce the varied patterns of clock bits that are required to write the different types of address marks onto a diskette (refer to Section 1.2).

### 3.2.6 Data Flow Control Block

The data flow control block routes data to/from the various other functional blocks within the Channel Board. This block consists of five 8212 bi-directional latching bus drivers, a 3404 six-bit latch and various gating circuits, as shown on sheet 2 of the board schematic (Section 3.3).

The six least significant data outputs (D0 - D5) from the CPE array are applied to the inputs of the 3404 six-bit latch. When the microprogram generates the LDOPC control pulse (see Table 3-3), D0 - D5 are latched and inverted.  $\overline{D0} - \overline{D2}$  are made available to the 'primary instruction bus' multiplexer (A5) in the MCU block.  $\overline{D3}$  is used for 16-bit data flow control as described below.  $\overline{D4}$  and  $\overline{D5}$  are sent to the Interface Board as the unit select signals, USA (pin P2-9) and USB (pin P2-12), respectively.

All eight CPE data outputs, D0 - D7, are also applied to three of the 8212 latching bus drivers. D0 - D7 are loaded into the 8212 device at A41 when the microprogram generates the LDADD control pulse (see Table 3-3). The 8212

device at A41 drives the eight least significant lines of the system address bus,  $ADR\emptyset/ - ADR7/$ . When the microprogram generates the STBDL control pulse (see Table 3-3),  $D\emptyset - D7$  are latched into the 8212 device at A43 which drives the eight least significant lines of the system data bus,  $DAT\emptyset/ - DAT7/$  (pins P1 - 67 through P1 - 74). STBDL is generated when the microprogram is setting a result word or preparing write data. When the microprogram generates the STBDU control pulse (see Table 3-3),  $D\emptyset - D7$  are latched into the 8212 device at 42, which drives the eight most significant system data bus lines, DAT8/ - DATF/ pins P1 - 59 through P1 - 66). STBDU would only be generated if the Diskette System were operating in the 16 bit mode. The address latch (A41) is gated onto the MDS system bus whenever the SELECTED signal is true. The high-order data latch (A42) is gated onto the bus whenever the SELECTED, MEMORY WRITE and 16-BIT MODE signals are true. The low-order data latch (A43) is gated onto the bus during memory write operations or 'read result' operations.

When a master bus module in the INTELLEC System outputs data to the diskette controller, the data from lines DATD/ - DATT/ is applied to the 8212 bus driver at A25. DAT8/ - DATF/ is applied to the 8212 at A24. The data on those lines are strobed into the input latches at A24 and A25 by the microprogram control pulse CINBS (see Table 3-3). 'Slave' memory modules also drive the data lines, DATD/ - DATT/ and possibly DAT8/ - DATF/. Memory data are strobed into the latches when the STB MEM IN signal is generated by the Interface Board. The outputs from the devices at A24 and A25 are 'OR-ed' into lines MD/ - MT/. Depending on the state of the GATE LOWER signal, data from only one of the two latches will actually be gated onto the M input lines (MD/ - MT/) to the CPE array.

### 3.3 SCHEMATICS/PIN LISTS: CHANNEL BOARD

The schematic drawing (4 sheets) for the Channel Board is provided in Figure 3-4. These schematics are subject to change without notice. The Reference Schematic Drawings shipped with the Diskette System should be used as a reference.

Table 3-6 lists the pins and designated signal functions for the 86-pin P1 bus connector. Table 3-7 lists the same information for the 60-pin P2 controller connector.

PIN	SIGNAL	FUNCTION	
1	•	ADROV	
2			
3			
1			
4			
5			
6			
7			
8	NO CONNECTION		
9			
10			
11			
12			
13			
14	West Structure Systems		
15	2.01+6380		
16			
17			
10			
10	*		

### TABLE 3-6 PIN LIST: P1 BUS CONNECTOR

# TABLE 3-6 PIN LIST: P1 BUS CONNECTOR (CONTINUED)

19       A         21       A         23       A         24       B         25       B         26       B         27       B         28       B         29       NO CONNECTION         31       B         32       B         33       ADRE/         43       ADRE/         44       ADRE/         45       ADRC/         46       ADRB/         47       ADRB/         48       ADRB/         49       ADRB/         51       ADR6/         48       ADR8/         52       ADR1/         54       ADR2/         55       ADR3/         56       ADR3/         57       ADR0/         58       ADR1/         69       DATAE/         61       DATAE/         62       DATAB/         63       DATAB/         64       DATAB/         65       DATAB/         66       DATAB/         67       DATAB/         68	PIN	SIGNAL	FUNCTION
20       NO CONNECTION         21       NO CONNECTION         22       ADR/         23       ADRE/         24       ADRE/         25       ADRE/         26       ADRE/         27       ADRE/         28       ADRE/         29       ADRE/         41       ADRE/         42       ADRE/         43       ADRE/         44       ADRE/         45       ADRE/         46       ADRE/         47       ADRA/         48       ADRE/         51       ADRE/         52       ADRA/         53       ADRA/         54       ADRE/         55       ADR2/         56       ADR3/         57       ADR3/         58       ADR3/         57       ADR3/         58       ADR3/         59       DATAE/         60       DATAE/         61       DATAE/         62       DATAE/         63       DATAE/         64       DATAB/         65       DATA	19		Comparison of the second se
21	20		and the second se
23	21		
23	22		and the second residence of the second se
24       NO CONNECTION         30       NO CONNECTION         31	23	and the second	The state of the s
26       27         28       NO CONNECTION         31       33         32       33         33       34         34       35         35       36         37       38         39       44         41       42         42       44         44       ADRE/         45       ADRC/         46       ADRA/         48       ADRB/         49       ADRB/         50       ADRB/         51       ADR6/         33       ADRF/         44       ADRE/         45       ADRA/         48       ADRB/         50       ADRB/         51       ADR6/         52       ADR1/         53       ADR1/         54       ADR6/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         61       DATAE/         62       DATAA/         63       DATAA/         64<	24	Provide the second set and set there it's	the THEFT AND A COM VERMENT AND THE ARE NOT THE AND
27       28       NO CONNECTION         31	25	and firsters "fight	and it onto the time during waves with a perceiver of the
28	20		
29         NO CONNECTION           31	28	and state of the end work work and the state of a state	When a minute our module in the HATELLEC System outputs
30         NO CONNECTION           31	29	The - BATE, a sequely to the drift of a STAR - THE	DATE/ - DATE/ is studied to the 8212 lise (rover at A25, 621
31         32         33         34         35         36         37         38         39         40         41         42         43         ADRE/         44         ADRE/         45         ADRC/         46         ADRB/         47         ADRB/         48         ADRB/         49         ADR6/         address bus         51         ADR6/         address bus         52         ADR1/         54         ADR5/         55         ADR1/         54         ADR1/         55         ADR1/         56         ADR1/         57         ADR0/         58         ADR1/         59         DATAE/         61         DATAE/         62         DATAA/         64	30	NO CONNECTION	constructions have an attended one of a input tradition of A24, walled
32       33         34         35         36         37         38         39         40         41         42         43         ADRE/         44         ADRF/         45         ADRA/         46         ADRA/         47         ADRA/         48         ADRB/         50       ADR9/         ADR6/         48         ADR6/         49         ADR6/         44         ADRA/         45         ADRA/         46         ADRA/         47         ADRA/         48         ADRA/         51       ADR6/         32       ADR1/         54       ADR3/         55       ADR3/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         61       DATAA/         62 </th <th>31</th> <th>N BOTT ARE SHEET ARE NOT ARE TARE -</th> <th>SERVICE Management with a state of the service street finance, ISAN and</th>	31	N BOTT ARE SHEET ARE NOT ARE TARE -	SERVICE Management with a state of the service street finance, ISAN and
33       34         35       36         36       37         37       38         38       39         40       41         42	32	and the the lotter and the lotter is the set of the	reaction of MBM B12 and Males accurate of a bedattle me
34       36         36       37         37       38         39       40         40       41         42	33	milling on the state of the GAR's of the second	Antipits at \$24 pild A25 are '03-ed' into inter M6/ - 87/ -0 pe
35       36         37       38         39       40         40       40         41       41         42	34	· · · · · · · · · · · · · · · · · · ·	of many parest ad Alicotas Iline successful and with an easy first draw
36	35		and consistence of the constant of the second
37         38         39         40         41         42         43       ADRE/         44       ADRF/         45       ADRC/         46       ADRD/         47       ADRA/         48       ADR8/         50       ADR9/         51       ADR6/         35       ADR4/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAA/         62       DATAF/         63       DATAF/         64       DATAF/         65       DATAF/         66       DATAF/         67       DATAF/         68       DATAF/         66       DATAF/         67       DATAF/         68       DATAF/	36		CARACIO TRADAMENT SCIENT IN AUGUST MUSICAS - 2-2-1
38	37		The enterestic streament is stream in the Channel Report in the
33       ADRE/         41       ADRE/         42       ADRE/         44       ADRF/         45       ADRC/         46       ADRA/         48       ADRB/         49       ADR8/         50       ADR9/         51       ADR6/         33       ADR1/         52       ADR7/         53       ADR4/         54       ADR5/         55       ADR1/         56       ADR3/         57       ADR0/         58       ADR1/         60       DATAE/         61       DATAE/         62       DATAA/         64       DATAB/         65       DATAA/         66       DATAB/         67       DATAA/         68       DATAB/	38	the second	The monthly and a second the Strength of the second to be and
40       41         42       43         43       ADRE/         44       ADRF/         45       ADRC/         46       ADRD/         47       ADRA/         48       ADRB/         49       ADRB/         50       ADR6/         51       ADR6/         52       ADR1/         53       ADR2/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAA/         64       DATAA/         65       DATAB/         66       DATAB/         67       DATAB/         68       DATAB/         66       DATAB/         67       DATA6/	39		- Talanasi
42       ADRE/         43       ADRE/         44       ADRF/         45       ADRC/         46       ADRD/         47       ADRA/         48       ADRB/         49       ADR8/         50       ADR9/         51       ADR6/         52       ADR7/         53       ADR4/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAA/         64       DATAA/         65       DATAB/         66       DATAB/         67       DATA6/         68       DATA7/	40		
43         ADRE/           44         ADRF/           45         ADRC/           46         ADRD/           47         ADRA/           48         ADR8/           49         ADR8/           50         ADR8/           51         ADR6/           32         ADR7/           53         ADR4/           54         ADR5/           55         ADR3/           56         ADR3/           57         ADR0/           58         ADR1/           59         DATAE/           60         DATAE/           61         DATAC/           63         DATAB/           64         DATAB/           65         DATAB/           66         DATA9/           67         DATA6/	41	State of the second car T in 37 rest and 74 nations	Tradit 3.6 Intradic side and disigneet signal to test for the 1
44       ADRF/         45       ADRC/         46       ADRD/         47       ADRA/         48       ADRB/         49       ADR8/         50       ADR9/         51       ADR6/         33       ADR4/         54       ADR5/         55       ADR7/         56       ADR3/         57       ADR6/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAA/         63       DATAA/         64       DATAB/         65       DATAB/         66       DATAB/         67       DATAB/         68       DATAA/	43	ADRE/	HILLION D.Y. THE EXTERNET OF CONDUCTION CONCERNEY.
45       ADRC/         46       ADRD/         47       ADRA/         48       ADRB/         49       ADR8/         50       ADR9/         51       ADR6/         33       ADR4/         54       ADR5/         55       ADR7/         56       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAE/         61       DATAC/         62       DATAA/         64       DATAA/         65       DATAA/         66       DATAA/         67       DATA8/       INTELLEC System         66       DATAA/         67       DATAA/	44	ADRF/	
46       ADRD/         47       ADRA/         48       ADRB/         49       ADR8/         50       ADR6/         31       ADR6/         32       ADR1/         53       ADR2/         54       ADR6/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAA/         62       DATAA/         63       DATAA/         64       DATAB/         65       DATA8/         66       DATA9/         67       DATA6/         68       DATA7/	45	ADRC/	
47       ADRA/         48       ADRB/         49       ADR8/         50       ADR9/       INTELLEC System         51       ADR6/       address bus         52       ADR7/         53       ADR4/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAC//         62       DATAA/         64       DATAB/         65       DATAB/         66       DATA9/         67       DATA6/         68       DATA7/	46	ADRD/	
48       ADRB/         49       ADR8/         50       ADR9/       INTELLEC System         51       ADR6/       address bus         52       ADR7/	47	ADRA/	
49       ADR8/         50       ADR9/       INTELLEC System         51       ADR6/       address bus         52       ADR7/	48	ADRB/	The Frank Bac & Bact
50         ADR9/         INTELLEC System           51         ADR6/         address bus           52         ADR7/	49	ADR8/	
51       ADR6/       address bus         52       ADR7/         53       ADR4/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         60       DATAE/         61       DATAC/         62       DATAD/         63       DATAB/         64       DATAB/         65       DATA8/         66       DATA9/         67       DATA6/         68       DATA7/	50	ADR9/	INTELLEC System
52       ADR7//         53       ADR4/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAC/         62       DATAA/         63       DATAB/         65       DATA8/         66       DATA9/         67       DATA6/	51	ADR6/	address bus
53       ADR4/         54       ADR5/         55       ADR2/         56       ADR3/         57       ADR0/         58       ADR1/         59       DATAE/         60       DATAF/         61       DATAC/         62       DATAD/         63       DATAB/         64       DATAB/         65       DATA8/         66       DATA9/         67       DATA6/         68       DATA7/	52	ADR7/	
54     ADR3/       55     ADR3/       56     ADR3/       57     ADR0/       58     ADR1/       59     DATAE/       60     DATAF/       61     DATAC/       62     DATAD/       63     DATAA/       64     DATAB/       65     DATA8/       66     DATA9/       67     DATA6/       68     DATA7/	53	ADR4/	
56     ADR3/       57     ADR0/       58     ADR1/       59     DATAE/       60     DATAF/       61     DATAC/       62     DATAD/       63     DATAB/       64     DATA8/       65     DATA9/       66     DATA9/       67     DATA6/	54		
57     ADR0/       58     ADR1/       59     DATAE/       60     DATAF/       61     DATAC/       62     DATAD/       63     DATAA/       64     DATAB/       65     DATA8/       66     DATA9/       67     DATA6/       68     DATA7/	56	ADR3/	
58     ADR1/       59     DATAE/       60     DATAF/       61     DATAC/       62     DATAD/       63     DATAA/       64     DATAB/       65     DATA8/       66     DATA9/       67     DATA6/       68     DATA7/	57	ADR0/	
59         DATAE/           60         DATAF/           61         DATAC/           62         DATAD/           63         DATAA/           64         DATAB/           65         DATA8/           66         DATA9/           67         DATA6/           68         DATA7/	58	ADR1/	
60DATAF/61DATAC/62DATAD/63DATAA/64DATAB/65DATA8/66DATA9/67DATA6/68DATA7/	59	DATAE/	
61DATAC/62DATAD/63DATAA/64DATAB/65DATA8/66DATA9/67DATA6/68DATA7/	60	DATAF/	HER TOUGHNEE ON
62DATAD/63DATAA/64DATAB/65DATA8/66DATA9/67DATA6/68DATA7/	61	DATAC/	
63DATAA/64DATAB/65DATA8/66DATA9/67DATA6/68DATA7/	62	DATAD/	
64DATAB/65DATA8/66DATA9/67DATA6/68DATA7/	63	DATAA/	
65     DATA8/     INTELLEC System       66     DATA9/     data bus       67     DATA6/       68     DATA7/	64	DATAB/	
66         DATA9/         data bus           67         DATA6/	65	DATA8/	INTELLEC System
68 DATA6/ DATA7/	66	DATA9/	data bus
	67		
69 DATA/	60		52
70 DATA5/	70		

PIN	SIGNAL	FUNCTION	1.25
71	DATA2/	NO TUO SÃO	
72	DATA3/	INTELLEC System	
73	DATA0/	data bus	
74	DATA1/	DATA OF STO	
75	Seven data and JAc	SR BATA ODT	
76	fi set ship muri	100i	
77	Contract de socier 5 outraux	LE TUD SED	
78	Cauters Geauter & autour	DEC OUT U	
79	NO CONNECTION	ALL MODE STR	
80	NO CONNECTION	CENCE /	
81	Sugartish States and and the second	58 F \$3099	
82	transformer officeroor writedate	BiitAitB	
83	Castrot decides purpue 7	0.00 T YOU 7	
84	E sta to M	NK3	
85	Control decider support of	1 700 230	
86	Mesk, Ser. ij	3.946	

## TABLE 3-6 PIN LIST: P1 BUS CONNECTOR (CONTINUED)

# Criticatolica requests MDS was interned the All cards, valid CRC shock State and detected Cardenius has can hold at 509

3

20

## TABLE 3-7 PIN LIST: P2 CONTROLLER CONNECTOR

PIN	SIGNAL	FUNCTION
1	\$ 140 A2075	\$3M
2	MK4	Mask bit 4
3	CLK1/	Diskette controller clock 1
4	MK1	Mask bit 1
5	B rid skille	extra
6	SR CLK IN 1	Serial clock input line
7		-
8	CLK SR STB	Serial clock strobe
9	USA	Unit select bit A
10	SR CLK OUT	Serial clock out line
11	TRACK 00/	Track 00 detected
12	USB	Unit select bit B
13	MKØ	Mask bit 0
14	DSK WRT PROT/	Disk write protected
15	DRO/	Drive 0 ready
16	DOR/	Data overrun error
17	DR1/	Drive 1 ready
18	WRT ERR/	Write error
19	SR OUT	Write data multiplexer control level
20	SEL DR NRDY/	Selected drive not ready

# PIN LIST: P2 CONTROLLER CONNECTOR (CONTINUED)

PIN	SIGNAL	FUNCTION
21	DEC OUT 0/	Control decoder output 0
22	SR DATA IN/	Serial data in line
23	ID1/	Input data bit 1
24	DATA SR STB	Serial data strobe
25	SR DATA OUT	Serial data out line
26	1D0/	Input data bit 0
27	DEC OUT 5/	Control decoder 5 output
28	DEC OUT 4/	Control decoder 4 output
29	STB MEM IN	Strobe memory data in
30	CLK2/	Diskette controller clock 2
31	SET STOP/	Stop diskette' abappal command
32	ENABLE	Diskette controller addressed
22		Control decoder output 7
24	DEC OUT /	Made bit 2
34		
35	DEC OUT 6	Control decoder output 6
30	MK6	Mask bit 6
3/	RD RI/	'Read result type' channel command
38	TIME OUT	10 msec. timing pulse
39	XFER REQ/	Controller requests MDS bus
40	INT/	Interrupt line
41	AZ	All zeros, valid CRC check
42	INDEX	Index mark detected
43	SELECTED	Controller has control of MDS bus
44	GATE LOWER	Input low-order data byte
45	BUSY START	Microprogram responding to channel command
46	MR/	Master reset
47	WSUB2/	Not used at present
48	WSUB1/	Not used at present
49	RESET/	'Reset' channel command
50	MK2	Mask bit 2
51	MEM WRT	Write data to MDS memory
52	DEC OUT 1/	Control decoder output 1
53	WRT CMD	I/O write command
54	MK5	Mask bit 5
55	WBT GT	Write gate control level
56	MB	Master reset
57		'Read subsystem status' command
58	F	Shift registers are full or empty
50	A tel toules truly	Shift registers are full of empty
60	PD CMD	1/O road command
	ND CIVID	1/O read command







Figure 3-4 SCHEMATIC DRAWING: CHANNEL BOARD (Sheet 3 of 4)



### CHAPTER 4

# INTERFACE BOARD

The Interface Board provides the Diskette Channel with a means of communicating with the diskette drives, as well as with the INTELLEC System bus. Under control of the microprogram being executed on the Channel Board, the Interface Board generates those signals which cause the read/write head on the selected drive to be loaded (i.e., to come in contact with the diskette platter), then cause the head to move to the proper track. The Interface Board accepts the data being read off the diskette, interprets certain synchronizing bit patterns, checks the validity of the data using a cyclic redundancy check (CRC) polynomial, and passes the data to the Channel Board.

During write operations, the Interface Board outputs the data and clock bits to the selected drive at the proper times. It also generates CRC characters which are appended to the data; this allows the data to be verified when it is subsequently read.

When the Diskette Channel requires access to INTELLEC System memory, the Interface Board requests and maintains master control of the system bus, and generates the appropriate memory command.

When a CPU in the INTELLEC System issues a channel command to the diskette controller, the Interface Board acknowledges the command as required by INTELLEC System bus protocol.

The Interface Board resides within the INTELLEC System cabinet. The Interface Board, together with the Channel Board, constitute what we refer to as the Diskette Channel.

### 4.1 FUNCTIONAL ORGANIZATION OF THE INTERFACE BOARD

For descriptive purposes, the circuitry on the Interface Board can be divided into five functional blocks: (As shown in Figure 4-1)

- Disk drive control block
- Serial data/clock synchronization block
- Write clock generator block
- Cyclic Redundancy Check (CRC) block
- Bus control block

The DISK DRIVE CONTROL BLOCK provides the unit selection/head loading (SELn/) signal, the direction indicator (DIR/) and the step pulse (STEP/) that moves the read/write head on the selected unit one track in the specified direction. The disk drive control block also monitors the READY status, the INDEX indicator and the TRACKO indicator from the drives.

The SERIAL DATA/CLOCK SYNCHRONIZATION BLOCK receives the unseparated data, separates the data and clock bits with a phase locked loop, and examines the bit patterns looking for specific patterns which indicate an address mark. Address marks precede address and data fields and are used to synchronize the controller with the drive. The synchronization block then generates data and clock strobes (DATA SR STB and CLK SR STB) which shift the data and clock bits into the shift registers on the Channel Board. The synchronization block also includes a bit counter that determines when a byte (8-bits) has been shifted to/from the selected drive.

The WRITE CLOCK GENERATOR BLOCK provides double density encoding and timing references for the writing of data and clock bits. Data and clock bits are both output to the drive via the WRT DAT/ line. This write clock generator includes timing precompensation circuitry to anticipate bit shifting which occurs upon readback of the double density bit patterns.

The CRC BLOCK generates two CRC characters (16 bits) which are appended to the end of each address field and data field during format and write data operations. During read operations, the CRC block generates two CRC

A R号于哈森时日



Figure 4-1 INTERFACE BOARD: FUNCTIONAL BLOCK DIAGRAM

characters for each data field (includes address mark and 128 bytes of data) read, then compares these with the two CRC characters that were appended to the data field, to verify the validity of the data.

The BUS CONTROL BLOCK provides the interface with the INTELLEC System bus. The bus control block requests and maintains master control of the system bus, and generates the memory read (MRDC/) and memory write (MWTC/) commands that allow the diskette controller to access system memory. In addition, the bus control block acknowl-edges (XACK/) the I/O read (IORC/) or I/O write (IOWC/) command that is issued when the CPU in the INTELLEC System executes a channel command to the diskette controller.

## 4.2 THEORY OF OPERATION: INTERFACE BOARD

In this section we will describe the circuitry on the Interface Board. We will divide this theory of operation discussion into five sub-sections, each dealing with one of the functional blocks defined in Section 4.1.

The Interface Board accepts/transmits signals, data and power through three different PC edge connectors:

- P1 Bus connector (to/from INTELLEC System bus)
- P2 Controller connector (to/from Channel Board)
- J1 Drive connector (to/from diskette driver)

To avoid any ambiguity when referring to connector pins in subsequent paragraphs, we will always list the connector as well as the pin whenever such references are required; for example, P1–57 refers to pin 57 on connector P1. Pin lists for the three connectors are provided in Section 4.3.

The schematic drawing (6 sheets) for the Interface Board is also provided in Section 4.3.

The circuits which drive signals to the diskette drives and those which receive signals from the drives have been specified by the drive manufacturer. Refer to Chapter 5 for more information concerning the electrical characteristics of the interface. Note that all drive output and input signals are driven and received in parallel to/from each of the attached drive boxes (drives 0, 1 and drives 2, 3). Only one drive is selected at any time however.

## 4.2.1 Disk Drive Control

The disk drive control block interfaces with all drive input/output signals except read data, write data and write gate. The main function of this block is to cause the read/write head on the diskette drive to move to the next track (in either direction). The circuitry in this block is shown on sheet 1 (inop reset, track > 43), sheet 3 (drive selection, drive ready and write protect), and sheet 4 (step, direction, track 0, index and file inop).

The drive READY/ lines (pins J1 - 30, J1 - 24, J1 - 26, and J1 - 22 shown on sheet 3) are driven by each drive to indicate that a diskette is ready to be accessed in that drive. The disk drive control block receives the READY/ signals (I.C. A30) which are then passed to the Channel Board via the 7400 gates (A45) and the 74367 multiplexing gates at signal lines DR0/ (pin P2 - 15) and DR1/ (pin P2 - 17). The GATE LOWER signal (A58 - 9, sheet 1) is controlled by the microprogram (see Table 3-3) to multiplex the ready signals of either drives 0 or 1 or drives 2 and 3 to these pins. The ready lines for each drive are gated by a flip-flop which retains the 'drive not ready' status for that drive (I.C.s A43 and A44). These flip-flops are cleared by the RDY RS/ pulse (A38 - 11 on sheet 4) which is generated by the microprogram (see Table 3-3). In essence these flip-flops are used to insure that the Channel Board sees a 'drive not ready' status whenever a diskette is changed on a non-selected drive. The DATO/, DAT1/, DAT5/, and DAT6/ MDS BUS lines are driven at the P1 connector (sheet 4) whenever the READ INT/ signal is activated by the Channel Board, indicating the drive ready status to the Channel. The non-gated ready status of the selected drive is multiplexed and passed directly to the Channel Board as the SEL DR NRDY/ signal (pin P2 - 20) by the 74153 multiplexer (A31) under control of the unit select lines from the Channel Board (USA at Pin P2 - 9, USB at pin P2 - 12).

The unit select lines, USA and USB, are decoded by the 74S139 decoder (A56 on sheet 3) to generate the drive select signals. The decoder outputs are inverted and driven by 7438 gates (A17) at the DRV SEL lines to the drives (J1 - 46, J1 - 48, J1 - 50, J1 - 52). The HEAD LOAD/ signal (I.C. A46 - 4 on sheet 4) gates the DRV SEL signals. The decoder outputs are also used as inputs to the drivers for the drive select LED indicators (LED/ lines at J1 - 54, 66, 64, 68). These lines are also gated by the HEAD LOAD/ signal.

The HEAD LOAD latch is set by the LDHD/ control pulse (A47 - 3) which is generated by the microprogram being executed on the Channel Board (see Table 3-3). The LOAD latch is cleared by the UNLHD/ pulse (A47 - 11) which is also generated by the microprogram.

After loading the read/write head on the selected drive, the head must be positioned over the proper track. Any of the seven diskette operations will cause the diskette controller to seek the track specified in the I/O Parameter Block (IOPB), prior to actually performing the operation (refer to Chapter 2).

The direction of head movement is defined by the level on the DIR/ lines (pins J1 - 6, J1 - 8 on sheet 4). The DIREC control level (I.C. A58 - 11), maintained by the microprogram (see Table 3-3), is applied to the 7438 NAND gates in the disk drive control block. The outputs from these 7438 gates (A11 - 3, A11 - 6) drive the DIR/ lines.

Each pulse on the STEP/ lines (pins JI - 2, JI - 4) will cause the read/write head on the selected unit to move one track either in or out depending on the level of the DIR/ lines. When DIR/ is high, the head will move one track away from the center of the diskette. When DIR/ is low, the head will move one track closer to the center.

The STEP/ pulse is defined by the output of a 9602 one-shot (at A61 - 10). This one-shot is triggered by the CSTEP control pulse, generated by the microprogram (see Table 3-3), unless the read/write head at the selected unit is already over track 0 (the outermost track) while the DIR/ line indicates outward movement. If the head on the selected unit is loaded, the output from the one-shot will produce a 10 usec. pulse on the STEP/ line, as shown in Figure 4-2.

After the head has been positioned over the proper track (by pulsing STEP/ the required number of times), the diskette controller must wait at least 20 msec. before it begins examing the read data in an attempt to detect the ID address mark which precedes an address field. Reading the address field will verify that the seek operation placed the head over the proper track. Read initiate timing is illustrated in Figure 4-3.

The disk drive control block also includes a 9602 one-shot (at A61 – 7) which produces a 10 msec. TIMEOUT pulse, which is made available to the Channel Board (pin P2 – 38) for use by the microprogram. The microprogram triggers this one-shot by generating the SSCLK control pulse (see Table 3-3). Ten milliseconds after SSCLK triggers the one-shot, a low-to-high transition from the  $\overline{\Omega}$  output of the one-shot will appear on the TIMEOUT line.

The disk drive control block drives the INOP RESET/ lines (pins J1 - 60 and J1 - 62) and the TRACK>43/ lines (pins J1 - 56 and J1 - 58) to the diskette drives under control of the microprogram. The TRACK>43 latch (I.C. A46 - 7 on sheet 1) is set by the GTR43/ pulse (A59 - 3) which is generated by the microprogram (see Table 3-3).

The latch is reset by the NGTR43/ pulse (A59 - 6). The WFLRS level (I.C. A58 - 2) is maintained by the microprogram and drives the 7438 gates which in turn drive in INOP RESET/ lines to the drives. INOP RESET/ resets the FILE INOP/ lines driven by the selected drive. TRACK > 43/ forces the selected drive to reduce the write current on inner tracks of the diskette.

The disk drive control block accepts the TRACKO/, INDEX/, FILE INOP/, and WPROT/ lines from the diskette drives and passes them to the Channel Board for use by the microprogram. TRACKO/ (pin J1 – 38 or J1 – 44 depending on which drive is selected) is merely inverted twice and output as TRACKOO/ at pin P2 – 11. INDEX/ (pin J1 – 42 or J1 – 40) is inverted and clocks a 7474 latch to the set state. The Q output of this latch drives the INDEX line (pin P2 – 42) to the Channel Board. The microprogram can reset the INDEX latch by generating

the RNDX/ control pulse (see Table 3-3). An INDEX/ pulse will be received once every 166.7 msec. and will be approximately 1.7 msec. wide:



FILE INOP/ (pin J1 - 32 or J1 - 34) is inverted twice and passed to the channel board as the WRT ERR/ signal at pin P2 - 18. WPROT/ lines (pin J1 - 20 or J1 - 18) are multiplexed by the 74153 multiplexer (I.C. A31 on sheet 3) and passed on to the channel board at pin P2 - 14 to indicate the presence of a write protected diskette in the selected drive.

ers a fight of the set	Libertike unter demo brai	Construction of the second second second	
			staan ooloogoo goota bala Fisika shir dadhiin kaal
			bieri entatio ettal
	POWER UP		
SELD/			eager mad of up 5 all
(n=1 or 0)	(		
ATTAL LARGE T APPENDIA I MICH SERVICE ANTI-	"		
DIR/	by writing birster as minimum	-	Min.circled
a set in the set of the set of the set		per press live built ash	
to between any or that definition of	ette alle 197 bie eelligen ann		
	z sec	Ho men formined	aut of many included
STEP/		UU	
10	usec		
		min	

Figure 4-2 HEAD MOVEMENT CONTROL TIMING





### 4.2.2 Write Data Generator

The write data generator block develops the pulse stream which is driven to the drives as the WRT DAT/ lines (J1 - 10 and J1 - 12 on sheet 2 of the schematic). For each negative pulse on the WRT DAT/ line, the selected drive will change the direction of write current in the magnetic head, resulting in a flux reversal on the diskette media. The selected drive supplies write current to the media (that is, 'writes') only if the WRT GT/ signal is activated. The micro-program controls the WRT GT/ lines (pins J1 - 14 and J1 - 16 on sheet 2) by the DISK WRITE signal which is sent to the Interface Board at P2 - 55 (sheet 5).

The write data is double-density encoded using the Modified-Modified Frequency Modulation (M<sup>2</sup>FM) algorithm explained in Section 1.2. Figure 4-4 illustrates the double density encoding and provides a comparison with singledensity (FM) encoding to show that the bit cell time can be halved from 4 us to 2 us since the minimum time between pulses is 2 us. in both cases. Note that clock bits are only written to aid read-back synchronization and data recovery.

Since the bit cell is halved with double-density encoding, data recovery is more susceptible to errors associated with magnetic bit shift. To minimize the effects of read-back bit shift, the write data block includes precompensation circuitry. This circuitry anticipates magnetic shifts by writing bits earlier or later than nominal bit times in an opposite direction to the magnetic shifts that will occur upon readback. For example, the third data bit from the left (M<sup>2</sup>FM) in Figure 4-4 will tend to shift upon readback towards the '0' bit cell (to the right). This shift is 'precompensated' by writing the bit closer to the preceding data bit (more to the left).

The precompensation and encoding circuitry are shown on sheet 2 and 3 of the schematic. The write oscillator, Y1, outputs an 8 Mhz clock signal which drives a 74164 (A8 - 8) 8-bit shift register which has been connected as a bit-ring. The outputs of the bit ring are connected to 'AND' gates (7402, 7411 and 7408) which generate active high pulses relating to the specific clock bit times and data bit times which, in turn, are selected as WRT DAT/ pulses by the 74150 multiplexer (A34).

Figure 4-5 illustrates the timing of the precompensation circuitry which generates the pulses used by the encoding circuitry. Note that there are two possible times to write a clock bit: on-time (C), or 125 ns. early (CE). There are three possible times to write a data bit: on-time (D), 250 ns. early (DE) or 250 ns. late (DL).



0

### M<sup>2</sup>FM ENCODING RULES:

67

• WRITE CLOCK BITS (PULSES) AT THE BEGINNING OF A BIT CELL

WRITE DATA BITS AT THE MIDDLE OF A BIT CELL

WRITE A DATA BIT FOR EACH BIT CELL WITH A BINARY '1' VALUE

 WRITE A CLOCK BIT ONLY IF THERE IS NO DATA BIT IN THE CURRENT CELL AND THERE WAS NO CLOCK OR DATA BIT IN THE PRECEDING CELL

Figure 4-4 M<sup>2</sup>FM DATA ENCODING





100



The WRITE CLOCK signal (A8 - 3) is used to shift the serial data in the precomp selection and encoding shift register (A48 on sheet 3). In addition, the WRITE CLOCK signal is multiplexed with the read clock by the DISK WRITE signal to generate the CLOCK SR STB and DATA SR STB signals (P2 - 8 and P2 - 48 shown on sheet 5). These signals are used by the Channel Board to shift the data byte being written or read by the drive.

The encoding and precompensation selection for the write data is performed by the data shift register (A48) and the 74150 multiplexer (A34). The outputs of the register (SDA, SDB, SDC, SDD) drive the select inputs of the 74150 multiplexer. Depending upon the data pattern presented at the select inputs, the 74150 selects one of the five timing pulses during each bit cell (i.e., C, CE, D, DE or DL). For a 'zero-data' bit cell which was preceded by a bit cell which generated a pulse, no pulse is selected. The pair of flip-flops (A10 on sheet 3) which are clocked by WRITE CLOCK generate the CLOCK GATE signal (A10 - 8). This signal gates the C and CE pulses so that only every other clock bit is written in a string of 'zero' bit cells. Figure 4–6 illustrates the signal timing of the circuitry which generates WRT DAT/ pulses.

The AMWRT/ latch (A58 – 6 on sheet 1) is controlled by the microprogram on the Channel Board and is used to set the CLOCK GATE active during the writing of an address mark, resulting in a unique clock pattern (three clock bits in sequential bit cells) which aids in read-back synchronization. In addition, the AMWRT/ level controls the 74157 multiplexer (A7 – 5 on sheet 2) by selecting the appropriate precompensation times during an address mark. Note that all of the switches shown on sheet 2 and 3 of the schematic are only manufacturing options for an alternate type of data encoding and are not field selectable.

### 4.2.3 Serial Data/Clock Synchronization

The serial data/clock synchronization block contains circuitry which separates the serial READ DATA pulses from the drive into data and clock bits for serial transfer to the Channel Board. The circuitry can be subdivided into the following segments: phase locked oscillator (PLO, shown on sheet 6), PLO start-up logic (sheet 5), and byte-synchronization counter (A19 on sheet 4).

The PLO consists of linear circuitry which 'locks' onto the recorded information and generates separate 'windows' for data bits and clock bits. Staying in synchronization with small, slow variations in disk speed, it averages quick variations caused by bit shift. Figure 4–7 provides a block diagram of the PLO with startup logic and data separator.

When not reading, the RESET READ/ level (A46 – 9 on sheet 4), maintained by the microprogram on the Channel Board, is active (Iow) and the PLO is locked to the write oscillator. The 2F CLOCK signal is multiplexed to fire the SAMPLE one-shot (A37 – 5 on sheet 5) which provides the input pulse train feeding the PLO. When the microprogram initiates a read operation by inactivating the RESET READ/ signal, the PLO startup logic is activated. The startup logic monitors the drives' READ DATA/ signals (pins J1 – 36 and J1 – 28) until the all 1's area in an address mark preamble is detected. Then the PLO input pulse stream is switched from the write oscillator to read data. As soon as the PLO is locked to the read data, the startup logic starts waiting for the first bit of the address mark, that is, the first '0' bit cell. When this bit cell is detected, the ENABLE BR signal (A15 – 5 on sheet 5) is activated, enabling the 74195 bit ring to start counting the bits. On every eighth bit cell count, the 'F' signal (pin P2 – 58) is activated to notify the Channel Board that a valid data byte has been read. When the Channel Board receives the first 'F' signal, it compares the data and clock bytes with the known address mark patterns. If there is a match, the Channel Board continues to accept data bytes and the PLO stays locked to the read data. If there is not a match, the Channel Board resets the read circuitry by activating the RESET READ/ level and later enabling the read circuitry to continue searching for the desired address mark. Figure 4–8 illustrates the detailed timing for the serial data/clock synchronization block during the address mark synchronization process.

### 4.2.4 Cyclic Redundancy Check (CRC)

Two cyclic redundancy check (CRC) characters (16-bits) are generated for each data field (i.e., the address mark and 128 bytes of data) and are then appended to the data field as it is written to diskette. During all read operations, 16 CRC bits are generated as data is read; these CRC bits are then compared with the CRC bits that were appended to the field when it was written. CRC generation and checking are performed by the CRC block which consists of

瞬間はませる 二 夏行がれ えんばに ものみればら だけました いっかい

¥.

U

6

**i**()



Figure 4-7 PHASE LOCKED OSCILLATOR





a 9401 Universal Polynomial Generator (UPG), a 7451 multiplexer, a control latch, and several inverting circuits, as shown on sheet 4 of the board schematic (see Section 4.3).

During write operations, data bits from the data shift register (on the Channel Board – see Section 3.2.5) are input to the 9401 UPG device (pin 11, D), as well as the 7451 multiplexer via the SR DATA OUT line. The SR OUT control level (maintained by the microprogram on the Channel Board – see Table 3–3) allows the data bits through the multiplexer and onto the WRT DAT/ line. The data bits, which are also being input to the 9401 device, cause the 9401 to generate the CRC characters (16 bits) for the 128 data bytes by 'dividing' the data by the encoding polynomial ( $x^{16} + x^{12} + x^5 + 1$ ). When the entire 129 bytes (1 address mark byte and 128 data bytes) have been written to disk, the microprogram lowers the SR OUT level, which allows the 16 CRC bits being output by the 9401 device (pin 12, SDO) to pass through the 7451 multiplexer and be written onto the diskette immediately after the data.

During read operations, each data byte is shifted into the 9401 UPG device as the succeeding data byte is being shifted into the data shift register (on the Channel Board). The data bits are carried on the SR DATA OUT line, just as during a write operation. The absence of the SR OUT control level (from the microprogram), however, prevents the data bits from being gated out onto the WRT DAT/ line. The 129 bytes are 'divided' by the encoding polynomial to generate 16 CRC bits. After all 129 bytes have been read, the 16 CRC bits which were appended to the data when it was written are also shifted into the 9401 device where they are compared with the CRC bits just generated. If the two sets of CRC bits match, the all zeroes output (ER, pin 13) goes true (low), and is applied to the D-input on a 7474 latch at A60 - 12. When the bit counter in address mark detection logic determines that all data has been shifted out of the data register (i.e., when the F signal goes true), the low level from the ER output is clocked into the 7474 latch. The high  $\overline{\Omega}$  output from this latch drives the AZ line (pin P2 - 41) to the Channel Board.

The microprogram controls the various operating modes of the 9401 UPG by maintaining the appropriate levels on the CRCMD control line (see Table 3–3). CRCMD, which feeds the shift right (CWE) input to the UPG, is usually low, causing logical zeroes to be shifted through the UPG. It is only when CRC characters are being generated or checked that CRCMD presents a false (high) level to the active-low CWE input. The 9401 device is clocked by the data shift register strobe signal.

#### 4.2.5 Bus Control

The bus control block maintains the diskette controller interface with the INTELLEC System bus. This block consists of a 52-104 Bus Control I.C., six flip-flops, a 9602 one-shot multivibrator and assorted gating and inverting circuits, as shown on sheets 1 and 2 of the board schematic (see Section 4.3).

Before the diskette controller can transfer data to or from system memory, the bus control block must request and be granted master control of the INTELLEC System bus. When the Diskette Channel requires access to memory, the microprogram (being executed on the Channel Board – see Chapter 3) will initiate the bus request sequence by generating the SMREQ/ control pulse (see Table 3–3). SMREQ/ will cause the 74LS112 latch at A51 – 4 to be pre-set unless the inhibit memory write latch (A46 –13) is set.

The inhibit memory write latch will be set during VERIFY CRC diskette operations, in which data is read and verified but is not transferred to memory. The inhibit memory write latch is set and reset by the SINH/ and RINH/ control pulses, respectively (both are generated by the microprogram, see Table 3–3).

The Q output from the 7474 latch which is pre-set by SMREQ/ (A51 - 5) is applied to the transfer request inputs of the 52-104 Bus Control I.C. (A50 - 25, 3, 4). The next bus clock pulse (BCLK/ at P1 - 13) will clock this input into the 52-104. The low  $\overline{Q}$  output drives the XFER REQ/ line (pin P2 - 39) which informs the Channel Board that the memory transfer is not yet complete. The Q output from the transfer request latch feeds the J-input of the data overrun (DOR/) latch.



12

Figure 4-9 BUS CONTROL TIMING

If the microprogram requests a memory access again (i.e., if SMREQ is generated again) before the current access is completed, the data overrun latch will be clocked to the set state, and its  $\overline{Q}$  output will drive a true (low) level on the DOR/ error line to the Channel Board (pin P2 - 16).

When the 52-104 Bus Control I.C. receives the XFER REQ input, it initiates a memory transfer bus cycle, causing BREQ/ (pin P1 - 18) to go true (low). BREQ/ requests use of the INTELLEC System bus.

If no other master module is using the bus (i.e., if BUSY/ is false), and if no higher priority module is requesting the bus (i.e., the bus priority in line, BPRN/, is true), the next bus clock pulse (BCLK/) after BREQ/ will cause the 52-104 to activate BUSY/ (pin P1 – 17). BUSY/ informs the INTELLEC System that the diskette controller has master control of the bus. In addition the 52-104 activates the ADEN/ output which is inverted to generate the SELECTED signal (pin P2 – 43). On the next BCLK/ pulse after BUSY/ goes true, the 52-104 will drive the memory read (MRDC/) or memory write (MWTC/) command at pins P1 – 19 and P1 – 20, respectively, depending upon whether a read or write cycle was requested by the microprogram controlled MEMWRT level (A58 – 4 on sheet 1).

Recall that while logic on the Interface Board requests control of the bus, then generates the memory read or write command, it is the Channel Board which actually drives the system data and address buses (refer to Chapter 3) as gated by the SELECTED signal.

When the memory has accepted the data to be written or output the data which was read, it generates a transfer acknowledge signal (XACK/) which is received at pin P1 – 23 on the Interface Board. XACK/ triggers a 9602 one-shot (A37 – 11). The high pulse ( $\sim$ 70 nsec. wide) at the Q output of the one-shot drives the STB MEM IN line (pin P2 – 29) which allows the Channel Board to accept data read from memory.

The  $\overline{\Omega}$  output from the one-shot clocks the XFER REQ 7474 latch at A51 – 1 to the reset state. As a result, succeeding bus clock pulses (BCLK/) can reset the bus control logic, and cause the Interface Board to relinquish master bus control to another module.

Bus control timing is illustrated in Figure 4-9.

ROTATION AND THE OTHER AND ADDRESS





In addition to being the master module during memory access operations, the diskette controller also acts as the 'slave' module during I/O operations in which the CPU executes a channel command for the diskette controller. The bus control block accepts the I/O read (IORC/) or I/O write (IOWC/) command from the CPU (at pins P1 – 21, P1 – 22), inverts it and passes it to the Channel Board on the READ CMD line (pin P2 – 60) or the WRT CMD line (pin P2 – 53).

The 'slave' module must acknowledge all commands from the master. The bus control block performs this function in response to channel commands. Receipt of a 'reset', 'read subsystem status' or 'read result type' channel command (see Chapter 2) will clock the acknowledge latch (at A39 – 3) to the set state. The acknowledge latch is set at the proper time by the SACK/ control pulse (A57 – 11) from the microprogram for each of the other channel commands. The  $\overline{\Omega}$  output from the acknowledge latch feeds a 74125 tri-state driver. The output from the 74125 circuit (XACK/) is driven through pin P1 – 23. XACK/ is reset when IORC/ or IOWC/ go false via the 7432 gate (A38 – 8).

The bus control block also has an 8 position rotary switch which connects the interrupt line (INT/) from the Channel Board (pin P2 – 40) with one of the eight system priority interrupt request lines, INTO/ - INT7/ (via a 74125 tri-state gate which provides the required electrical characteristics for the INTELLEC System bus).

In addition, the two phase clock pulses (CLK1/ and CLK2/ on sheet 1) are generated in the bus control block. CLK1/ and CLK2/ are derived from the INTELLEC common clock, CCLK/ (9.8 MHz). CCLK/ is divided by the two 74LS74 flip-flops at A54 to produce CLK1/ and CLK2/ (400 nsec. period, 12% duty cycle) at the outputs of the 74S139 decoder as shown in Figure 4-10.

## 4.3 SCHEMATICS/PIN LISTS: INTERFACE BOARD

The schematic drawing (6 sheets) for the Interface Board is provided in Figure 4-11. These schematics are subject to change without notice. The Reference Schematic Drawings shipped with the Diskette System should be used as a reference.

Table 4–1 lists the pins and designated signal functions for the 86-pin P1 bus connector. Table 4–2 lists the same information for the 60-pin P2 controller connector, while Table 4–3 provides this information for the 100-pin J1 drive connector.

# Table 4-1 PIN LIST: P1 BUS CONNECTOR

PIN	SIGNAL	FUNCTION	
1	<b>A</b>		
2			
3			
4			
5			
6	NO CONNECTION		
7			
8			
9			
10			
11			
12			
13	BCLK/	Bus clock (9.803 MHz)	
14	INIT/	System initialization	
15	BPRN/	Bus priority in	
16	BPRO/	Bus priority out	
17	BUSY/	Bus busy	
18	BREQ/	Bus request	
19	MRDC/	Memory read command	
20	MWTC/	Memory write command	
21	IORC/	I/O read command	
22	IOWC/	I/O write command	
23	XACK/	Transfer acknowledge	
24		entransite par leave the contract public terms which share we are a	
25	The dustrial sheets the PARSES 45		
26	IF AL and SEX and the whet of		
27	NO CONNECTION		
28	an dear " () FISSE period supervised and		
29	News, WETS) - RY TV CONSTR		
30	<ul> <li>Lavet result of</li> </ul>	in the second of the resourced static light devices for the the transformer with the first transformer devices	
31	CCLK/	Common clock (9.803 MHz)	
32	sent fordation and with our behinding		
33	NO CONNECTION		
34	vendel et the dy data of the 74	ips at ASS to the state CEEL and CE.S.27 (400 ose), sector 12% day	
35	INT6/		
36	INT7/		
37	INT4/		
38	INT5/	Priority interrupt request lines	
39	INT2/		
40	INT3/		
41	INTO/		
42	INT1/		
43	The contraction Tense in the		
44	set in a caracter are set		
45	NO CONNECTION		
46			
47			
48	↓ ↓		
PIN	SIGNAL	FUNCTION	1919
-----	---	-----------	------
19			
50	the standard and the standard		
51	Sakere austriller noch i		
2	1 Yes shall A		
3	2 12 1 12 1 12 1 1 1 1 1 1 1 1 1 1 1 1		
4	Saturi erazi - Saturi		
5	Missis New T		
i6	Salette catelo atrone		
57	A std restart by		
8			
9	testeleser 68 adurti		
60	It with readers which		
51	15 323 March 1		
52	District provided		
63	Crive O ready or Brive 2 reader		
64	Guida construction and an		
65	NO CONNECTION		
66	Wetta with		
67	Shift register out christical level		
68	Solution thread in the second		
69	Cristical defenden surgest C		
0	Sector data in the		
1			
2	Serial data threby		
'3	Second the state and here		
74			
75	Conversi derestio 8 surgest		
6	talas wai a nebeceste listareadi		
77	Bitrabe methody lines in		
'8	Dimensi sompratier prace 2		
'9			
30			
31	Carteria de cader la carta /		
32	E 102 Reptil		
33	<ul> <li>a nicital photos (consel)</li> </ul>		
34	78 state 6		
35	Search by an average in a second second		
36	Course provints means BI	1996 1991	
	Controller requests INTELEC Specific hits		

# Table 4-1 PIN LIST: P1 BUS CONNECTOR (CONTINUED)

# Table 4-2

PIN LIST: P2 CONTROLLER CONNECTOR

TION
1
adv
auy
adu alia
ady
un l
vei
command
LEC System bus
NIELLEC System bus

PIN	SIGNAL	FUNCTION
49	RESET/	'Reset' channel command
50	MK2	Mask bit 2
51	MEM WRT	Write data to Intellec System memory
52	DEC OUT 1/	Control decoder output 1
53	WRT CMD	I/O write command
54	MK5	Mask bit 5
55	WRTGT	Write gate control level
56	MR	Master reset
57	RD INT/	'Read subsystem status' channel command
58	F F	Shift registers full or empty
59	TP	Test point
60	RD CMD	I/O read command

### Table 4-2 PIN LIST: P2 CONTROLLER CONNECTOR (CONTINUED)

Table 4-3 J1 DRIVE CONNECTOR

#### PIN FUNCTION SIGNAL 1 GND Ground 2 STEP 0, 1/ Steps head one track (drive 0, 1) Ground 3 GND Steps head one track (drive 2, 3) STEP 2, 3/ 4 5 GND Ground 6 DIR 0, 1/ Step direction indicator (drive 0, 1) 7 GND Ground 8 DIR 2, 3/ Step direction indicator (drive 2, 3) 9 GND Ground 10 WRT DAT 0, 1/ Write data (drive 0, 1) 11 GND Ground 12 Write data (drive 2, 3) WRT DAT 2, 3/ 13 GND Ground 14 Write gate (drive 0, 1) WRT GT 0, 1/ 15 Ground GND 16 WRT GT 2, 3/ Write gate (drive 2, 3) 17 Ground GND 18 WPROT 2, 3/ Diskette write protected indicator (drive 0, 1) 19 GND Ground 20 WPROT 0, 1/ Diskette write protected indicator (drive 2, 3) 21 GND Ground 22 READY 3/ Ready indicator from drive 3 23 GND Ground 24 **READY 1/** Ready indicator from drive 1 25 GND Ground 26 **READY 2/** Ready indicator from drive 2 27 GND Ground 28 READ DATA 2, 3/ Read data, unseparated (drive 2, 3)

PIN	SIGNAL	FUNCTION	Mith
29	GND	Ground	23
30	READY 0/	Ready indicator from drive 0	
31	GND	Ground	
32	FILE INOP 0, 1/	Drive inoperable, write fault (drive 0, 1)	
33	GND	Ground	
34	FILE INOP 2, 3/	Drive inoperable, write fault (drive 2, 3)	
35	GND	Ground	
36	READ DATA 0, 1/	Read data, unseparated (drive 0, 1)	
37	GND	Ground	
38	TRACK00 - 0, 1/	Track 0 indicator (drive 0, 1)	
39	GND	Ground	
40	INDEX 2, 3/	Index indicator (drive 2, 3)	
41	GND	Ground	
42	INDEX 0, 1/	Index indicator (drive 0, 1)	
43	GND	Ground	
44	TRACK00 – 2, 3/	Track Ø indicator (drive 2, 3)	
45	GND	Ground	
46	DRV SEL 0/	Select/load head drive Ø	
47	GND	Ground	
48	DRV SEL 1/	Select/load head drive 1	
49	GND	Ground	
50	DRV SEL 2/	Select/load head drive 2	
51	GND	Ground	
52	DRV SEL 3/	Select/load head drive 3	
53	GND	Ground	
54	LED 0/	Drive 0 selected indicator	
55	GND	Ground	
56	TRACK > 43 - 0, 1/	Track greater than 43, low write current (dr	ive 0, 1)
57	GND	Ground	
58	TRACK > $43 - 2, 3/$	Track greater than 43, low write current (dr	ive 2, 3)
59	GND	Ground	
60	INOP RESET 0, 1/	File inoperable reset (drive 0, 1)	
61	GND	Ground	
62	INOP RESET 2, 3/	File inoperable reset (drive 2, 3)	
63	GND	Ground	
64	LED 2/	Drive 2 selected indicator	
65	GND	Ground	
66	LED 1/	Drive 1 selected indicator	
67	GND	Ground	
68	LED 3/	Drive 3 selected indicator	
69	TP	Test Point	
70	TP	Mani wilks	
71	TP	GHD CHED	
72	TP	this shirt is wanted	
73	TP	State State	
74	TP	NE ARRY 21 STORE FOR	
75	TP		
76	TP	Test Point	

# Table 4-3 J1 DRIVE CONNECTOR (CONTINUED)



## Table 4-3 J1 DRIVE CONNECTOR (CONTINUED)

1











每回4.4.4.11。我们可能指指了UC 和优化的问题的。 10月节期开始存着 你认真的问题 (finite of of th

4-26



6

Figure 4-11 SCHEMATIC DRAWING: INTERFACE BOARD (Sheet 6 of 6)



# CHAPTER 5 DISKETTE DRIVES

The Diskette System uses the Shugart Associate's SA 800-1 Flexible Disk Drive (FDD) or equivalent. The FDD is a reliable random access storage device utilizing a single, removable diskette as the storage medium. This chapter summarizes the manufacturers information on the drive. The FDD uses an IBM 3740 media compatible diskette. The disk itself is 7.88 inches in diameter and is contained in an 8 inch square protective envelope. To load the disk, the entire envelope is inserted into a slot in the FDD behind a small access cover.

Rotating at 360 rpm, data is read or written on the 77 tracks of the single recording surface at a rate of 500,000 bits per second in double density mode to provide a total unformatted capacity of 6-megabits. The single head need only be in contact with the media during actual data transfer operations. Track accessing is accomplished using a stepping motor. Index is detected using a photo-optical technique to sense the physical index hole in the disk cart-ridge.

The FDD contains all the analog read, write and control electronics necessary to perform data transfer operations using only simple control commands.

### 5.1 FUNCTIONAL DESCRIPTION

The following paragraphs describe the major components of the FDD.

#### **Electronics:**

All electronic circuitry required to convert from the digital I/O to the analog read/write and positioning information is contained on a single circuit board mounted underneath the deck. Logic is  $T^2L$  with a minimal number of discrete analog components.

#### **Positioner:**

Positioning of the read/write head is accomplished using a stepping motor driving a lead screw shaft.

#### Head Loading Mechanism:

Head loading is achieved by a solenoid/pressure pad scheme. When the solenoid is activated, it releases the pressure pad arm which, in turn, pushes the disk against the read/write head.

#### Spindle Motor:

The spindle is belt driven from the spindle motor, which maintains a speed of 360 RPM  $\pm 3.5\%$ .

#### **Disk Loading Mechanism:**

Disk Loading is accomplished when the disk loading access cover is closed. A two piece expandable centering cone is loaded against the center of the disc on the side opposing the spindle, causing the disk to be located accurately between the centering cone and the spindle. The centering cone, disk, and spindle then rotate together.

#### Head:

The read/write head is a single gap head plus track edge erase gaps. Nominal track width is 0.013 inches.

### Mechanical Framework:

A solid deck die casting provides a clean construction to enhance reliable operation. The deck casting provides for spindle housing, disk cartridge registration and envelope stabilization surfaces, drive motor mounting surfaces, stepper motor mounting surface, electronic circuit board mounting as well as providing a stable base for integration and operation of unit components. A secondary frame die casting provides stable mounting, in relationship to the main deck casting, for the disk centering cone and loading mechanism.

A simple disk loading access cover completes the disk loading/unloading mechanism and prevents the possibility of objects falling into the unit.

#### Diskette:

The single disk cartridge is in a sealed envelope. The envelope size is 8" x 8" with a recording disk diameter of 7.88". The FDD uses the IBM 2305830 type diskette or double density certified media such as Dysan 3740D or ITC 34-9000D.

The disk has 77 concentric recording tracks spaced .02083 inch apart on a single surface. Track centerlines are calculated by the formula: centerline radius = 2.029 + (76-N). N is the physical track number. 48

### 5.2 PERFORMANCE CHARACTERISTICS

The following sections list the performance characteristics of the FDD.

### 5.2.1 Recording Characteristics

M<sup>2</sup>FM, self-clocking, serial-by-bit for double density operation, providing:

Outer track (TR00)	-	36
Inner track (TR76)		65
Track density	9 <u></u>	48

3672 bits/inch 6576 bits/inch 48 tracks/inch

#### 5.2.2 Bit Transfer Rate

Based on a nominal disk speed of 360 rpm, the bit transfer rate is 500,000 bits per second.

#### 5.2.3 Data Capacity

The data capacity listed below is an unformatted maximum and will be reduced by formatting allowances for sector operation and spare track allocation.

Track capacity – Disk capacity –

83,328 bits 6,416,256 bits

## 5.2.4 Latency Time

Latency time is the time required to reach a particular point on a track after positioning is complete. It is a function of spindle speed.

The spindle speed for the FDD is 360 RPM  $\pm$ 3.5%. The speed tolerance includes motor performance, pulley tolerance, spindle variation,  $\pm$ 10% AC line voltage variation, and a  $\pm$ 2% AC line frequency variation.

Based on a nominal disk speed of 360 rpm, the average latency time is 83.33 milliseconds. Based on a minimum disk speed of 347 rpm, (360 - 3.5%) the maximum latency time is 173 milliseconds.

### 5.2.5 Positioning Characteristics

The time for a single track move is 20ms including settling time. This is defined as the time to move between any pair of adjacent tracks. Multiple track moves can be made at 10ms per step plus 10ms settling time.

The random average positioning time is 260ms including settling time. This is defined as the summation of the move times for all possible moves divided by the number of possible moves.

The maximum positioning time is 770ms. This is defined as the time to move the head from track 00 to track 76 or from 76 to 00 and includes settling time.

#### 5.2.6 FDD Start and Stop Time

The FDD spindle runs at all times while power is applied to the unit and is not stopped for disk loading or unloading. Since the time for the disk to reach the same speed as the spindle is negligible (less than 2 seconds) there is essentially no operator waiting time required.

#### 5.2.7 Error Recovery

#### **Read/Write Errors**

To guard against degradation from imperfections in the media, it is recommended that no more than 4 attempts to write a record be used when read after write errors are encountered. In the event a record cannot be successfully written within 4 attempts, it is recommended that the sector or track be labeled defective and an alternate sector or track assigned. If more than 2 defective tracks are encountered, it is recommended that the disk be replaced.

In the event of a read error up to 10 attempts should be made to recover with re-reads. If after 10 attempts the data has not been recovered, step the head several tracks away and re-position to recover the data. If the error persists, the sequence should be attempted at least 10 times. Unloading the head when data transfers are not imminent will increase the data reliability and extend the disk life.

#### Seek Errors:

Seek errors will rarely occur unless the stepping rate is exceeded. In the event of a seek error, recalibration of track location can be achieved by repetitive Step Out commands until a track 00 signal is received.

## 5.2.8 Environmental Limits

#### **Temperature and Humidity:**

The FDD can withstand the following conditions, if the combined rate of temperature and humidity change precludes condensation of moisture on any part of the unit.

	Operating	Storage and Transit
Temperature, <sup>O</sup> F	50° to 100°	-30° to 150°
Temperature, <sup>o</sup> C	10º to 38º	-35° to 65°
Temp. Change, <sup>o</sup> F/Hr.	12	60
Temp. Change, <sup>o</sup> C/Hr.	6.7	33
Relative Humidity	20% to 80%	5% to 95%
Max. Wet Bulb Temp. <sup>o</sup> F	80	
Max. Wet Bulb Temp. <sup>o</sup> C	26.7	

#### 5.2.9 Write Protect

Write protect uses a photo-optical sensor that senses the presence of a write protect hole in the diskette jacket (see Figure 5-4). This feature prohibits the controller from accidently writing on a protected disk. The diskette can be written upon, if so desired, by masking the write protect hole.

### 5.3 INTERFACE SPECIFICATION

The following paragraphs describe the control and data interface lines, shown in Figure 5-1.

All signal lines must be terminated at the receiver with an impedance of 130 ohms, nominal. The following definitions will be used in the signal definitions:

LOGIC LEVEL	STATUS SIGNALS	COMMAND SIGNALS	
High (False) (Ø)	2.4V min.	2.0V min.	
Low (True) (1)	0.4V max.	0.8V max.	

Figure 5-2 illustrates the basic driver and receiver circuits for the FDD.

Control and Data Lines to the FDD:

1. STEP

A 10 microsecond (minimum) logic 1 level pulse on this line causes the head to move one track inward or outward from the center of the disk, depending upon the state of the direction line.

#### 2. DIRECTION

A logic 1 level on this line causes the head to move toward the center of the spindle when a step signal occurs.

#### 3. UNIT SELECT 1, 2

Two unit select lines are used by the controller to select the appropriate drive. These two lines are mutually exclusive; only one drive can be selected at a time. The lines must remain active during any command from the controller. Logical Unit assignment is accomplished by means of the unit select jumpers on the drive Printed Circuit Board and the appropriate signal adapter PCB attached to the drive (either drive 0 or 1).

#### 4. WRITE ENABLE

To enable the FDD write driver, this line is held at a logic 1.

To disable the FDD write driver and enable the FDD read circuitry, this line is held at logic 0.

#### 5. WRITE FAULT RESET

A logic 1 level on this line clears the Write Fault Latch. This signal is not used on the SA 800-1 drive.

#### 6. WRITE DATA (REFER TO FIGURE 5–3)

This line contains the double-density encoded Write Clock and Data information to the FDD. The Write Clock and Data Pulses must be 250 nanoseconds  $\pm$  20% in length and are true at the logic 1 level. Information to be recorded on the disk is derived from the leading edge of each pulse (i.e., at the logic 0 to logic 1 transition point).

#### 7. LOW CURRENT

A logic 1 level on this line causes reduced write current to be used during a write operation. Low current should be true for all tracks greater than 43 (inner tracks). It is not necessary to gate low current with write enable in the controller. This signal is not used on the SA 800-1 drive.



# NOTE: FOR FOUR-DRIVE OPERATION THE CABLING SHOWN IS DUPLICATED FOR AN IDENTICALLY CONFIGURED SECOND DRIVE BOX.

Figure 5-1 FDD/FDCC INTERFACE LINES

5-6



Figure 5-2 FDD DRIVER/RECEIVER CIRCUITS

Control and Data Lines from the FDD:

#### 1. INDEX

This line gives an indication of the relative position of the disk by outputting a logic 1 pulse for every revolution of the risk. The pulse of  $1.5 \pm 0.7$  milliseconds is generated by sensing the index hole in the disk using a photo-optical technique.



a

3

3

# Figure 5-3 WRITE DATA TIMING

#### 2. WRITE FAULT

A logic 1 level on this line indicates one or more of the following fault conditions:

-write enable without head load.
 -write enable without write data.

NOTE: Erase current signal is derived internally on PCB from the write enable input line. Erase current is on automatically during writing.

A fault on this line can be cleared by a logic 1 on the Write Fault Reset line to the FDD. This signal is not used on the SA 800-1 drive.

#### 3. TRACK 00

A logic 1 level on this line indicates that the head is positioned over track 00.

#### 4. READ DATA (REFER TO FIGURE 5-4)

This line contains the composite data and clock information. A logic 1 level pulse of 250 nsec  $\pm$  20% corresponds to a data bit or clock bit. This information is decoded within the controller.

#### 5. UNIT READY INTERRUPT 1, 2

There are two Unit Ready Interrupt lines, one from each unit, indicating that the unit power is on, the door is closed and the diskette has reached its final speed. The Unit Ready Interrupt assignments are accomplished by attaching the 'drive 0' or 'drive 1' signal adapter PCB.

#### 6. WRITE PROTECT

This line will be a logical 1 when the write protect hole in a diskette jacket is present. When logical 1 this line will disable write and erase current circuitry. (For hole location, refer to Figure 5–5).

#### 5.4 DISKETTE CARTRIDGE STORAGE AND HANDLING

The disk performs well when given reasonable care. The same handling specified for computer magnetic tape should be followed. Some specific areas are as follows:

When not in the unit, keep the disk in the protective envelope. Place the disk in the envelope before writing on the label so that the label is visible through the cut-away front of the envelope.

Always handle the disk by the label area to avoid touching the mylar surface.

Keep all magnets away from disk. Magnetic fields can destroy recorded data on the disk.

Do not touch or attempt to clean the disk surface. Abrasion may result in loss of stored data.

5-9

					Societies and		
SELECT	- Burne						
		497 655 - 99 J. 91			<u>992 001 841</u>	an dual Pr	
	/						
	(						
		and the second second second					
ENABLE							
· · · · · · · · · · · · · · · · · · ·	-)						
	/						
	/						
	/						
HEAD LOAD	1						
design of the second state	4						
	4						
			3.3	TIURAS	THI YOAR	a ragio la	
16 T		nuss mon ason	t, 2 Ist Root, 1	THERAS	rt <mark>ki Vdač</mark> i ust fili pu	8, 70895 (8 7 996 30677	
16) - 13 (15-15		nass mort est	5, 2 191 1100 - 10 191 1100 - 10	THURAS	HHL VOAS) MR THU DW D MT .40 S	8, 70850 - 8 7 986 30647 1986 30647	
46) - 3 (16-12) (16-12)		nusa mon eks autostrainib a sus strainib a	t, 2 opt Rough Latenth The Latenth Laten	THURAS	ntiti Vidiala Marini Vidiala Marini Jao a Marini Marini	R. TARLE	
VALID READ DATA/CLOCK		nusis mon sino aut straikih a badailganobas '1'	t, 2 op Robin of Grant to combine to combine to the Tr	THURAS Internet of a second to be regional des 1100 automatics	.0,		·11
VALID READ DATA/CLOCK			t, 2 opt House of and the optical set of the optical set of	11'	ʻ0ʻ	·1·	-'1'
VALID READ DATA/CLOCK			·1· D	'1' D	ʻ0ʻ	'1' D	'1' Ď
VALID READ DATA/CLOCK			ή. D	'1' D	,0,	'1' D	'1' Ď
VALID READ DATA/CLOCK			лан алан алан лан алан алан лан алан ала	'1' D	10°	1' D	'1' Ď
VALID READ DATA/CLOCK	$\frac{1}{2}$		·1· 	'1' D	.0,	'1' D	'1' Ď
VALID READ DATA/CLOCK	$\frac{1}{2}3$			'1' D	°0°	'1' D	'1' Ď
VALID READ DATA/CLOCK	$\frac{1}{2}$	$ \begin{array}{c}                                     $	ή, D		'0'	1' D	'1' Ď
VALID READ DATA/CLOCK	$\frac{1}{2}$	$\begin{array}{c} 11' \\ 0 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1$	'1' D	'1' D	'0' 250 ± 50 nsec	'1' D	'1' Ď
VALID READ DATA/CLOCK	1 1 2 3 4 60 msec maximum	$\begin{array}{c} 1'\\ D\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\$	'1' D		'0' • 250 ± 50 nsec		чт Б
VALID READ DATA/CLOCK	$\frac{1}{2}$	$ \begin{array}{c}                                     $	'1' D		'0' • 250 ± 50 nsec	'1' D	'1' δ
VALID READ DATA/CLOCK	I CO msec maximum	$\begin{array}{c} 1'\\ D\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\ 1\\$	'1' D		'0' - 250 ± 50 nsec		-1' δ
VALID READ DATA/CLOCK	I CO msec maximum	$ \begin{array}{c}                                     $	'1' D om		′0′ • 250 ± 50 nsec	'1' D	тт. b
$\frac{VALID READ}{DATA/CLOCK}$	ENABLE IS HIGH real	$\frac{1}{1}$	'1' D om		'0' 250 ± 50 nsec		-1' Δ
VALID READ DATA/CLOCK	ENABLE IS HIGH real	'1' □ □ □ □ □ □ □ □ □ □ □ □ □	'1' D I I I I I I I I I I I I I		′0′ • 250 ± 50 nsec		·τ. δ
VALID READ DATA/CLOCK When WRITE During this time Subject to the	ENABLE IS HIGH real 1 60 msec 1 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	1 1 1 1 1 1 1 1 1 1 1 1 1 1	'1' D		'0' 250 ± 50 nsec		Υ1' Δ
VALID READ DATA/CLOCK $\widehat{\}$ When WRITE $\widehat{\}$ During this tim $\widehat{\}$ Subject to $\pm$	ENABLE IS HIGH real ne interval READ DAT 3.5% speed tolerance.	<pre>'1' D D I I I I I I I I I I I I I I I I I</pre>	'1' D		'0' - 250 ± 50 nsec		-η. b
VALID READ DATA/CLOCK When WRITE 2 During this tim $3$ Subject to $\pm$	ENABLE IS HIGH real ne interval READ DAT 3.5% speed tolerance.	<sup>'1'</sup> □ □ □ <sup>1</sup> <sup>2</sup> <sup>1</sup> <sup>1</sup> <sup>1</sup> <sup>1</sup> <sup>1</sup> <sup>1</sup> <sup>1</sup> <sup>1</sup>	'1' D		'0' 250 ± 50 nsec		·1' δ
VALID READ DATA/CLOCK $\widehat{\}$ When WRITE $\widehat{\}$ During this tim $\widehat{\}$ Subject to $\pm$ $\widehat{\}$ For product acc to $\pm$ 300 nsec b	ENABLE IS HIGH real 1 60 msec 1 4 1 60 msec maximum 1 5 ENABLE IS HIGH real ne interval READ DAT 3.5% speed tolerance.	<pre>'1'</pre>	'1' D I om olied. e ingored. hay be subject		'0' - 250 ± 50 nsec		
VALID READ DATA/CLOCK When WRITE 2 When WRITE During this tim $3$ Subject to $\pm$ A For product acc to $\pm$ 300 nsec b	ENABLE IS HIGH real 1 60 msec 1 4 1 60 msec maximum 1 ENABLE IS HIGH real 1 3.5% speed tolerance. Explance purposes any fit shift from this nomin	1 1 1 1 1 1 1 1 1 1 1 1 1 1	'1' D om om olied. e ingored.		'0' 250 ± 50 nsec		·1' δ

# Figure 5-4 READ DATA TIMING

# 5.5 DISKETTE CARTRIDGE WRITE PROTECT NOTCH

Each flexible disk drive is equipped with a write-protect sensor which prohibits the writing of data on a diskette. A write-protect notch is located on the sealed diskette envelope (see Figure 5-5). Data may be written on such diskettes if the write-protect notch is completely covered by an opaque material such as masking tape. The diskettes shipped with the DDS have masked write-protect notches; removal of the opaque tape will yield a write-protected diskette.

# 5.6 ADDITIONAL INFORMATION

0

Additional information can be obtained from the Customer Maintenance Manual which accompanies each drive.



#### Figure 5-5 DISKETTE CARTRIDGE

#### 出版和目标在目标。如此目标的时代,如何目标在目标的。当时间的组织

**bith fiering disk deite is equiliged quitt a wate protect senser which provides the vertice of settiment of the subsection disks is justified on the texted diskette encoders (see Figure 5-5). Data they be a fille of the set is the entitution of the operative coeffective an uppade sense of the cost of an exacting taxe. The subsector and with the ODE face desired writerecords minimate resource of the controls test will be the well of the subsector a device with the ODE face desired writerecords minimate resource of the controls test will be the other test of the subsector with the ODE face desired writerecords and the test resource of the controls test will be the protector of the subsector test the ODE face desired writerecords and the subsector of the controls test will be the test of the subsector** 

#### HOT ADDITIONAL INFORMATION

3

Additional interactions for the second from the Costoners Maintenance Maintenance Maintenance in the second s



A REAL PROPERTY OF CARTERINGE

## CHAPTER 6

# DISKETTE SYSTEM MICROPROGRAM

## 6.1 INTRODUCTION

The Diskette Operating System microcode consists of 512 words x 32 bits. The bit description can be found in Table 3-2. The microcode is organized functionally as modules. There are two types of modules – primary and subroutine. Primary modules, in general, implement high level functions while subroutines implement specific lower level functions. A specific subroutine may be invoked by many primary modules, but no subroutine can itself invoke another subroutine.

The primary modules within the microcode are as follows:

INIT	-	Initialization
ML	-	Mainline
MAL		Load M.A. Lower
STIO	—	Load M.A. Upper and Start I/O
RR	-	Read Result Byte
IOPB	-	IOPB Loader/Op Decode
FIN	-	I/O Finish
SEEK	-	Seek
FMT	-	Format
REC	-	Recalibrate
VERF/RD	_	Verify/Read
WDEL/WT	la <del>nne</del>	Write Deleted/Write

The subroutine modules within the microcode are as follows:

CHKR		Address Parameter Checker
INC		Read Next Memory Word
WDAT	-	Write Data Field
WCURR		Write Current Check
то	-	Time Out
AM		Address Mark Detect
MVR	_	Head Stepper
TNIBS	-5-	Read Disk Byte
ID		Process Address (ID) Field
WADD	-	Write Address Field

The following conventions will be used throughout:



# 6.2 MICROPROGRAM MODULE DESCRIPTION

The following flow charts describe each module in detail.

#### CRAPTER 6

#### HARDDRIDE BY STREEM MICHOLICE IN TRADER

The Deletite Christian Excession methodes consists of 612 weeks x 32 bits. The DR discription can in Galadian Fature 32. The mightends is organized functionally as modules. There are two types of motories who conversion from y modules in general implementation that tends functions while submotations implificant structure convertion, as A specific relationing any to invende by many transitive methods, but no submotations in the transition of motories and the structure of the point of the first in the invented by many transitive methods. But no submotations in the transition of the structure of the structure of the many be invented by many transitive methods. But no submotations in the transition of the structure of the struct

swolida is for application out would write a function for a longer

4

3

9

15



to faillowing dataset from tell he bent filmouthed



Figure 6-1 INITIALIZATION



 $\dot{a}$ 

- 7

# Figure 6-2 MAINLINE

6-3







3

-

a.

# Figure 6-4 LOAD MA UPPER AND START I/O



20

.

# Figure 6-5 READ RESULT BYTE



Figure 6-6 IOPB LOADER/OP DECODE

ŝ,





2



Figure 6-8 SEEK



Figure 6-9 FORMAT



Figure 6-9 FORMAT (CONTINUED)

4



# Figure 6-10 RECALIBRATE






Figure 6-11 VERIFY/READ (CONTINUED)



Figure 6-12 WRITE DELETED/WRITE



Figure 6-13 ADDRESS PARAMETER CHECKER



Figure 6-14 READ NEXT MEMORY WORD



Figure 6-15 WRITE DATA FIELD



Q

6

# Figure 6-16 WRITE CURRENT CHECK



Figure 6-17 TIME-OUT





-









Figure 6-21 PROCESS ADDRESS FIELD



## Figure 6-22 WRITE ADDRESS FIELD

2



÷

10.

0

φ.

(L)314 就的有能能 新有部群。\$\$\$4 ennet

85.4

## CHAPTER 7

# UTILIZATION

This chapter provides the necessary information to install and fully utilize the capabilities of the Diskette System. In installing the Diskette System, consider the following:

- 1. Environmental extremes
- 2. Mounting recommendations
- 3. Electrical connections
- 4. Base address selection
- 5. Interrupt level selection

The following sections of this chapter will deal with these considerations.

#### 7.1 ENVIRONMENTAL EXTREMES

Temperature extremes can cause instability, or result in permanent damage to the circuits or the drive mechanisms. Ambient temperature must therefore be maintained within the limits of  $50^{\circ}$  to  $100^{\circ}$ F ( $10^{\circ} - 38^{\circ}$ C), 20% to 80% relative humidity with maximum wet bulb temperature of  $80^{\circ}$ F.

Exercise caution in locating the system, giving particular attention to radiant and conductive sources of heat. Remember that the system itself will contribute some heat to the environment (314 BTU/hour for each diskette drive). Provide adequate ventilation to permit the convective dissipation of heat from the system components.

#### 7.2 MOUNTING RECOMMENDATIONS

**Controller:** The Channel Board and Interface Board (jointly referred to as the diskette controller) are to be inserted inside the INTELLEC System cabinet. Both boards are designed to plug directly into three standard PC-edge connectors. An 86-pin connector and a 60-pin connector are located on the bottom edge of the board and plug into the mother-board assembly. A 100-pin connector is on the opposite edge of the boards. The connectors serve as a mounting, as well as an electrical junction (see Section 7.3). Additional protection is provided by the guide slots in the INTELLEC System cabinet. The Channel and Interface Boards are each 12.00'' x 6.75''.

Before the controller boards are installed, the 60-pin dual auxiliary connector (1000515) must be installed in the INTELLEC System cabinet. The controller boards then plug in with the Interface Board in an <u>ODD</u> numbered slot and the Channel Board in an <u>EVEN</u> numbered slot.

**Diskette Drive(s):** The diskette drive(s) arrive in the diskette enclosure with their own power supply. No mounting is required.

#### 7.3 ELECTRICAL CONNECTIONS

The Channel and Interface Boards each communicate with the INTELLEC System bus through a standard 86-pin doublesided PC edge connector (P1), 0.156" contact centers (see Figure 7-1). CONTROL DATA CORPORATION'S VPB01E43A00A1 is one suitable type of connector for P1. The two controller boards communicate with each other via a 60-pin, double-sided PC edge connector, 0.1" contact centers (see Figure 7-1). CDC97169001 is one suitable type of connector for P2. Both boards also include a 100-pin, double-sided PC edge connector (J1), 0.1" contact centers (see Figure 7-1). VIKING 3VH50/1JN5 is one suitable type of connector for J1. The Channel Board only uses its J1 connector as a means of accessing various test points on the board. The Interface Board, however, communicates with the diskette drive(s) via its J1 connector. The Interface Board's J1 connector also allows access to various test points. Pin allocations for each of the connectors on the Interface Board are provided in Section 4.3. The same information for the Channel Board is provided in Section 3.3.

The 'Floppy Disk Controller Cable' (supplied with the Diskette System) plugs into the J1 connector on the Interface Board. The other ends of the Controller Cable should be attached with the screws provided to the bulkhead on the back panel of the INTELLEC System cabinet. The 'Floppy Disk Peripheral Cable' should be attached to the drive enclosure and to J8 of the Controller Cable. To add an additional system drive enclosure (four drives total), plug a second 'Floppy Disk Peripheral Cable' onto the additional drive enclosure and to J10 of the Controller cable. All necessary cables are supplied with the equipment. Controller cable connector J8 interfaces to logical drives '0' and '1'. J10 interfaces to logical drives '2' and '3'.

The Diskette enclosure also includes an AC power cord which must be plugged into a convenient AC source.

**CAUTION:** The Diskette enclosure is shipped from the factory as either a 110V/60Hz system or 220V/50Hz system. Consult the shipping list and customer letter before plugging in the AC line cord. Using incorrect line voltage/frequency results in improper operation and potential damage to the diskette drives.

#### 7.4 BASE ADDRESS SELECTION

The user must assign a base address to the Diskette Channel. The base address is defined by the five most significant bits of the eight-bit I/O port address. The three least significant bits, then, can be used to differentiate between eight input or eight output channel commands. When the CPU accesses the Diskette Channel by executing an I/O instruction the base address (BASE) is used to select the Diskette Channel, while the three low-order address bits select one of the channel commands, as described in Chapter 2.

A base address is assigned by opening or closing the five most significant switch positions of the S1 switch (S1 - 4, 5, 6, 7, 8) on the Channel Board (see sheet 1 of the Channel Board schematic in Section 3.3). When a switch position is closed (on) (tied to ground) it represents the assignment of a logical 0 address bit. When a position is open (off) (+5V), it represents a logical 1 selection.

The following sketch represents a base address selection of 7816.





If the controller is to be used in conjunction with ISIS, the Diskette System software driver, the base address must be set to the value used with ISIS. This value is  $78_{16}$ .

## 7.5 INTERRUPT LEVEL SELECTION

The user can assign the Diskette Channel's interrupt request line to any one of eight interrupt priority levels (INTO/ – INT7/) by moving the interrupt level select switch (S1) on the Interface Board to the desired position. This eight

position rotary switch is shown on sheet 3 of the Interface Board schematic in Section 4.3. The eight switch positions are associated with the following priority levels:

SWITCH POSITION	INTERRUPT PRIORITY LINE	RELATIVE PRIORITY (INTELLEC MDS SYSTEM)
1	INTO/	HIGHEST
2	INT1/	1
3	INT2/	
4	INT3/	
5	INT4/	
6	INT5/	
7	INT6/	*
8	INT7/	LOWEST

The following sketch shows the switch setting 3 corresponding to priority line INT2/.



If the controller is to be used in conjunction with ISIS, the interrupt level section must be compatible with that used by ISIS. This value is switch setting 3.



Figure 7-1 CONNECTORS ON THE CHANNEL AND INTERFACE BOARDS

**Billion totily enrol**est shown on them 3 of the Interface Board shereas, is to line to The right will be interface we associated with the following priority levels

The tallowing shatch allows the swerch without 3 correspondence to evanety (i.e. 1975)



Periodian auto in takin in conjunctions with USE the instrume level sector main instrumentantly and the instrument in the constant of the instrument of t



PORTAGE OR THE CHARGES IN THE CHARGES AND STREET ACE TO APDS

# CHAPTER 8

# **OPERATING CHARACTERISTICS**

This chapter provides AC and DC characteristics for all signals not internal to the Diskette System modules. These signals include the INTELLEC bus signals as well as the drive interface. Refer to the appropriate tables and figures for the desired rating.

## 8.1 AC CHARACTERISTICS

Tables 8-1 and 8-2 give the AC characteristics for the Diskette System boards.

PARAMETER	OVERALL MIN(NS) MAX(NS)	DESCRIPTION	REMARKS
<sup>t</sup> SAS	50	Address Setup Time to I/O Command	Provided by Host CPU
tSDS	0	Data Setup Time to I/O Command	Provided by Host CPU
<sup>t</sup> SAH	0	Address Hold Time from I/O Command	Provided by Host CPU
<sup>t</sup> SDHW	0	Data Hold Time from I/O Command	Provided by Host CPU
<sup>t</sup> SDHR	25	Read Data Hold Time from I/O Command	Provided by Flexible Disc Controller (FDC)
<sup>t</sup> ACC	Bus Timeout	I/O Access Time	Provided by FDC
<sup>t</sup> XKD	7	XACK Delay from Read Data	Provided by FDC
<sup>t</sup> XKO	30	XACK Hold Time from I/O Command	Provided by FDC
<sup>t</sup> BCY	100	Bus Clock Cycle Time	Provided by CPU
<sup>t</sup> BW	25	Bus Clock Low and High Periods	Provided by CPU
TCCY	100	Common Clock Cycle Time	Provided by CPU
<sup>t</sup> CW	25	Common Clock Low and High Periods	Provided by CPU
<sup>t</sup> DRQ	35	Bus Request Delay	10.0
<sup>t</sup> DBY	65	Bus Busy Turn on Delay	Salar -
<sup>t</sup> DBYF	40	Bus Busy Turn off Delay	
<sup>t</sup> DBPN	30	Priority Input Setup Time	
<sup>t</sup> DBPO	20	BPRO/ Serial Delay from BPRN/	
<sup>t</sup> DB	50	Busy to Address/Data Delay	

Table 8-1 DISKETTE SYSTEM/INTELLEC BUS AC CHARACTERISTICS

# OPERATING CHARACIERSING

#### OVERALL PARAMETER DESCRIPTION REMARKS MIN(NS) MAX(NS) Address/Data Setup to Command tAS, DS 60 XACK to Command Turn Off <sup>t</sup>XKCO 35 125 <sup>t</sup>AH Address Hold Time 115 Data Hold Time <sup>t</sup>DHW 125 Provided by Memory 0 Read Data Hold Time <sup>t</sup>DHR Module (Slave) tBS Bus Sample Delay Time 200

# Table 8–1 DISKETTE OPERATING SYSTEM INTELLEC BUS AC CHARACTERISTICS (CONTINUED)

USD INTER WE SEE STUDIES

have a second





# Figure 8-2 BUS EXCHANGE TIMING



Figure 8-3 MASTER COMMAND TIMING

D

61

		OVERALL		DESCRIPTION		
PARAMETER	MIN	ТҮР	MAX	DESCRIPTION		
tSCYS	8 msec	10 msec	12 msec	Step Cycle Time		
<sup>t</sup> SPW	1. T	10 usec		Step Pulse Width		
<sup>t</sup> LSET		60 msec		Settling Time – Select to Data		
<sup>t</sup> SSET		20 msec		Settling Time – Step to Data		
<sup>t</sup> RDPW	200 nsec	250 nsec	300 nsec	Read Data Pulse Width (Rd)		
<sup>t</sup> CELL		2 usec	12 1	Bit Cell Time		
twdpw		250 nsec	1 hourses	Write Data Pulse Width (Wt)		
<sup>t</sup> NXPW		1.5 msec		Index Pulse Width		
<sup>t</sup> NXCY		166.7 msec		Index Cycle Time		
<sup>t</sup> WFPW	2 usec	1	2.8 usec	Write Fault Reset Pulse Width		

# Table 8-2 DISKETTE SYSTEM/DRIVE INTERFACE AC CHARACTERISTICS



Figure 8-4 STEP/SETTLING TIMINGS

6





## 8.2 DC CHARACTERISTICS

The following two tables (8-3 and 8-4) give the DC characteristics for the Channel and Interface Boards. Both the INTELLEC bus and drive interface are included. The values are derived from manufacturers' specifications and calculated values if passive loading exists. Capacitance values are approximations.

Power requirements for the boards are as follows:

	Vcc(+5VDC±5%)		-10	VDC	
	TYP	MAX	TYP	MAX	
CHANNEL BOARD	3.75A	5.0A	21	_	
INTERFACE BOARD	1.5A	2.5A	100mA	200mA	
TOTAL	5.25A	7.5A	100mA	200mA	

#### Table 8-3 DISKETTE OPERATING SYSTEM DC CHARACTERISTICS (INTELLEC BUS)

		PARAMETER	TEST	PARAMETER		
SIGNAL	SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNITS
ADRF/-ADR8/	VOL	Output Low Voltage	I <sub>OL</sub> =10mA		.45	V
	V <sub>OH</sub>	Output High Voltage	IOH=-1mA	2.4		V
	С	Capacitive Load			15	pf
ADR7/ - ADRØ/	VOL	Output Low Voltage	I <sub>OI</sub> =15mA		.45	V
	VOH	Output High Voltage	IOH=-1mA	3.65	20100	V
	VIL	Input Low Voltage			.8	V
	VIH	Input High Voltage		2		V
	IIL I	Input Current at VIL	V <sub>11</sub> = .4V		-1.6	mA
	Чн	Input Current at VIH	VIH=2.4V	Mag	40	uA
	С	Capacitive Load	- Andra		15	pf
DATF/ - DAT4/	VOL	Output Low Voltage	I <sub>O1</sub> =15mA	.11 <sup>2</sup>	.45	V
	VOH	Output High Voltage	IOH=-1mA	3.65		V
	VIL	Input Low Voltage		- J.3*	.85	V
	VIH	Input High Voltage	a me trant.	2		V
	IL I	Input Current at VIL	V11 = .45V		25	mA
	Чн	Input Current at VIH	VIH=5.25V		10	uA
	с	Capacitive Load	in al fught 0	211V 239	15	pf
DAT3/ - DATØ/	VOL	Output Low Voltage	IOI =15mA	A	.45	
	VOH	Output High Voltage	IOH=-1mA	3.65		V
	VIL	Input Low Voltage	PRO REMARK		.85	V
	VIH	Input High Voltage	e Hanasa - Ta	2		V

		PARAMETER	TEST	P	ARAMET	R
SIGNAL	SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNITS
	ΙL	Input Current at VIL	V <sub>IL</sub> = .45V		25	mA
	Чн	Input Current at VIH	V <sub>IH</sub> =5.25V		10	uA
	C	Capacitive Load	Street and Astron		15	pf
	Condition 1		104.9.45.57145			
BCLK/	VIL	Input Low Voltage			.8	V
CCLK/	VIH	Input High Voltage	JAIOT	2		V
	1 <sub>IL</sub>	Input Current at VIL	$V_{IL} = .4V$		-2	mA
	Чн	Input Current at VIH	V <sub>IH</sub> =2.4V		50	uA
	С	Capacitive Load			15	pf
	- 1		221. Deeptor del 1	1.22.24	-10-8 plan	
BPRN/	VIL	Input Low Voltage	the second second		.8	V
	VIH	Input High Voltage	S. 49.53	2		V
	IIL	Input Current at VIL	$V_{IL} = .4V$		-3.2	mA
	Чн	Input Current at VIH	V <sub>IH</sub> =2.4V	a selection	80	uA
	C	Capacitive Load	The state of the s		15	pf
IORC/, IOWC/	VIL	Input Low Voltage	elaza a	1350 °	.8	V
INIT/	VIH	Input High Voltage		2		V
	ηL	Input Current at $V_{IL}$	V <sub>IL</sub> = .4V	and a	-1.6	mA
	Чн	Input Current at VIH	V <sub>IH</sub> =2.4V		40	uA
	C	Capacitive Load	and the second	and a second	15	pf
			And the stand of the	1		
XACK/	VOL	Output Low Voltage	I <sub>OL</sub> =16mA		.4	V
	VOH	Output High Voltage	I <sub>OH</sub> =-5.2mA	2.4		V
	VIL	Input Low Voltage	a second		.8	V
	VIH	Input High Voltage		2		V
	IIL I	Input Current at VIL	$V_{IL} = .4V$	1.25	-1.6	mA
	ЧН	Input Current at V <sub>IH</sub>	V <sub>IH</sub> =2.4V	Ser. Y	40	uA
	LL	Input Leakage Low	High Z V <sub>o</sub> =2.4	V	-40	uA
	LH	Input Leakage High	High Z V <sub>0</sub> = .4	V	40	uA
	С	Capacitive Load	States - Black		15	pf
5000 /			a mad a caref	341		
RNKO/	VOL	Output Low Voltage	OL=3.2mA		.45	V
	<sup>V</sup> OH	Output High Voltage	OH=400uA	2.4		V
	C	Capacitive Load	Walt too ist.	154	15	pf
BREQ	Voi	Output Low Voltage	lou =20mA	104	.45	v
	VOH	Output High Voltage	Iоц=400uA	2.4		V
	C	Capacitive Load	Un		15	of

# TABLE 8-3 (CONTINUED)



CICNIAL	01/1000	PARAMETER	TEST CONDITION	PARAMETER		
SIGNAL	SYMBOL	DESCRIPTION		MIN	MAX	UNITS
SELØ/, SEL1/	VOL	Output Low Voltage	I <sub>OL</sub> =48mA		.4	V
SEL2/, SEL3/	ЮН	Output High Leakage	Open Collector	1.		internet i
			Off V <sub>OH</sub> =5.5V		250	uA
WRT DAT/	С	Capacitive Load			15	pf
WRT GT/						
STEP/	A.1	S. Marken and S. Marken	1910 B 19			128-1
DIR/	10.0	and the second	ing of the			
WRT FLT						
RESET/						1
TRACK GT	An	Strand Contract of Strand	when when		11	of the F
43/		the state of the state	topul"			
READY Ø/	VIL	Input Low Voltage			.8	V
READY 1/	V <sub>IH</sub>	Input High Voltage	1 i i i	3.0		V
SEP DATA/	IIL.	Input Current at VIL	V <sub>11</sub> = .8		-26	mA (2)
SEP CLOCK/	- IIH	Input Current at VIH	V <sub>IH</sub> =3.0		10	mA (1)
TRACK Ø/	С	Capacitive Load			15	pf
INDEX/						
WRT FLT/	_			1		1
WPROT/						
LEDØ/	VOL	Output Low Voltage	IOL=16mA		.4	V
LED1/	VOH	Output High Voltage	I <sub>OH</sub> =400ua	2.4		V
	С	Capacitive Load			15	pf

# Table 8-4 FDCC DC CHARACTERISTICS (DRIVE/DISPLAY INTERFACE)

5

(1) Includes 9.1mA due to  $220/330\Omega$  pull-up/pull-down.

(2) Includes 25mA due to  $220/330\Omega$  pull-up/pull-down.

