NCR 8418 Card

Technical Reference Manual

Preface

This manual describes the NCR 286 Card (to be referred to as processor board) and its interfaces. Both the power-fail recovery (PFR) card and the non-power fail recovery (NPFR) card descriptions are included in this publication. The Card supports three processing speeds, 6.0MHz, 8.0MHz, and 10.0MHz, and allows operation at two speeds. The speed is user selectable and may be set to either 6.0MHz and 8.0MHz or 6.0MHz and 10.0MHz depending on the processor board. The default speed is 6.0MHz for both boards. The higher speed is determined by the frequency of the crystal oscillator. The 6/8 board has a 16.0MHz crystal and the 6/10 board has a 20.0MHz crystal. These boards utilize NCR's split board architecture (SBA), in which major system components are placed on different pluggable cards.

The information in this publication is for reference and is intended for system integrators and anyone else who needs to understand the design of the NCR 286 Cards.

This manual consists of eight chapters:

- The first chapter gives general information about the board including its physical dimensions, electrical, environmental, and safety characteristics, and shipping considerations.
- The second chapter gives the functional description of the board's main components and describes its interfaces, system timing, address maps, and connectors.
- Chapter three contains information on switch settings, jumper strappings, and adjustments.
- Chapter four describes level 0 diagnostics.

- Chapter five contains pin-outs for the main components on the board.

- Chapter six contains board specifications information.
- Chapter seven contains logic diagrams.
- Chapter eight contains the 80286 instruction set.

286 Card Technical Reference

Chapter 1 General Information

Chapter 2 Functional Description

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General Information

General Information

INTRODUCTION

The processor board is an IBM-PC/AT-compatible single-board computer card that uses split board architecture (SBA). The board, designed for modularity and flexibility, is functionally PC/AT compatible in terms of processor speed, input/output port assignments, memory configuration, and expansion-bus interface.

The board is designed on the PC/AT peripheral card form factor using state-of-the-art application-specific integrated circuits (ASIC), very large-scale integration (VLSI) technology, and surface-mount technology (SMT). Figures 1-1 and 1-2 show the location of the components on the board. Features of the processor board are:

- Intel 80286 Microprocessor
- DMA - 7 channels
- Three programmable timers
- ROM memory - 128KB
- 24-bit address bus
- 1GB virtual memory
- Keyboard port
- Software speed switching
- User selectable wait state
- LED speed indicator
- Battery backup
- Base memory expansion to 640KB
- Multiple VLSI chips
- Pipelined bus interface
- Real-Time Clock (RTC)
- 16-level interrupt
- RAM memory - 512KB
- 16-bit data bus
- 16MB real memory
- PC/AT compatible ROM BIOS
- 80287 coprocessor socket
- System clock
- Keyboard entry lockout
- Speaker - volume control
- PC/AT-standard peripheral card size

PHYSICAL DESCRIPTION

The processor board is a 4.8-inch by 13.15-inch, multilayered printed circuit board. It is an industry-standard PC/AT card-sized board.

The key operating component is the INTEL 80286-10 16-bit microprocessor (U43) located on the right side of the board. Other major components on the card include:

Right side of board:

- DRAM VLSI (NPFR board U72, PFR board U71)
- 80287 math coprocessor socket (U44)

Center of board:

- CPU VLSI (U39)
- 8259A-2 Interrupt Controllers (2) - NPFR U68,U69/PFR U67,U68
- 8237-5 DMA controllers (2) - U55,U66
- DMA page register - 74LS612 (U38)
- ROM BIOS low byte (U30)

Left side of board:

- Real-Time Clock (RTC) VLSI (U63)
- 8742 Universal Peripheral Interface (U37)
- ROM BIOS high byte (U27)

DC power is supplied to the board through the bus connector located on the bottom right of the board near the DRAM VLSI chip.

Mounted near the RTC VLSI chip are two adjustable capacitors: VC1 to trim the 14.318MHz clock and VC2 to trim the 32.768KHz crystal for the Time of Day clock.

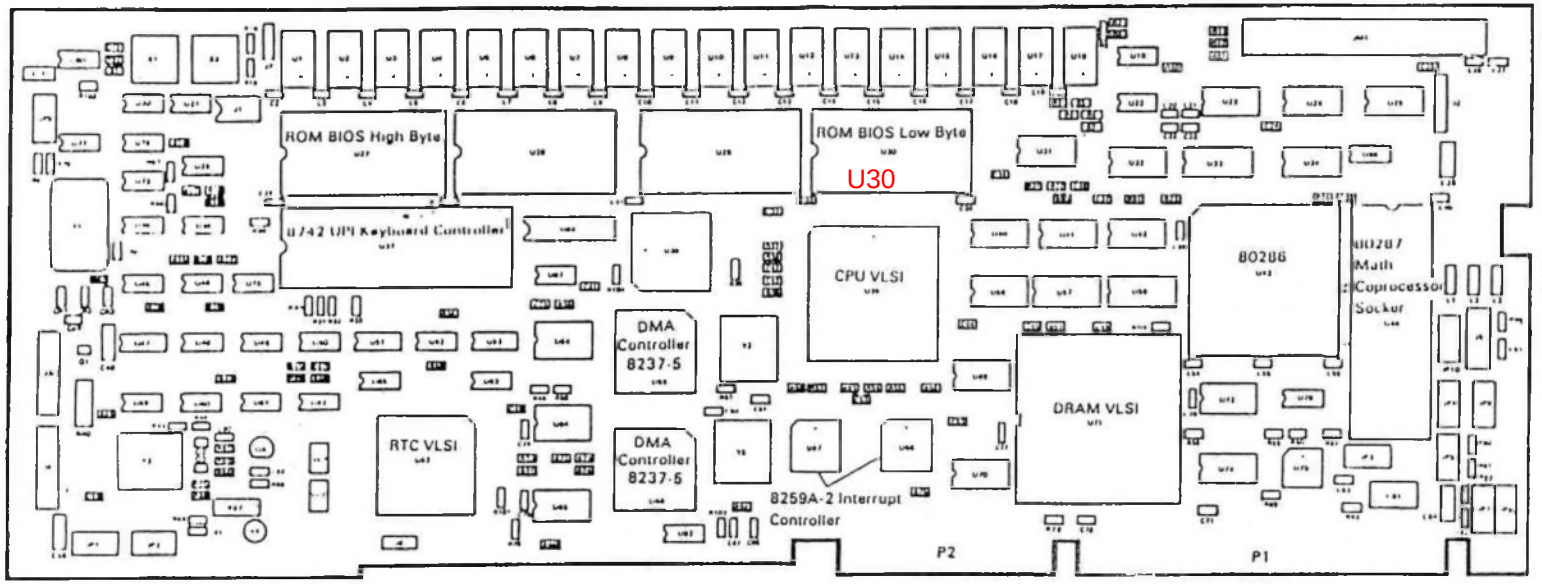

Figure 1-1 Power fail recovery processor board layout (PFR)

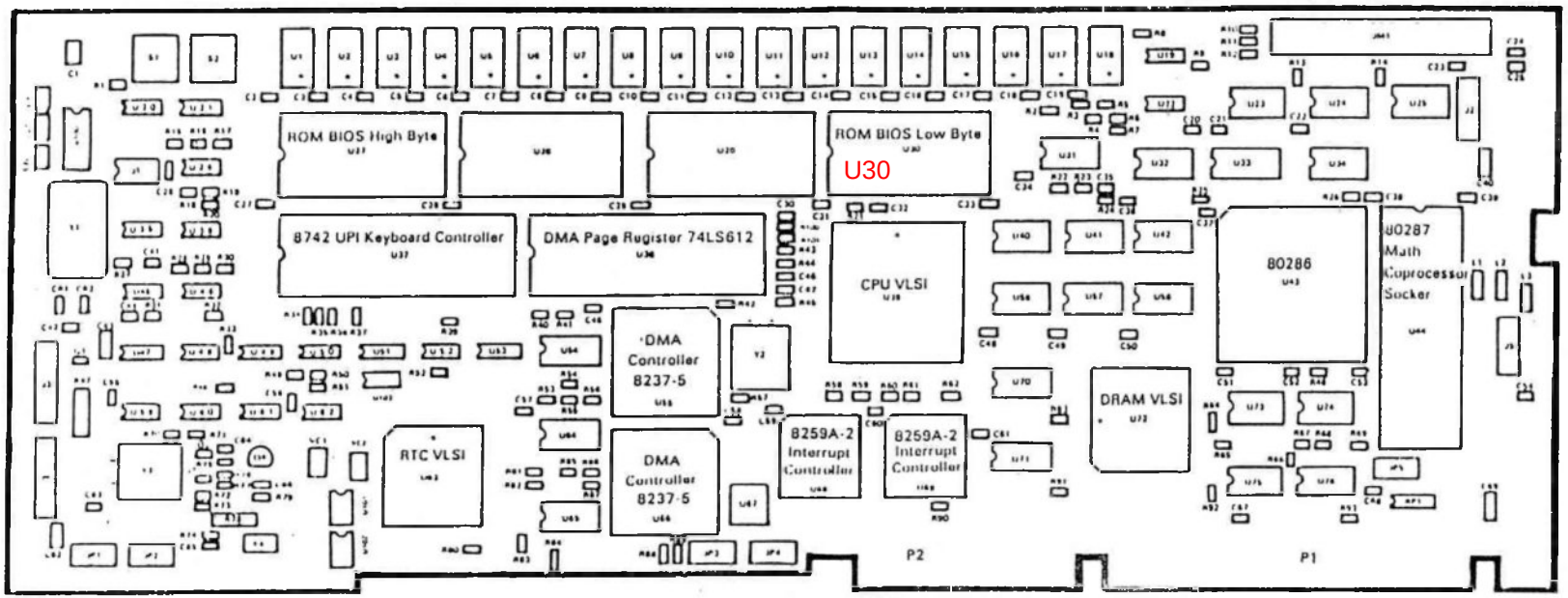

Figure 1-2 Non-power fail recovery board layout (NPFR)

Also on the board are connectors for the following:

- 6-pin 8-ohm speaker (J4)
- 5-pin battery back-up (PFR), 4-pin (NPFR) - RTC/CMOS configuration table (J2)
- 6-pin keyboard lock/LED speed indicator (J3)
- 10-pin keyboard/power good (J5)
- 36-pin expansion RAM (JM1)

Below the Interrupt controller chip area are two board-edge bus connectors:

- 62-pin 8-bit I/O bus signal interface (P1)
- 36-pin 16-bit I/O bus signal interface (P2)

Also on the board are two banks of dynamic RAM. Each bank consists of nine chips; eight chips are for data and the ninth is for parity. These chips provide 512KB of base memory. RAM memory may be increased 128KB for a maximum of 640KB base memory.

ELECTRICAL CHARACTERISTICS

DC power is provided to the board through the bus connector. Figure 1-3 shows the power input connector pin-outs.

Pin	Voltage
B3	+5 volts
B29	+5 volts
D16	+5 volts
B1	Ground
B10	Ground
B31	Ground
D18	Ground

Figure 1-3 Power connector pin-outs

CURRENT REQUIREMENTS

The current requirements are shown in Figure 1-4. Maximum current indicates a fully populated system board, including an 80287 math coprocessor and two extra EPROMs.

Voltage	Voltage Tolerance	Typical Current	Maximum Current
+12v*	+-10%	0.0 mA	0.0 mA
+ 5v	+- 5%	2.25 A	3.0 A
- 5v*		0.0 mA	0.0 mA
-12v*	+-10%	0.0	0.0 mA

* -5,+12 and -12 volts are not used by this board.

Figure 1-4 Current requirements

ENVIRONMENTAL CHARACTERISTICS

The processor board withstands various environmental conditions during normal operation, shipment, storage, and handling as specified in Figure 1-5.

RANGE	DRY BULB TEMPERATURE	RELATIVE HUMIDITY	BAROMETRIC PRESSURE
Operating	10 C to 55 C 10 C Change per hour	20% to 80% 10% Change per hour	105 to 69,000 Pascals up to 9850 ft.
Extreme Power On*	0 C to 60 C 10 C Change per hour	10% to 95% w/o condensation	Same for all ranges.
Storage	-10 C to 50 C 15 C Change per hour	10% to 90% w/o condensation	
Transit	-40 C to 60 C 20 C Change per hour	5% to 95% w/o condensation	

* NOTE: The extreme power-on range indicates limits which are likely if the heating or air conditioning plant fails or has not yet brought the room to operating conditions.

Figure 1-5 Environmental characteristics

SAFETY CHARACTERISTICS

The board is constructed of UL recognized material and processed by a UL recognized etching house. The board meets 94V2 flammability rating and is marked in accordance with UL procedures.

FCC NOTICE

The processor board, when operating in the final product configuration, is subject to FCC part 15J (USA) and/or FTZ (Germany) measurements of conducted and radiated radio frequency emissions, depending on the product classification. The board, as delivered, is neither Class A VERIFIED nor Class B CERTIFIED. The final product must be tested to establish its compliance with the applicable emissions regulations.

SOCKET-MOUNTED COMPONENTS

The processor board contains the following socket-mounted components:

- ROM BIOS chips (U27,U30)
- Keyboard Controller (U37)
- 80286 Microprocessor (U43)
- DRAM Controller VLSI (U71)

The pin assignments for these components are shown in the "Integrated Circuit Component Pin-out Configuration" section.

SHIPPING CONSIDERATIONS

The board will withstand the following vibrations without any detrimental effects to its operation or life expectancy:

- Frequency — 7 to 100 HZ
- Force — 1.2 G's, minimum
- Time — 2.5 hours
- Shock — 30 G's in any plane with no surrounding protective package.

REFERENCES

- Intel Corporation:
  - *Microsystem Components*, volumes I and II
  - *Memory Components Handbook*
  - *Microprocessor and Peripheral Handbook*
  - *Introduction to the iAPX 286*
  - *iAPX 286 Hardware Reference Manual*
  - *iAPX 286 Programmer's Reference Manual*
  - *iAPX 286 Operating Systems Writer's Guide*
- Texas Instruments:
  - *MOS Memory Supplement*
- Motorola, Incorporated
  - *Microprocessors Data Manual*

Functional Description

Functional Description

PROCESSOR BOARD

This section contains a functional description of the processor board. The major functions, as shown in Figure 2-4, described are:

- 80286 Microprocessor control
- DRAM VLSI control
- CPU VLSI control
- Real-Time Clock VLSI control
- DMA control
- Interrupt control
- 80287 Numeric Processor control
- Keyboard control
- ROM control
- RAM control
- Addressing
- Connector signal control

80286 MICROPROCESSOR

The central processing unit (U43) is an INTEL 80286-10. It has a clock rate of 6.0MHz, 8.0MHz, or 10.0MHz. The clock rate may be selected through the DOS FREQ utility or the keyboard by pressing ALT, ESC, and SYS REQ simultaneously. Proper jumper strapping is required for the selected speed; refer to the *Switches, Jumpers, and Adjustments* chapter of this manual.

Two upwardly compatible operating modes are supported: the real address mode and the protected virtual address mode. The real address mode of the 80286 allows a 1 MB address space. In protected mode, a 16 MB real address space with 1 GB virtual addressing per task is supported.

The processor board also supports an 80287 high performance 80-bit math coprocessor.

A comparison of overall system performance showing wait states and cycle times for the different operating speeds is shown in Figure 2-1.

CYCLE TYPE	CPU CLOCK CYCLE	WAIT STATE	6 MHz CYCLE TIME	8 MHz CYCLE TIME	10 MHz CYCLE TIME	8 MHz 0 MEMORY WAIT STATES
16 BIT BUS	2	1	500ns	375ns	300ns	250ns BASE
	2	0				250ns MEMORY
16 BIT BUS	2	1	500ns	375ns		375ns EXPANSION
	2	2			400ns	375ns MEMORY
8 BIT TO	2	4	1000ns	750ns		750ns
8 BIT I/O		6			800ns	
16 BIT TO	2	10	2000ns	1500ns		1500ns
8 BIT I/O		14			1600ns	
16 BIT TO	2	1	500ns	375ns		375ns
16 BIT I/O		2			400ns	

Figure 2-1 System performance

RANDOM ACCESS MEMORY (RAM)

The processor board has two banks, 512K bytes, of dynamic RAM (U1-U18). Each bank consists of eight chips for data and one for parity checking.

RAM memory may be increased to a maximum of 640K bytes by inserting a 128K expansion board into one of the expansion slots or by using the 128K expansion connector (JM1) on the processor board with the 128K piggyback board. Additional memory may be added in the form of RAM expansion cards.

The dynamic RAM memory is refreshed using the DRAM VLSI, the CPU VLSI and counter 1 of the timer. Refresh requires one memory cycle every 15 microseconds. In power-down operation, a strap allows the memory to be refreshed at a slower rate, to conserve power.

Single bit errors are detected using a ninth bit for parity. A parity error generates a non-maskable interrupt to the 80286 CPU.

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8 BIT TO 8 BIT I/O	2	4	1000ns	750ns		750ns
		6			800ns	
16 BIT TO 8 BIT I/O	2	10	2000ns	1500ns		1500ns
		14			1600ns	
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READ ONLY MEMORY (ROM)

The processor board has four sockets, U27 - U30, for ROM or erasable-programmable-read-only memory (EPROM). Each socket accommodates 27128 (16k x 8) or 27256 (32k x 8) memory chips. Refer to Figures 1-1 or 1-2 for the location of the four ROM/EPROM sockets.

The top 64K of memory, F0000(H) to FFFFF(H) real mode (1M total system memory), and FF0000(H) to FFFFFF(H) protected mode (16M total system memory) are reserved for ROM BIOS. The address map for the ROMs is shown in Figure 2-3. At 6.0 MHz a ROM memory cycle is 375ns and the data access time is 200ns. With the 10 MHz option enabled ROM memory cycles are 300ns and data access time is 180ns.

ADDRESS	DEVICE DESIGNATION
0E0000 TO 0EFFFF	Reserved ROM memory space
0F0000 TO 0FFFFF	BIOS ROM memory space
FE0000 TO FEFFFF	Reserved ROM memory space
FF0000 TO FFFFFF	BIOS ROM memory space

Figure 2-3 ROM address map

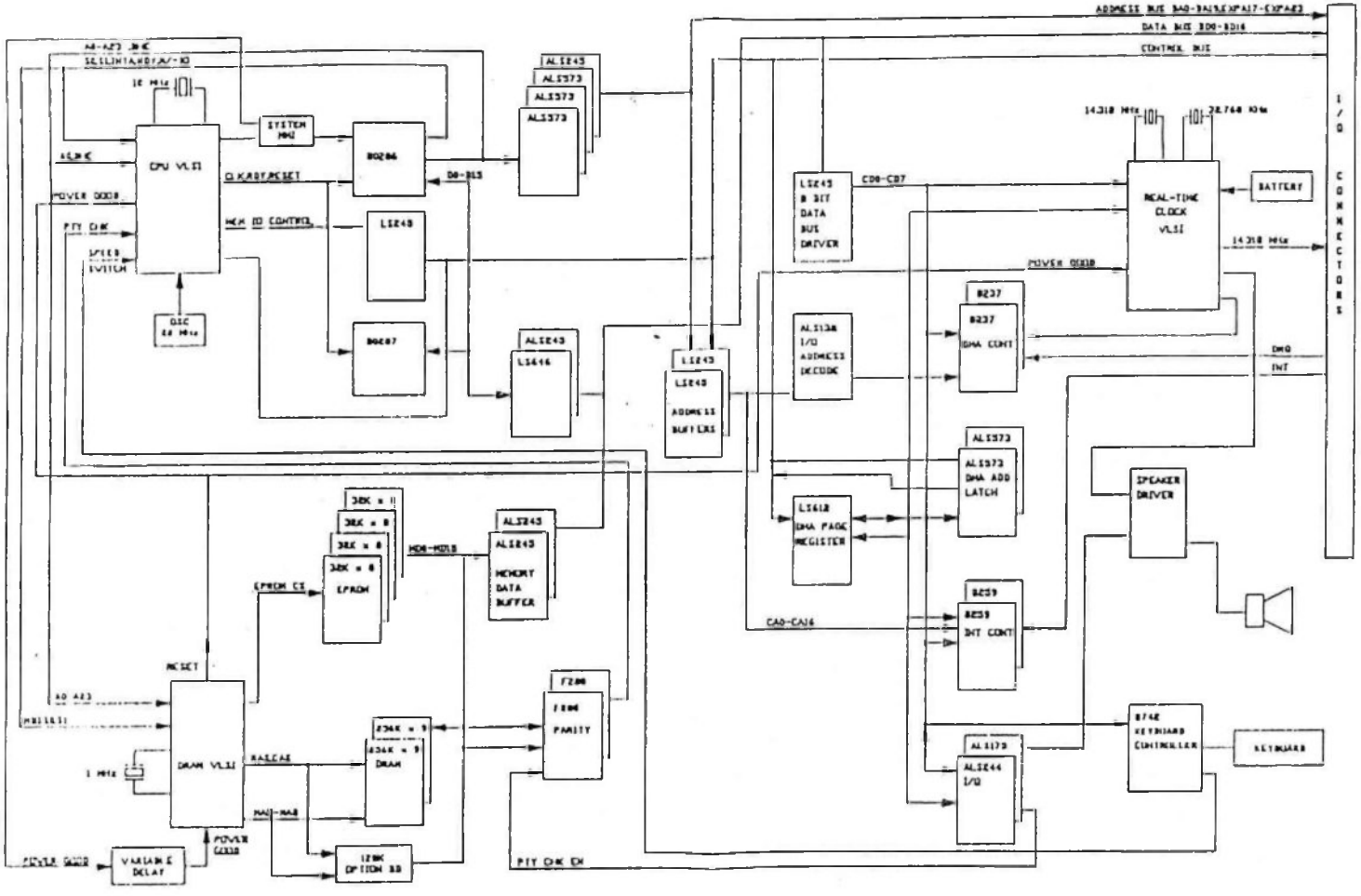
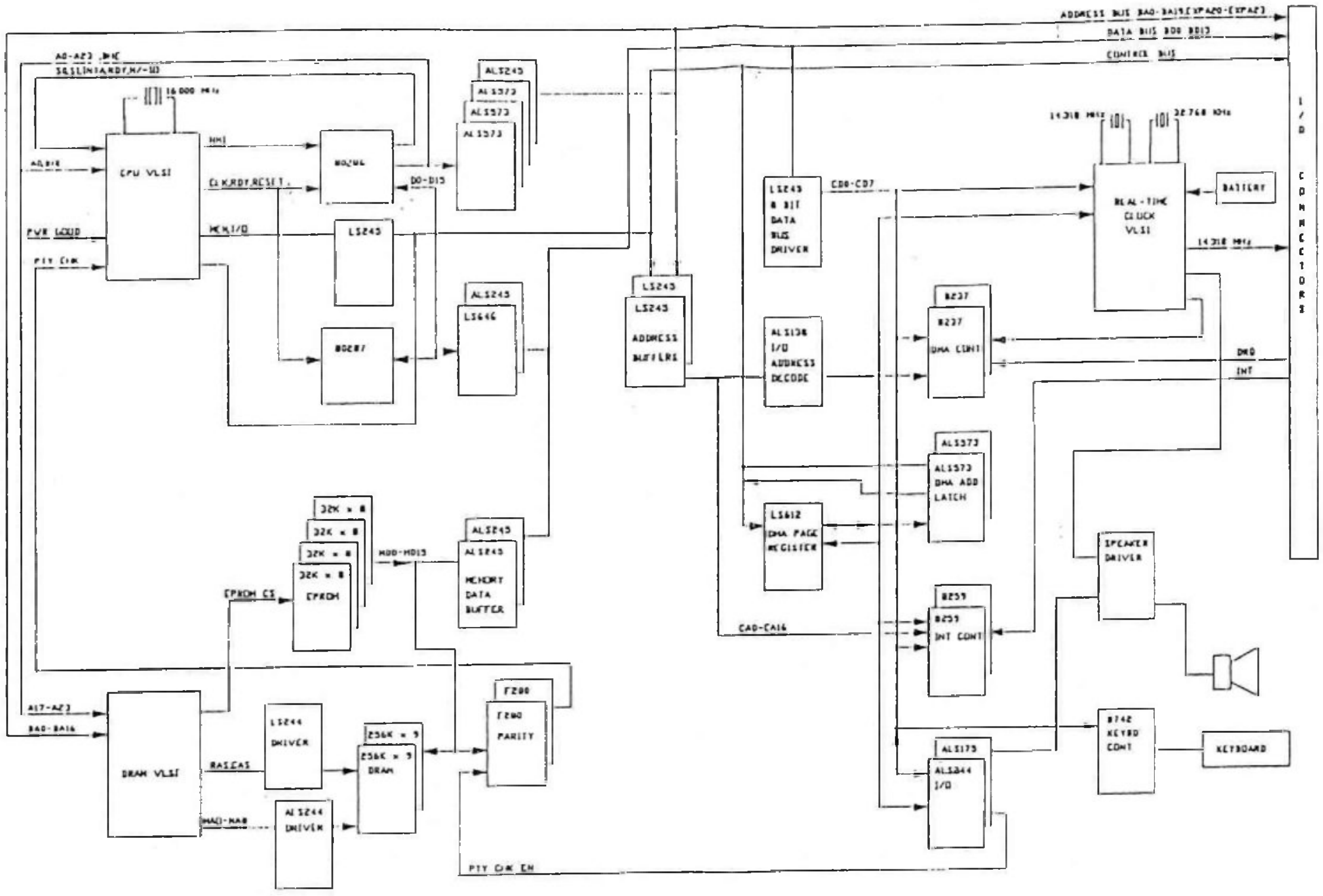


Figure 2-4 Power fail recovery board functional block diagram (PFR)



'gure 2-5 Non-power fail recovery board functional block diagram (NPFR)

DIRECT MEMORY ACCESS (DMA)

The processor board includes two INTEL 8237-5 DMA controllers, (U55 and U66). Each controller has four channels. Since one channel is used for cascading, seven are available for system use.

DMA controller 1 (U55) controls channels 0-3. It supports 8-bit data transfers between 8-bit I/O devices and 8-bit or 16-bit system memory. Data is transferred in blocks up to 64K bits in size and can be transferred anywhere in the total system memory address range of 16M bytes. DMA controller 1 controls addresses A0 to A15 and its associated page register controls A16 to A23.

DMA controller 2 (U66) controls channels 4-7. It supports 16-bit data transfers between 16-bit I/O devices and 16-bit memory. Data is transferred, in blocks up to 128K bits in size, on even byte boundaries only. Channel 4 is reserved for cascading the two controllers. DMA controller 2 controls address lines A1 to A16 and its associated page register controls lines A17 to A24.

DMA page register (U38), for channels 5-7, contain the address bits A17 through A23. The addresses are output in data bits D1 through D7. D0 is not used for 16-bit transfers. The base address, for channels 5-7, written into the base address register should be the real address divided by two.

When addressing memory DMA channel addresses, do not increment across page boundaries.

The Page Register addresses are shown in Figure 2-6.

DMA CONTROLLER	CHANNEL	FUNCTION	PAGE REGISTER I/O ADDRESS
1	0	UNDEDICATED	87H
1	1	SDLC	83H
1	2	FLEX DISK	81H
1	3	UNDEDICATED	82H
2	4	CASCADE TO CNT 1	
2	5	UNDEDICATED	8BH
2	6	UNDEDICATED	89H
2	7	UNDEDICATED	8AH
		REFRESH REGISTER	8FH

Figure 2-6 Page register addresses

The DMA controller command code addresses are shown in Figure 2-7.

ADDRESS	FUNCTION
0C0H	CH0 BASE AND CURRENT ADDRESS
0C2H	CH0 BASE AND CURRENT WORD COUNT
0C4H	CH1 BASE AND CURRENT ADDRESS
0C6H	CH1 BASE AND CURRENT WORD COUNT
0C8H	CH2 BASE AND CURRENT ADDRESS
0CAH	CH2 BASE AND CURRENT WORD COUNT
0CCH	CH3 BASE AND CURRENT ADDRESS
0CEH	CH3 BASE AND CURRENT WORD COUNT
0D0H	READ STATUS REG OR WRITE COMMAND REG
0D2H	WRITE REQUEST REGISTER
0D4H	WRITE MASK REGISTER (SINGLE BIT)
0D6H	WRITE MODE REGISTER
0D8H	CLEAR BYTE POINTER
0DAH	READ TEMP REGISTER OR MASTER CLEAR
0DCH	CLEAR MASK REGISTER
0DEH	WRITE MASK REGISTER (ALL BITS)

Figure 2-7 DMA controller command code addresses

TIMER/COUNTER

The board provides three programmable 16-bit timer counters (U63). Counter 0 is tied to interrupt 0, counter 1 is used for dynamic RAM refresh and counter 2 is used for the speaker, as shown in Figure 2-8.

COUNTER	CLK IN	OUTPUT
0	1.190MHz	8259A IRQ0
1	1.190MHz	REFRESH REQUEST
2	1.190MHz	SPEAKER DRIVE

Figure 2-8 Timer counters

INTERRUPT CONTROL

Two 8259A-2 interrupt controllers (U67 and U68 for the PFR board and U68 and U69 for the NPFR board) regulate the interrupt requests from external devices. They are cascaded to provide 16 levels of interrupts as shown in Figure 2-9.

Interrupt		Use
(U68)	0	Timer Counter 0
	1	Keyboard output buffer full
	2	Cascade input from second controller
	3	Auxiliary serial port
	4	Serial Asynchronous Communications Port
	5	Auxiliary parallel port
	6	Flex disk drive controller
	7	Parallel (Printer) Port
(U67)	8	Clock Interrupt
	9	Causes IRQ2 (software controlled)
	10	Reserved
	11	Reserved
	12	Reserved
	13	80287 Coprocessor
	14	Fixed disk drive controller
	15	Reserved

Figure 2-9 Hardware interrupt assignments

A non-maskable interrupt (NMI) is activated when either:

- A parity error occurs when reading from RAM
- An error has occurred in a device in one of the expansion slots
- Power to the power supply has been lost. (Applicable only to the PFR board.)

NUMERIC PROCESSOR EXTENSION

This board supports an 80287 high performance numeric processor (U44) which provides high-speed mathematical computation capabilities. The specific device speed required depends on the operational speed of the system, as shown in Figure 2-10.

SYSTEM CLOCK	COPROCESSOR TYPE REQUIRED
6.0 MHz	80287-3
8.0 MHz	80287-8
10.0 MHz	80287-8

Figure 2-10 System speed/coprocessor type requirements

The numeric processor control registers function as follows:

An OUT instruction to port 0F0H clears the 80287 busy signal.

This busy signal is latched if the 80287 generates an error signal while busy.

An OUT instruction to port 0F1H resets the 80287.

When the processor board is powered up, the non-maskable interrupt (NMI) is disabled outside the 80286.

Enable the NMI by writing a byte with data bit 7 equal to a logic 1, to I/O address 070H.

Disable the NMI by writing a byte with data bit 7 equal to a logic 0, to I/O address 070H.

CPU VLSI

The CPU VLSI, U39, is a CMOS chip containing much of the 'glue' logic required for operation of the processor board. The main features of this chip are system clock generation, system control signal generation, shut down logic and NMI control logic. The device is packaged in a 84-pin plastic leaded chip carrier (PLCC). Figure 2-11 is a block diagram of the CPU VLSI chip.

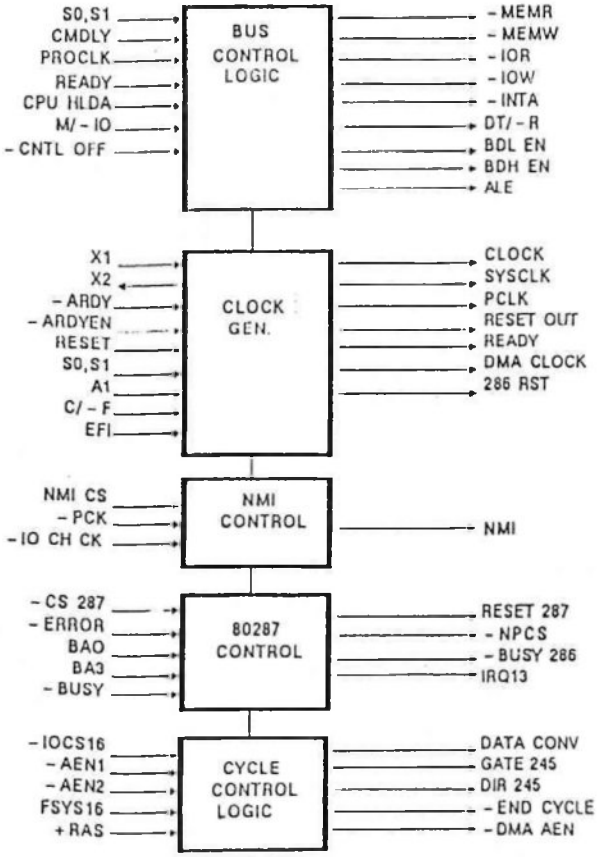


Figure 2-11 CPU VLSI block diagram

DRAM CONTROLLER VLSI - POWER FAIL RECOVERY BOARD (PFR)

The DRAM controller VLSI chip (U71) generates the appropriate signals required to control up to 2.128M bytes of dynamic RAM and 128K bytes of EPROM/ROM, and maintain the RAM when in the power down mode. The length of time that the integrity of memory can be maintained depends on the amount of memory and the size of the battery. The DRAM controller is packaged in a 84-pin PLCC. Figure 2-12 is a block diagram of the DRAM controller.

NOTE: This information applies only to the power fail recovery board.

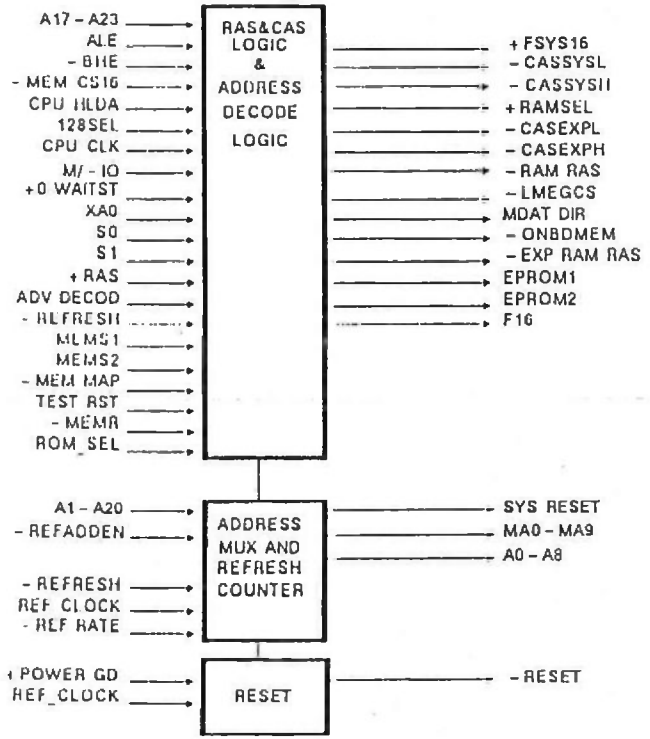


Figure 2-12 DRAM controller VLSI (PFR)

Signals MEMS1, MEMS2, -MEM_MAP, and 128_SEL decode the addresses on the chip. If the address is a RAM address, the proper RAS and CAS signals are generated. If the ADVANCE_DECODE signal is held high, the chip allows 0 wait state operation. If the ADVANCE_DECODE function is active, signals M/-IO, S0, and S1 determine if the current machine cycle is a memory read or a memory write. If the ADVANCE_DECODE function is not active, the chip waits for the +RAS signal to go high before generating RAS and CAS signals to memory. No advance decoding is possible during a DMA cycle.

Under normal operation, this chip generates a refresh RAS once every 15 microseconds. After power is lost, the chip runs through a normal refresh for 512 cycles. Memory is then refreshed at an extended rate, if jumper JP6 is set to 1-2, which is about eight times slower than normal memory speed. Upon power-up, the chip reverts back to the normal refresh rate and begins normal operation. The ROM BIOS firmware is responsible for keeping -REFRESH high long enough for 512 refresh cycles to be generated before -REFRESH goes low.

DRAM CONTROLLER VLSI - NON-POWER FAIL RECOVERY BOARD (NPFR)

The DRAM controller VLSI (U72) generates the appropriate signals required to control up to 640K bytes of dynamic RAM and 128K bytes of EPROM/ROM. The DRAM controller is packaged in a 68 pin PLCC. Figure 2-13 is a block diagram of the DRAM controller.

NOTE: This information applies only to the non-power fail recovery board.

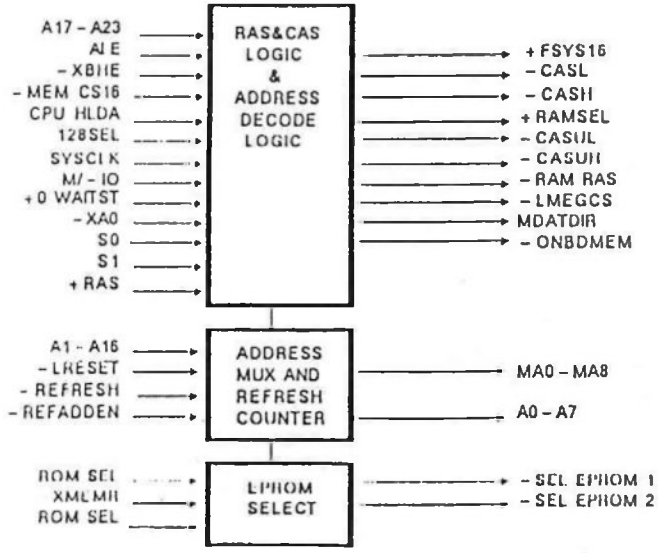


Figure 2-13 DRAM controller VLSI (NPFR)

REAL-TIME CLOCK VLSI

The Real-Time Clock (RTC) VLSI chip, U63, contains the functional equivalent of the Motorola MC146818 Time of Day chip and the Intel 8254 Timer chip. It supports all of the time of day modes provided by the MC146818, three user programable counters, and battery back-up. The chip is packaged in a 68-pin PLCC. Figure 2-14 is a block diagram of the RTC VLSI chip. This section includes a block diagram, an I/O address map, a list of significant features of the chip, and a description of the interface to the chip.

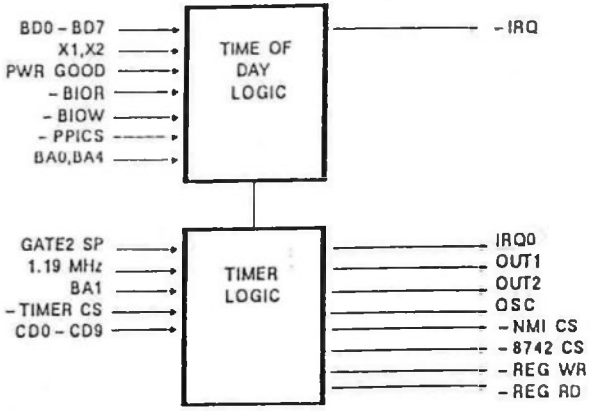


Figure 2-14 RTC VLSI block diagram

The real-time clock logic contains 14 bytes used by the RTC chip for time and date control. The remaining 50 bytes are used by the processor board to store various parameters required for system operation. The function of each of these bytes is outlined in Figure 2-15.

I/O ADDRESS	FUNCTION
00H	RTC Seconds*
01H	RTC Seconds alarm*
02H	RTC Minutes*
03H	RTC Minutes alarm*
04H	RTC Hours*
05H	RTC Hours alarm*
06H	RTC Day of the week*
07H	RTC Day of the month
08H	RTC Month
09H	RTC Year
0AH	RTC Status register A
0BH	RTC Status register B
0CH	RTC Status register C
0DH	RTC Status register D
0EH	Status byte (Diagnostic)*
0FH	Status byte (Shutdown)*
10H	Flex disk drive (Type)
11H	Unused
12H	Fixed disk drive (type)
13H	Unused
14H	Equipment flag
15H	Base memory byte (Low)
16H	Base memory byte (High)
17H	Expansion memory byte (Low)
18H	Expansion memory byte (High)
19H-2DH	Unused
2EH-2FH	Checksum
30H	Expansion memory byte (Low)*
31H	Expansion memory byte (High)*
32H	Century data*
33H	Power on Flags*
34H-3FH	Unused

* These bytes are not included in the checksum calculation.

Figure 2-15 RTC RAM I/O address map

The following is a list of significant features of the RTC VLSI chip:

- Internal Time Base and Oscillator
- Counts Seconds, Minutes, and Hours of the Day
- Counts Days of the Week, Date, Month, and Year
- Time Base Input: 32.768 KHz
- Time Base Oscillator for Parallel Resonant Crystals
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12 or 24 Hour Clock with AM and PM in 12 Hour Mode
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Interfaced as 64 RAM Locations
- 14 Bytes of Clock and Control Registers
- 50 Bytes of General Purpose RAM
- Status Bit Indicates Data Integrity
- Three software-maskable and testable interrupts:
  - Time of Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Interrupt Rates from 122.070 uS to 500 mS
  - End-of-Clock Update Cycle

The interface to the RTC is described below.

Input and Output Control Line Functions

The functions of the I/O control lines are described below.

Multiplexed Bidirectional Address/Data Bus (AD0-AD7) -- The bus presents the address during the first phase of the bus cycle, and the data during the second phase. The valid address must be presented just before the fall of ALE. Valid write data must be presented and held stable at the end of the write cycle. In a read cycle, 8 bits of data are output near the end of the cycle.

ALE - Multiplexed Address Strobe -- This input is a positive strobe pulse that demultiplexes the bus. The falling edge of ALE causes the address to be latched within this device.

IRQ - Interrupt Request -- This active High output interrupts the host processor as needed. The IRQ output remains High as long as the status bit enabling the interrupt is set. To clear IRQ, the processor reads Register C. RESET also clears pending interrupts. When no interrupt is occurring, the IRQ pin is Low or Tri-Stated according to the way the RTC is programmed.

RESET -- This input does not affect the clock, calendar, or RAM functions. It does affect the following:

- Periodic Interrupt Enable (PIE) bit is cleared, zero
- Alarm Interrupt Enable (AIE) bit is cleared, zero
- Update Ended Interrupt Enable (UIE) bit is cleared, zero
- Update Ended Interrupt Flag (UF) bit is cleared, zero
- Interrupt Request Status Flag (IRQF) bit is cleared, zero
- Periodic Interrupt Flag (PF) bit is cleared, zero
- Alarm Interrupt Flag (AF) bit is cleared, zero
- IRQ pin is Tri-Stated

PS - Power Sense -- This input controls the Valid RAM and Time (VRT) bit in Status Register D. When PS is low, the VRT bit is cleared. During power-up, the PS pin must be externally held low for a minimum of 5uS. As power is applied, the VRT bit remains LOW . The contents of RAM, time registers, and calendar are not guaranteed as long as the VRT bit is low.

Address Map -- Memory consists of 50 user RAM bytes, 10 time, calendar, and alarm data bytes, and four control and status bytes. The processor can read and write to all 64 bytes except registers C and D, Bit 7 of Register A and of the seconds byte, which are read only, and Bit 7 of the seconds byte which is always "0". Figure 2-16 shows the RAM address map and control registers in this chip.

The processor obtains time and calendar information by reading the proper locations. The time, calendar, and alarm may be initialized by writing to the correct RAM locations. The contents of the ten time, calendar, and alarm bytes can be either binary or binary coded decimal (BCD). Figure 2-17 shows the binary and BCD formats of the ten time, calendar, and alarm locations.

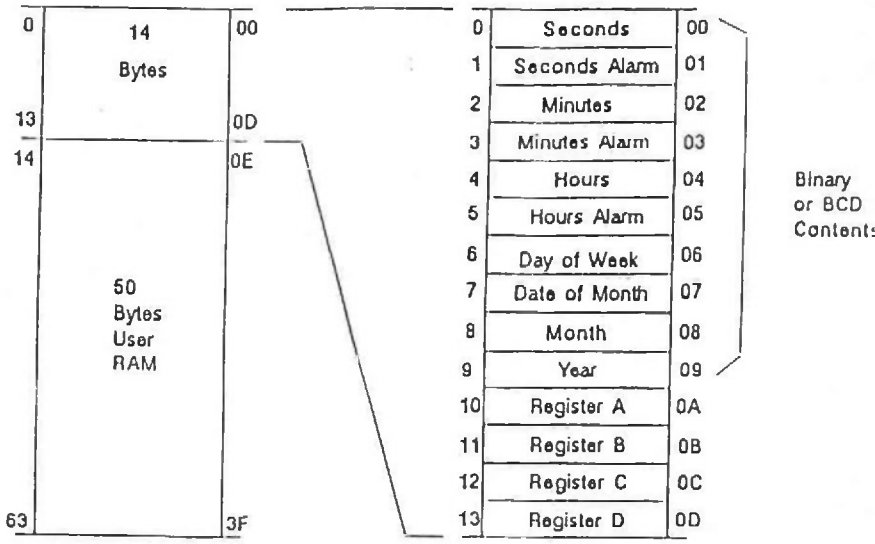


Figure 2-16 RAM and control registers address map

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	Binary Data Mode
0	Seconds	0 - 59	$00 - $3B	$00 - $59	15	21
1	Seconds Alarm	0 - 59	$00 - $3B	$00 - $59	15	21
2	Minutes	0 - 59	$00 - $3B	$00 - $59	3A	59
3	Minutes Alarm	0 - 59	$00 - $3B	$00 - $59	3A	59
4	Hours Alarm (12 Hour Mode)	1 - 12	$01 - $0C (AM) and $81 - $8C (PM)	$01 - $12 (AM) and $81 - $92 (PM)	06	06
	Hours Alarm (24 Hour Mode)	0 - 23	$00 - $17	$00 - $23	06	06
5	Hours Alarm (12 Hour Mode)	1 - 12	$01 - $0C (AM) and $81 - $8C (PM)	$01 - $12 (AM) and $81 - $92 (PM)	06	06
	Hours Alarm (24 Hour Mode)	0 - 23	$00 - $17	$00 - $23	06	06
6	Day of the Week Sunday = 1	1 - 7	$01 - $07	$01 - $07	06	06
7	Date of the Month	1 - 31	$01 - $1F	$01 - $31	07	16
8	Month	1 - 12	$01 - $0C	$01 - $12	02	02
9	Year	0 - 99	$00 - $63	$00 - $99	4F	79

* Example: 6:59:21 Thursday 15 February 1979 (time in AM)

Figure 2-17 Time, calendar, and alarm data modes

Periodic Interrupt Selection -- The periodic interrupt allows the IRQ pin to be triggered once every 122.070 uS to 500mS. It is separate from the alarm interrupt which can output once per second to once per day. Figure 2-18 shows the selection of the Register A bits that set the periodic interrupt frequency. The periodic interrupts must be enabled by the PIE bit in Register B.

Rate Select Control Register A				32.768 KHz Time Base Periodic Interrupt Rate tPI	Rate Select Control Register A				32.768 KHz Time Base Periodic Interrupt Rate tPI
RS3	RS2	RS1	RS0		RS3	RS2	RS1	RS0	
0	0	0	0	None	1	0	0	0	3.90625 mS
0	0	0	1	3.90625 mS	1	0	0	1	7.8125 mS
0	0	1	0	7.8125 mS	1	0	1	0	15.625 mS
0	0	1	1	122.070 uS	1	0	1	1	31.25 mS
0	1	0	0	244.141 uS	1	1	0	0	62.5 mS
0	1	0	1	488.281 uS	1	1	0	1	125 mS
0	1	1	0	976.562 uS	1	1	1	0	250 mS
0	1	1	1	1.953125 mS	1	1	1	1	500 mS

Figure 2-18 Register A rate selection bit settings

Alarm Interrupt Selection -- The three alarm bytes can be used in two ways. The processor can insert an alarm time in the appropriate hours, minutes, and seconds alarm locations and set the alarm enable bit to enable the alarm interrupt to occur at the specified time each day.

A "Don't Care" ("DC") code can also be inserted in any of the three alarm bytes to obtain different results. A "DC" code is any hexadecimal byte, from C0 to FF, with its two most significant bits set to 1. An alarm interrupt occurs each hour if a "DC" is inserted in the hours alarm byte, each minute if inserted in the hours and minutes bytes, or each second if inserted into all three alarm bytes.

The processor selects which interrupts, if any, it wishes to receive. A "1" written to the appropriate register B bit locations enables one of the three interrupts. A "0" in a bit location prohibits the corresponding interrupt from occurring. If an interrupt flag is already set when the interrupt is enabled, the IRQ pin is immediately activated though the interrupt, that initiated the event, may have occurred much earlier. Therefore, the processor should clear earlier initiated interrupts before enabling new interrupts. When an interrupt occurs, a flag bit is set to a "1" in Register A. Each of the interrupts have a bit in Register A which are set independent of the state of the corresponding enable bits in Register B. The flags may be used with or without enabling the corresponding enable bits. However, there is one precaution: the flag bits in Register A are cleared when Register A is read, more than one interrupt bit could be set in a read and all would be erased. Therefore, if the processor is polling instead of using interrupts, all set bits should be read and the bit status saved while handling all polled interrupts.

Static CMOS RAM -- The 50 bytes of RAM are not dedicated to any particular function. They may be used by the processor and are accessible during the update cycle. They can be used to store essential non-volatile data since the RAM can be kept valid by use of battery backup.

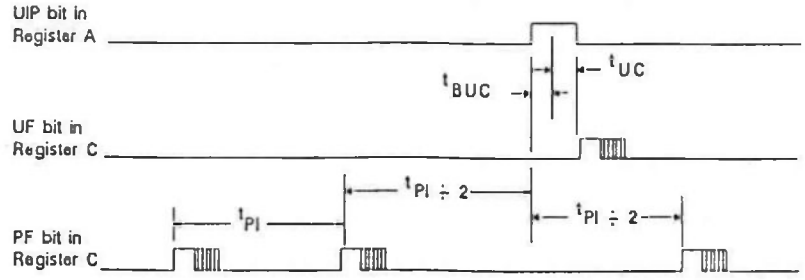
Update Cycle -- The RTC executes an update cycle once per second assuming one of the proper time bases is in place and the SET bit in Register B is clear. When the SET bit is a "1", the processor can initialize the time and calendar bits by stopping any existing update and by preventing a new one to begin. The most important function of the update cycle is to increment the seconds byte, check for an overflow condition, increment the minutes byte when needed and so on through to the year of the century byte. Also, each alarm byte is compared to its corresponding time byte, and an alarm is executed if there is a match or if a "DC" code (11XXXXXX) is present in all three positions. A 32.768 KHz time base update takes 1,984 uS. During the update cycle, the time, calendar, and alarm bytes are inaccessible. The Update In Progress (UIP) status bit is set at this time.

There are three routines the processor may use to avoid the update cycle.

If the Update-Ended interrupt is enabled, an interrupt occurs every update cycle and over 999 mS are available to read valid data. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second routine uses the Update-In-Progress bit (UIP) in Register B to determine the status of the update. The UIP bit is set once per second. After the UIP bit goes High, the update begins 244 uS later. Therefore, the user has at least 244 uS, if the UIP bit is Low, to read valid data. Once the UIP bit is set, data is not valid and should not be used by the processor. Also, the user should avoid interrupt service routines that cause it to take longer than 244 uS to read time/calendar data.

The third routine uses the periodic interrupt to determine if an update cycle is in progress. The UIP bit is set High between the setting of the PF bit in Register C. Periodic interrupts that occur at a rate greater than tBUC + tUC allow valid information to be read at each occurrence of the periodic interrupt. The reads should be done within (tPI + 2) + tBUC to insure valid data. See Figure 2-19 for more information on the update cycle.



tPI = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62.6 ms, etc. per Figure 2 – 18)
tUC = Update Cycle Time (248 µs or 1984 µs)
tBUC = Delay Time Before Update Cycle (244 µs)

Figure 2-19 Update-ended and periodic interrupt relationships

RTC Registers

The RTC has four registers, A,B,C, and D, which are accessible by the 80286 processor during the update cycle. These registers are described below.

Register A -- A diagram of register A's bit functions is shown in Figure 2-20. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
UIP	x	x	x	RS3	RS2	RS1	RS0

Figure 2-20 Register A bit functions

Update In Progress Bit (UIP) -- This is a status bit that can be monitored by the processor. If set to a "1", the update cycle is in progress or will be shortly. If a "0", an update will not occur for at least 244 uS. The time, calendar, and alarm data is all valid and accessible when the bit is "0". This bit is read only and ignores RESET; however, writing a "1" in the SET bit of Register B will prohibit updates and clear the UIP status bit.

Rate Selection Bits (RS3,RS2,RS1,RS0) -- These four bits select the rate the periodic interrupts will occur if the PIE bit in Register B is set to "1". These four bits are read/write, are not affected by RESET and are never changed by the RTC. See Figure 2-18.

Register B -- A diagram of register B's bit functions is shown in Figure 2-21. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	x	DM	24/12	DSE

Figure 2-21 Register B bit functions

SET -- When the SET bit is a "0", the update cycle advances the count once per second. When SET is a "1", any update cycle in progress is aborted and the processor may initialize the time and calendar bytes without an update occurring. SET is a read/write bit and is not modified by RESET.

Periodic Interrupt Enable Bit (PIE) -- PIE is a read/write bit that allows the periodic interrupt flag (PF) bit to cause the IRQ pin to be driven High. The processor writes a "1" to the PIE bit in order to receive periodic interrupts at the rate selected by RS3, RS2, RS1, and RS0 in Register A. A "0" in PIE keeps IRQ inactive by a periodic interrupt, but the PF bit is still set at the periodic rate. PIE is cleared to "0" by RESET.

Alarm Interrupt Enable Bit (AIE) -- The AIE bit is a read/write bit which, when set to a "1", permits the alarm flag (AF) to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal their corresponding alarm bytes including the "DC" state. When AIE is "0", the AF bit does not set IRQ. The RESET pin clears AIE to "0".

Update-ended Interrupt Enable bit (UIE) -- The UIE bit is a read/write bit which enables the update-end flag (UF) bit to set IRQ. If the RESET pin or the SET bit is set to a "1", the UIE bit is cleared.

Data Mode Bit (DM) -- The DM bit indicates whether the time and data updates are to use binary or BCD formats. It is dependent only on the processor. A "1" indicates binary data, a "0" indicates BCD data.

24/12 Bit -- The 24/12 bit sets the format of the hours bytes as either the 24 hour mode, set to a "1" or the 12 hour mode, set to a "0". It is affected only by the processor.

Daylight Savings Enable Bit (DSE) -- The DSE bit is a read/write bit which allows the processor to enable two special updates when DSE is a "1". On the last Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October, the time changes from 1:59:59 AM to 1:00:00 AM. These times do not change when DSE is "0". DSE is not changed by any internal operations or RESET.

Register C -- A diagram of register C's bit functions is shown in Figure 2-22. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

Figure 2-22 Register C bit functions

Interrupt Request Flag (IRQF) -- The IRQF flag is set to "1" if one or more of the following occur:

- PF = PIE = "1"
- AF = AIE = "1"
- UF = UIE = "1"

When IRQF is set to "1", the IRQ pin is driven Low. All flag bits are cleared after Register C is read or RESET is activated.

Periodic Interrupt Flag (PF) -- The PF flag is a read only bit. It is set to "1" when a particular edge is detected on the divider chain. This flag is cleared when Register C is read or by RESET.

Alarm Interrupt Flag (AF) -- When the AF bit is set to "1", the current time has matched the alarm time. A "1" causes IRQ to go High if AIE is also High ("1"). This also sets the IRQF bit. A RESET or Register C read clears AF.

Update-Ended Interrupt Flag (UF) -- This flag bit is set at the end of each update cycle. When UF and UIE are a "1", IRQF is set to "1" and IRQ goes High. UF is cleared by RESET or a Register C read.

B3 to B0 -- Unused bits of Register C, read as "0's". They cannot be written to.

Register D -- A diagram of register D's bit functions is shown in Figure 2-23. These functions are described in the following paragraphs.

b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Figure 2-23 Register D bit functions

Valid RAM and Time Bit (VRT) -- The VRT bit indicates the condition of the contents of RAM provided the power sense (PS) pin of the chip is properly connected. A "0" appears when the PS pin is Low. The processor can set the VRT bit when the time and calendar are initialized. The VRT is a read only bit that cannot be modified by the RESET pin. The VRT bit can only be set by reading Register D.

b6 to b0 -- These unused bits are always read as "0's" and cannot be written to.

KEYBOARD INTERFACE

The processor board contains a port for a serial keyboard. The keyboard status and interface is provided by an Intel 8247 UPI controller chip, described below. The connector, J5, is a 10 pin dual jumper block. In addition to the signals used for keyboard control the connector also can input the POWER GOOD signal from the power supply on pin three. This signal is not required for keyboard operation.

The pin-out is listed in Figure 2-24. See Figure 1-1 or 1-2 for the location of this connector.

SIGNAL	PIN	DIRECTION
+Clock	1	Bi-directional
+Data	2	Bi-directional
POWER GOOD	3	Input
+5 Volts	4	Output
NC	5	
GROUND	6	
GROUND	7	
GROUND	8	
GROUND	9	
GROUND	10	

Figure 2-24 Keyboard connector pin-out

8742 CONTROLLER

The two ports on the 8742 Universal Peripheral Interface (UPI) chip, U37, are used by the system for status and keyboard interface. They are described in Figure 2-25.

DATA BIT	INPUT PORT	OUTPUT PORT
0	Unused	Reset system board
1	Unused	Gate Address 20
2	Unused	System speed switch
3	Unused	Unused
4	Sense RAM size 0-Not supported 1-512K on system board	Output buffer full
5	Power-on default speed 0-S2 pins 1-2 High speed 1-S2 pins 2-3 Low speed	Input buffer empty
6	Display type Switch S1 0-Color/Graphics 1-Monochrome	Keyboard clock out
7	Keyboard disable switch 0-Keyboard disabled 1-Keyboard enabled	Keyboard data out

Figure 2-25 UPI port description

In addition to the input/output ports two test pins, 1 and 39, are used to sample keyboard data from the keyboard. Their functions are shown in Figure 2-26.

Pin 1	TEST 0	Keyboard clock input
Pin 39	TEST 1	Keyboard data input

Figure 2-26 UPI test pin definitions

SOFTWARE SPEED SWITCHING

The board has provision for software speed switching. This option allows operation at two speeds. Proper jumper strapping is required for the selected speed; refer to the "Switches, Jumpers, and Adjustments" section of this manual. One speed is determined by the frequency of the primary crystal. This is fixed at 6.0 MHz. The second frequency is determined by the frequency of the crystal oscillator on the board. This oscillator must be between 6.0MHz and 10.0MHz. Figure 2-27 shows RAM speed/performance increase for different speed options.

Wait State	6.0MHz	8.0MHz	10.0MHz
0	120ns/33%	80ns/50%	not available
1	200ns/0%	150ns/25%	120ns/40%

Figure 2-27 Speed/performance comparison

ADDRESS MAPS

Two types of addressing are defined for the 80286 CPU, memory and I/O. They are described below.

Memory Address Map

The 24-bit address bus of the 80286 CPU defines a 16 MB physical address space. The 80286 operates in two addressing modes:

- The real address mode supports a 1MB address space. In this mode the 80286 is object code compatible with the 8088 and 8086 processors.

- The protected mode allows a 16 MB physical address space with a one gigabyte virtual address space. In protected mode some object code for the 8088 and the 8086 may require modification to support the virtual addressing requirements. The memory address map is shown in Figure 2-28.

Memory Address	Memory Type	Locations
000000H - 07FFFFH	512 KB RAM	SYSTEM BOARD
080000H - 09FFFFH	128 KB RAM	SYSTEM BOARD OR EXPANSION BOARD
0A0000H - 0BFFFFH	128 KB RAM	VIDEO DISPLAY
0C0000H - 0DFFFFH	128 KB ROM	EXPANSION ROM FOR I/O BOARDS
0E0000H - EFFFFFH	64 KB ROM	SYSTEM BOARD ROM DUPLICATED AT FE0000
0F0000H - 0FFFFFH	64 KB ROM	SYSTEM BOARD BIOS DUPLICATED AT FF0000
100000H - FDFFFFH	15 MB RAM	EXPANSION RAM SPACE
FE0000H - FEFFFFH	64 KB ROM	SYSTEM BOARD ROM DUPLICATED AT 0E0000
FF0000H - FFFFFFH	64 KB ROM	SYSTEM BOARD BIOS DUPLICATED AT 0F0000

Figure 2-28 Memory address map

I/O Address Map

The 80286 CPU defines an I/O address map by dedicating ten address bits, A0-A9, to address 1KB of address space reserved for I/O instructions. The I/O address map includes I/O addresses reserved for specific devices in the expansion slots as well as dedicated system board I/O addresses.

Dedicated processor board I/O addresses are shown in Figure 2-29.

ADDRESS	DEVICE
000H - 01FH	DMA chip 1 (8237A-5)
020H - 03FH	Interrupt controller 1 (8259A-2)
040H - 05FH	RTC VLSI
060H - 06FH	Keyboard controller (8742)
070H - 07FH	RTC chip, DMA mask
080H - 09FH	DMA page register (74LS612)
0A0H - 0BFH	Interrupt controller 2 (8259A-2)
0C0H - 0DFH	DMA chip 2 (8237A-5)
0E0H - 0EFH	Reserved
0F0H	Clear math coprocessor busy
0F1H	Reset math coprocessor
0F8H - 0FFH	Math coprocessor
219H	Power-down NMI - NOTE: Applicable only to the PFR board.

Figure 2-29 Dedicated I/O addresses

I/O addresses reserved for specific devices in the expansion slots are shown in Figure 2-30.

ADDRESS	DEVICE
1F0H - 1F8H	Fixed disk controller
200H - 20FH	Game adapter
278H - 27FH	Parallel printer port (secondary)
2F8H - 2FFH	Serial port (secondary)
300H - 31FH	Prototype card
330H - 35FH	Reserved
360H - 36FH	Reserved
378H - 37FH	Parallel printer port (primary)
380H - 38FH	SDLC/BISYNC (secondary)
390H - 39FH	Reserved
3A0H - 3AFH	SDLC/BISYNC (primary)
3B0H - 3BFH	Monochrome CRT and parallel port
3C0H - 3CFH	Reserved
3D0H - 3DFH	Color/graphics CRT adapter
3E0H - 3EFH	Reserved
3F0H - 3F7H	Flex disk adapter
3F8H - 3FFH	Serial port (primary)

Figure 2-30 Reserved I/O addresses

CONNECTORS

SPEAKER CONNECTOR

The speaker connector, J4, is available for connection of an 8-ohm speaker. Counter 2 of the timer drives the speaker. The pin-out is shown in Figure 2-31.

PIN #	DESCRIPTION
1	SPEAKER SIGNAL (speaker -terminal)
2	KEY
3	GROUND
4	+5 Volts DC (speaker +terminal)
5	Volume control (jumpering pin 5 to pin 6 disables the volume circuitry)
6	Volume control

Figure 2-31 Speaker connector pin-out

BATTERY CONNECTOR

The battery connector, J2, connects an external battery to the processor board for powering the Real-Time Clock chip and provides an alternate connection for POWER GOOD. To support the battery back-up mode of operation, +5 volts must be supplied to the DRAM Controller VLSI chip and +6.3 volts to the Real-Time Clock chip. The pin-out is shown in Figure 2-32.

PIN #	DESCRIPTION
1	+VOLTAGE (+Battery voltage to RTC chip)
2	KEY
3	POWER GOOD (Active high power good signal)
4	GROUND (Logic ground)
5*	+BATTERY VOLTAGE (Battery voltage to DRAM and memory)
	*NOTE: Applicable only to the PFR board.

Figure 2-32 Battery connector pin-out

KEYBOARD LOCK/LED SPEED INDICATOR CONNECTOR

The keyboard lock/LED speed indicator connector, J3, indicates processor speed by the color of the LED (if a two color LED is used). It also prohibits keyboard entry while the system is unattended. The pin-out is shown in Figure 2-33.

PIN #	DESCRIPTION
1	LED ANODE (Higher speed indication)
2	GROUND
3	KEY
4	+INHIBIT KBD
5	GROUND
6	LED ANODE (6.0MHz operation)

Figure 2-33 Keyboard lock/LED speed indicator connector pin-out

KEYBOARD/POWER GOOD CONNECTOR

The keyboard/power good connector, J5, provides control signals to an external keyboard and inputs a POWER GOOD signal from the power supply. The pin-out is shown in Figure 2-34.

PIN#	DESCRIPTION	PIN#	DESCRIPTION
1	+CLOCK	6	GROUND
2	+DATA	7	GROUND
3	POWER GOOD	8	GROUND
4	+5 VOLTS	9	GROUND
5	NC	10	GROUND

Figure 2-34 Keyboard/power good connector pin-out

EXPANSION RAM CONNECTOR

Connector JM1 is used for RAM expansion above the 512K on the processor board. It is a 36 pin header containing all the signals required to support a 128K byte expansion board. Jumper strap JP3 and JP8 must be set properly to enable this option, refer to the *Jumper Strapping* chapter of this manual. The pin-out is shown in Figure 2-35.

PIN#	SIGNAL	DESCRIPTION	PIN#	SIGNAL	DESCRIPTION
1*	-EXP RAS	DRAM RAS	2	MD0	DATA BUS
3	-CAS 2	LO BYTE CAS	4	MD1	DATA BUS
5	-CAS 3	HI BYTE CAS	6	MD2	DATA BUS
7	-WE	WRITE ENABLE	8	MD3	DATA BUS
9	MA0	DRAM ADDRESS	10	MD4	DATA BUS
11	MA1	DRAM ADDRESS	12	MD5	DATA BUS
13	MA2	DRAM ADDRESS	14	MD6	DATA BUS
15	MA3	DRAM ADDRESS	16	MD7	DATA BUS
17	MA4	DRAM ADDRESS	18	MD8	DATA BUS
19	MA5	DRAM ADDRESS	20	MD9	DATA BUS
21	MA6	DRAM ADDRESS	22	MD10	DATA BUS
23	MA7	DRAM ADDRESS	24	MD11	DATA BUS
25	-MEMR	MEMORY READ	26	MD12	DATA BUS
27	PTYINLO	LOW PARITY IN	28	MD13	DATA BUS
29	PTYINHI	HI PARITY IN	30	MD14	DATA BUS
31	PTYOUTLO	LOW PARITY OUT	32	MD15	DATA BUS
33	PTYOUTHI	HI PARITY OUT	34	**	See Note
35	+5V	POWER	36	GND	LOGIC GND

*NOTE: This signal is -RAS 1 for the NPFR board.

**NOTE: Pin 34 is connected to JP8, and can either be a logic ground or the ninth memory address MA8 on the power fail recovery board. For the non-power fail recovery board, it is a logic ground.

Figure 2-35 Expansion RAM connector pin-out

EDGE CONNECTORS

The processor board contains one 62 pin and one 36 pin bus connector. The 62 pin connector (P1), shown in Figure 2-36, provides the signals required for 8-bit bus interface. The in-line 36 pin connector (P2), shown in Figure 2-37, provides the extra bus signals required for 16-bit operation. The processor board is capable of driving eight I/O slots.

The signals for the bus connectors slots and their corresponding pin designations are listed below. The location of these connectors is shown in Figure 1-1 or 1-2.

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
GROUND	B1	-I/O CHECK	A1
+BRESET	B2	+BD 7	A2
+5 VOLTS	B3	+BD 6	A3
+IRQ9	B4	+BD 5	A4
-5 VOLTS	B5	+BD 4	A5
+DRQ2	B6	+BD 3	A6
-12 VOLTS	B7	+BD 2	A7
EXT_0WS	B8	+BD 1	A8
+12 VOLTS	B9	+BD 0	A9
GROUND	B10	-I/O CH RDY	A10
-CMEMW	B11	+AEN	A11
-CMEMR	B12	+BA19	A12
-IOW	B13	+BA18	A13
-IOR	B14	+BA17	A14
-DACK3	B15	+BA16	A15
+DRQ3	B16	+BA15	A16
-DACK1	B17	+BA14	A17
+DRQ1	B18	+BA13	A18
-REFRESH	B19	+BA12	A19
+BSYSCLK	B20	+BA11	A20
+IRQ7	B21	+BA10	A21
+IRQ6	B22	+BA9	A22
+IRQ5	B23	+BA8	A23
+IRQ4	B24	+BA7	A24
+IRQ3	B25	+BA6	A25
-DACK2	B26	+BA5	A26
+T/C	B27	+BA4	A27
+BSELALE	B28	+BA3	A28
+5 VOLTS	B29	+BA2	A29
+OSC	B30	+BA1	A30
GROUND	B31	+BA0	A31

Figure 2-36 62 Pin card edge connector, 8-bit bus interface

SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER
-MEM CS16	D1	BBHE	C1
-I/O CS16	D2	EXPA23	C2
IRQ10	D3	EXPA22	C3
IRQ11	D4	EXPA21	C4
IRQ12	D5	EXPA20	C5
IRQ15	D6	EXPA19	C6
IRQ14	D7	EXPA18	C7
-DACK0	D8	EXPA17	C8
DRQ0	D9	-MEMR	C9
-DACK5	D10	-MEMW	C10
DRQ5	D11	BD08	C11
-DACK6	D12	BD09	C12
DRQ6	D13	BD10	C13
-DACK7	D14	BD11	C14
DRQ7	D15	BD12	C15
+5 VOLTS	D16	BD13	C16
-BUS CNTRL	D17	BD14	C17
GROUND	D18	BD15	C18

Figure 2-37 36-Pin card edge connector, 16-bit bus interface

Logic Signals and Their Functions

Logic signals and their functions are shown below.

SIGNAL	TYPE	FUNCTION
+BRESET	Out	This signal is the system reset.
+IRQ3- +IRQ15	In	These signals are the interrupt request lines. Interrupt 9 has the highest priority and interrupt 7 the lowest. The signal should be held high until acknowledged by the CPU.
+DRQ0 - +DRQ7	In	These signals are the DMA request lines. +DRQ0 has the highest priority and +DRQ7 the lowest. A request should remain active (high) until the corresponding DACK is received.
-DACK0 - -DACK7	Out	These signals are the DMA acknowledge lines. -DACK4 is reserved for cascading the second DMA controller.
+T/C	Out	This signal indicates that a DMA channel has reached its terminal count.
-MEMW,-CMEMW	I/O	These control signals indicate a processor or DMA memory write cycle. CMEMW is active only when writing memory in the lowest 1MB.

SIGNAL	TYPE	FUNCTION
-MEMR,-CMEMR	I/O	This control signal indicates a processor or DMA memory r cycle. CMEMR is active only whe.. writing memory in the lowest 1MB.
-IOW	I/O	This control signal indicates a processor or DMA I/O write cycle.
-IOR	I/O	This control signal indicates a processor or DMA I/O read cycle.
-I/OCH RDY	In	When this line is low (not ready), the current memory or I/O cycle is extended until after this line goes high (ready). The cycle is extended in multiples of clock cycles. This line should not be held longer than 2.5 micro-seconds.
+OSC	Out	This is a 14.31838 Mhz clock with a 50% duty cycle.
+BSYSCLK	Out	This is the system clock speed. It has a 50% duty cycle.
+AEN	Out	When this line is high, the DMA chip has control of the bus.

SIGNAL	TYPE	FUNCTION
-I/OCHCHECK	In	This line is used to indicate that there is an error on a device in the expansion bus. Activating this line results in an NMI interrupt to the CPU. Memory expansion options commonly use this line to indicate parity errors.
+BSELALE	Out	This signal is used to indicate when the address bus is valid. Processor addresses are latched on the falling edge of +ALE.
+BD0-BD15	I/O	These signals are the data bus.
+BA0-BA19	Out	These signals are the address bus.
EXT_0WS	In	The Zero Wait State signal indicates that the present bus cycle can be completed. For 16-bit devices 0WS is generated by anding a decoded address with a read or write command. For 8-bit devices 0WS must become active one CLK cycle after a read or write command.
-REFSH	I/O	This signal indicates a refresh cycle and is driven by the CPU or the expansion bus.
-BUS CNTRL	In	This signal tri-states the system boards address, data and control signals allowing an external device to gain control of the bus.

SIGNAL	TYPE	FUNCTION
-MEM CS16	In	This signal indicates a 16-bit memory cycle with 1 wait state(
-I/O CS16	In	This signal indicates a 16-bit I/O cycle with 1 wait state.
BBHE	I/O	This signal indicates a data transfer is occurring on BD08-BD15.
EXPA17-23	Out	These signals allow the system board a 16M byte address space.

Data and Control Signals

The data and interface control signals are compatible with standard TTL. Input logic levels are defined in Figure 2-38.

BINARY LEVEL	SYMBOL	VOLTAGE LEVEL (VOLTS) MIN.	MAX.
logic 0	VIL		0.8
logic 1	VIH	2.0	

Figure 2-38 Input logic level voltages

Loading characteristics for the input signals are shown in Figure 2-39.

BINARY LEVEL	SYMBOL	LOAD (MAX)
logic 0	IIL	-0.1 mA
logic 1	IIH	20.0 uA

Figure 2-39 Input loading characteristics

Output logic levels are defined in Figure 2-40.

BINARY LEVEL	SYMBOL	VOLTAGE LEVEL (VOLTS) MIN.	MAX.
logic 0	VOL		0.5
logic 1	VOH	2.4	

Figure 2-40 Output logic level voltages

Loading characteristics for signals BA1-19, OSC and BBHE are shown in Figure 2-41.

BINARY LEVEL	SYMBOL	LOAD (MAX)
logic 0	VOL	24.0 mA
logic 1	IOH	-2.6 mA

Figure 2-41 Signals BA1-19, OSC, and BBHE loading characteristics

Loading characteristics for signals +BRESET, +AEN, BSELALE, BD0-15, -IOW, -IOR, -MEMW AND EXPA17-23 are shown in Figure 2-42.

BINARY LEVEL	SYMBOL	LOAD (MAX)
logic 0	IOL	24.0 mA
logic 1	IOH	-15.0 mA

Figure 2-42 Signals +BRESET, +AEN, BSELALE, BD0-15, -IOW, -IOR, -MEMW, AND EXPA17-23 LOADING CHARACTERISTICS

Loading characteristics for signals BSYSCLK, -REFRESH, -CMEMR, -CMEMW, MEMR AND BA0 are shown in Figure 2-43.

BINARY LEVEL	SYMBOL	LOAD (MAX)
logic 0	IOL	48.0 mA
logic 1	IOH	-15.0 mA

Figure 2-43 Signals BSYSCLK, -REFRESH, -CMEMR, -CMEMW, MEMR, AND BA0 loading characteristics

Loading characteristics for signal T/C are shown in Figure 2-44.

BINARY LEVEL	SYMBOL	LOAD (MAX)
logic 0	IOL	8.0 mA
logic 1	IOH	-0.4 mA

Figure 2-44 Signal T/C loading characteristics

Loading characteristics for signal -REFSH are shown in Figure 2-45.

BINARY LEVEL	SYMBOL	LOAD (MAX)
logic 0	IOL	8.0 mA
logic 1	IOH	-8.0 mA

Figure 2-45 Signal -REFRESH loading characteristics

SYSTEM TIMING

Figure 2-46 reflects the system bus timings, in nanoseconds, at the bus connectors or the VLSI outputs.

SYM	PARAMETER	6.0 MHz MIN	6.0 MHz MAX	8.0 MHz MIN	8.0 MHz MAX	10.0 MHz MIN	10.0 MHz MAX
1	SYS Clock Period	83	250	62	250	50	250
2	SYS Clock Low.	20	250	15	225	11	232
3	SYS Clock High	25	230	25	235	18	239
4	RD Data Set up D8-15	20		20		18	
	RD Data Set up D0-7	30		30		28	
5	RD Data Hold D8-15	15		15		20	
	RD Data Hold D0-7	25		25		28	
6	Ready/ Set up time	50		38		26	
7	Ready/ Hold time	35		25		25	
8	Status PEACK/ valid	1	55	1	45	1	28
	Status PEACK/ inactive					1	30
9	Address valid delay	3	70	3	70	4	57
10	WR data valid delay	3	60	3	60	3	50
11	Address,status,data float delay	0	80	0	50	0	47
12	HLDA valid delay	0	80	0	50	0	47
12a	Address valid to status valid set up			38		27	
13	SRDY/,SRDYEN/ set up	25		17		15	
14	SRDY/,SRDYEN/ hold	0		0		0	
15	ARDY/,ARDYEN/ setup	5		0		0	
16	ARDY/,RDYEN/ hold	30		30		30	
17	PCLK delay	0	45	0	45	0	35
18	ALE active	3	25	3	20	3	16
19	ALE inactive		35		25		19
20	CMDLY setup	25		20		15	
21	CMDLY hold	1		1		1	
22	CMDLY inactive		24		24		24
23	CMDLY active		24		24		24
24	DT,R/ read active		40		25		23
25	DT,R/ read inactive	5	45	5	35	5	20
26	DEN read active	5	50	5	35	5	31
27	DEN read inactive	3	40	3	35	3	21
28	DEN write active		35		30		23
29	DEN write inactive	3	35	3	30	3	19

Figure 2-46 System bus timings

The system timing diagram is shown in Figure 2-47.

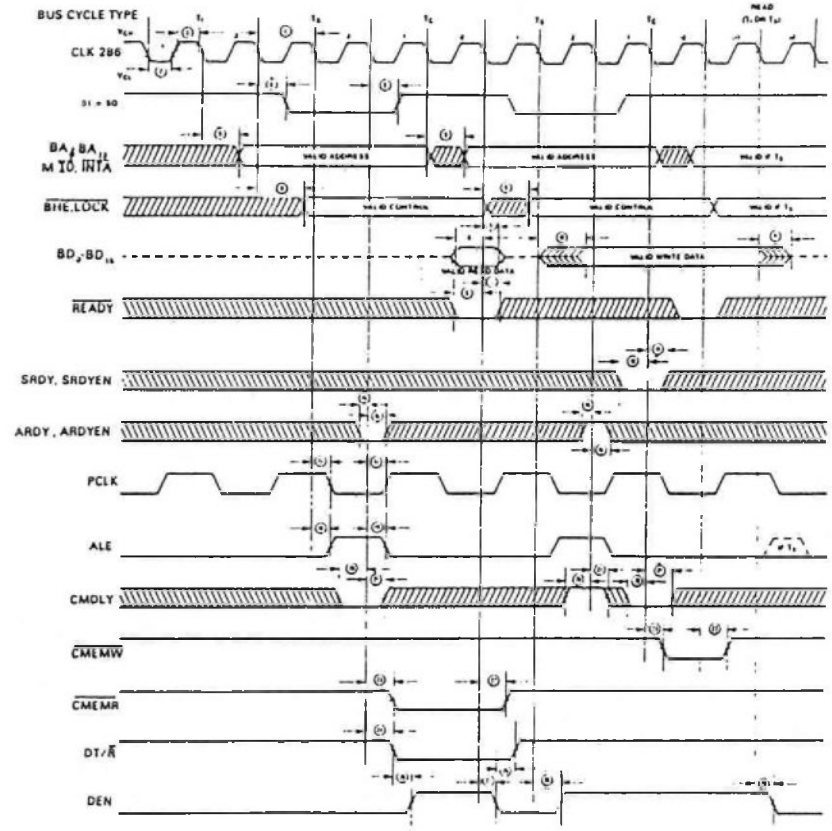


Figure 2-47 System timing diagram

ROM BIOS

The on-board BIOS system firmware resides in two Rom chips, U27 and U30, located on the top left of the board. Both High byte and Low byte components are identified in Figure 1-1 and 1-2. This firmware provides maximum compatibility and supports MS-DOS, CP/M-86, and the existing standard application software base.

SETUP

Setup is a utility packaged with the ROM BIOS. It is a menu driven utility that reinitializes CMOS memory. If the memory or attached device configuration is changed, SETUP should be run. If a condition is detected during power-up which requires CMOS to be reinitialized, a message appears on the screen stating that SETUP should be run. The *Diagnostic* chapter of this manual describes how to run SETUP.

Switches, Jumpers, and Adjustments

Switches, Jumpers, and Adjustments

SWITCH SETTINGS

Switch settings for the video display are shown in Figure 3-1.

PRIMARY VIDEO DISPLAY TYPE	SWITCH S1
Monochrome (00x25)	Slide toward switch S2
Color/Graphics	Slide toward resistor R1

Figure 3-1 Video display switch settings

JUMPER STRAPPING

Some of the options on the processor board require the use of programming straps. The following paragraphs outline the use of these straps.

HIGH PERFORMANCE OPTION

Jumper JP1 selects the high performance mode, zero wait state, of operation. When JP1 is strapped to pin 2-3, the processor board will operate with zero wait states. This mode of operation requires lower access time ROM/EPROM and RAM devices.

ROM/EPROM SIZE SELECT

Strapping for the ROM/EPROM size select is shown in Figure 3-2.

ROM SIZE	JUMPER	PINS
16K x 8	J1	1-8 and 2-7
32K x 8	J1	3-6 and 4-5

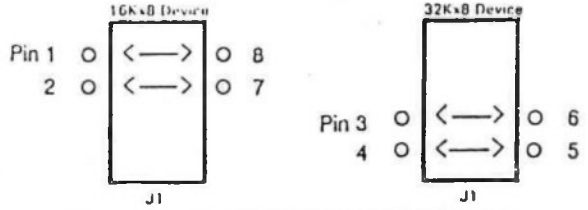


Figure 3-2 ROM/EPROM size select strapping

DESCRIPTION OF JUMPERS (NPFR)

Jumper strapping for the non-power fail recovery board is defined in Figure 3-3.

	OPTION STRAPS	JUMPER 1-2	JUMPER 2-3
JP1	0 WAIT STATES 6-8 MHz ONLY	ENABLE 1 WS	ENABLE 0 WS
JP2	6-8MHz/10MHz	FOR 10 MHz OPERATION	FOR 6-8 MHz OPERATON
JP3	256K/512K SELECT	ENABLE 512K ON BOARD	ENABLE 256K ON BOARD
JP4	DISABLE ALL RAM MEMORY	ENABLE RAM	DISABLE RAM
JP5	128K SELECT	ENABLE 128K EXPANSION	DISABLE 128K EXPANSION CONNECTOR

Figure 3-3 Processor board jumper strapping (NPFR)

SPEED SELECTION SWITCH

Jumper strapping for the initial power-up speed is shown in Figure 3-4.

Speed	Jumper	Pins
6 MHz	S2	2-3
10 MHz	S2	1-2

Figure 3-4 Initial power-up speed strapping

POWER FAIL PROTECTION MODE (PFR)

For normal power fail protection, the jumper straps should be configured as shown in Figure 3-5.

NOTE: This information applies only to the power fail recovery board.

Jumper	Pins	Effect
J6	3-2	Dedicated crystal input to DRAM VLSI enabled.
J7	3-2	Battery Power connection.
JP8	1-2	Ground pin 34 on piggyback connector.
JP9	3-2	Extra power fail delay disabled.

Figure 3-5 Power fail protection strapping (PFR)

NON-POWER FAIL PROTECTION MODE (PFR)

For operation without the Power Down RAM Protection, Figure 3-6 shows the jumper straps that should be connected.

NOTE: This information applies only to the power fail recovery board.

Jumper	Pins	Effect
J6	1-2	Crystal input to DRAM VLSI from RTC
J7	1-2	Normal Power connection.
JP8	1-2	Ground pin 34 on piggyback connector.
JP9	3-2	Extra power fail delay disabled.

Figure 3-6 Non-power fail protection strapping (PFR)

MEMORY CONFIGURATION (PFR)

Memory configuration jumper strapping is shown in Figure 3-7.

NOTE: This information applies only to the power fail recovery board.

JP10	JP4	MEMORY SIZE
1-2	1-2	0 RAM AVAILABLE
2-3	1-2	256KB RAM AVAILABLE
1-2	2-3	512KB RAM AVAILABLE
2-3	2-3	2MB RAM AVAILABLE

Figure 3-7 Memory configuration strapping (PFR)

Normal setting of JP10 and JP4 should be for 512k RAM.

JP5 should be set to 2-3 since this board normally uses 256k RAMs.

JP3 should be set to 1-2 if the 128k piggyback expansion board is not used. Otherwise it should be at 2-3.

WAIT STATE SETTINGS (PFR)

Wait state jumper strapping is shown in Figure 3-8.

NOTE: This information applies only to the power fail recovery board.

STRAP	6/8MHz,1WS	6/8MHz,0WS	6/10MHz,1WS
JP1	1-2	2-3	1-2
JP2	2-3	2-3	1-2

Figure 3-8 Wait state strapping (PFR)

EXTENDED REFRESH (PFR)

If the memory chips used have an extended refresh capability, the jumper JP6 should have pins 1-2 connected. Otherwise, pins 3-2 should be connected.

NOTE: This information applies only to the power fail recovery board.

DESCRIPTION OF JUMPERS (PFR)

Jumper strapping for the power fail recovery board is defined in Figure 3-9.

	OPTION STRAPS	JUMPER 1-2	JUMPER 2-3
JP1	0 WAIT STATES 6 8 MHz ONLY	ENABLE 1 WS	ENABLE 0 WS
JP2	6·8MHz/10MHz	ENABLE 10 MHz SWITCH	DISABLE 10 MHz SWITCH
JP3	128K SELECT	ENABLE 128K EXPANSION	DISABLE 128K EXPANSION CONNECTOR
JP4	MEMS2	See Figure 3-7	See Figure 3-7
JP5	MEM MAP	2 MEG PHYSICAL ADDRESS SPACE	1.640 MEG PHYSICAL ADDRESS SPACE
JP6	REFSH RATE	EXTENDED POWER FAIL REFRESH TIMING	NORMAL SYSTEM SPEED POWER FAIL REFRESH TIMING
JP7	ADV DECODE*	DISABLE ADVANCE DECODE	ENABLE ADVANCE DECODE
JP8	MA8 SELECT	EXTRA GROUND ON 128K BRD.	SENDS MEMORY ADDRESS MA8 TO 128K EXPANSION
JP9	EXTRA POWER DOWN DELAY	NO EXTRA DELAY	74ALS121 ADDED DELAY
JP10	MEMS1	See Figure 3-7	See Figure 3-7
J7	BATTERY CONNECTED	NO BATTERY	BATTERY CONNECTED
J6	OSC	FROM RTC	FROM CRYSTAL

* Refer to the DRAM Controller VLSI section for more detail.

Figure 3-9 Processor board jumper strapping (PFR)

ADJUSTMENTS

The processor board contains an adjustable capacitor VC1 to trim the 14.318 MHz clock. This clock is divided by four to generate 3.579MHz required for color burst synchronization with color televisions. Capacitor VC1 should be adjusted to cause 14.318MHz ± 500Hz at B30 on the I/O bus connectors.

The board also contains an adjustable capacitor for the Time of Day clock. This capacitor, VC2, should be adjusted until 32.768KHz ± 2Hz is measured on U63 pin 63.

Diagnostics

Diagnostics

LEVEL 0 DIAGNOSTICS

This chapter describes the level 0 diagnostic tests performed at power-up. These diagnostic routines reside in ROM and are helpful in detecting defective components. Normal and error messages that may be displayed are shown. Error codes (testpoints) that are output through the processor board port 8011, DMA page 0 register, are also listed.

The following devices are helpful when running level 0 diagnostics:

- Diagnostic plug-in LED test board -- This board plugs into an expansion slot. It has eight LEDs to indicate the test error code and three to indicate voltage. This board, part number 017-0035850, is available from an NCR Worldwide Service and Parts Center.
- Video display
- Keyboard

CAUTION

Only personnel that have experience with multi-layer boards and Surface-Mount Technology (SMT), and have access to specialized desoldering/soldering equipment required to support SMT, should attempt to replace defective components.

LEVEL 0 DIAGNOSTICS MESSAGES

Two forms of Level 0 Diagnostics messages are provided:

- "Beeps" from a speaker
- Video display messages

Speaker Beeps

Speaker beeps provide the following information:

- Five short beeps indicate a fatal error and the system halts.
- Three short beeps indicate a non-fatal error and the system continues to run.
- One long beep indicates successful completion of Level 0 Diagnostics. If the signature 'CA' is present in the first two bytes of a rom at segment address E00011, control is given to that rom. If a rom is not installed at that address, control is given to the boot vector, interrupt 19H.

Video Display Messages

Diagnostic routines display test names and system messages in upper-case characters and error messages in initial caps lower-case characters.

LEVEL 0 DIAGNOSTICS PHASES

Three phases of Level 0 Diagnostics are performed:

- Initial processor board diagnostics -- verifies that the board is functioning properly.
- System test and initialization -- tests and initializes system boards for normal operation.
- System configuration verification -- compares defined configuration with actual hardware.

Initial Processor Board Tests

Before Level 0 routines load the operating system, they make some basic checks on the processor board. If they detect an error, the system attempts to sound five beeps and to display one of the following error messages.

System Port Error
The I/O Port at address 61H was read and verified as defective.

System ROM Error
The sumcheck of the processor board ROM BIOS is not correct.

DMA Page Register Error
DMA Page Register verification failed.

Timer Error
Timer failed.

Refresh Error
The refresh logic did not provide refresh pulses.

0-64KB Ram Error
An error was detected in the first 64KB of RAM.

Bus 8 - 16 Error
The 8 bit to 16 bit bus converting logic failed.

Interrupt Controller Error
The interrupt mask registers do not verify.

8742 Controller Error
The 8742 self-check failed.

CMOS Ram Error
The Real Time Clock Controller failed.

Protected Mode Error (System Halt)
The protected virtual memory in the 80286 failed.

NOTE: The system halts after five beeps or after any of the above messages or errors.

Primary CRT Error
The video monitor indicated by the MPB jumper block is not correctly set.

When the initial level 0 diagnostic tests have run successfully, the following status message is displayed and additional processor board tests are then initiated to verify and initialize the installed system hardware.

MAIN BOARD DIAGNOSTICS COMPLETE,

Test and Initialize:

After the initial phase, the Level 0 diagnostic routines determine what system hardware is installed and test and initialize that hardware. They display test messages throughout this phase to show progress. Test names, preceded by an underscore (_), are displayed at the beginning of the tests. When a test fails, the system stops and/or attempts to sound five beeps and to display an error message.

_DMA CONTROLLERS
Both DMA Controllers are tested and initialized.

_TIMER ZERO
Timer zero is tested.

_INTERRUPT CONTROLLERS
Both Interrupt Controllers are tested and initialized.

_MEMORY
The routine conducts the memory test in 64KB increments. In normal operation, the upper boundary of the bank of memory tested is displayed as shown in the following.

BASE MEMORY TEST
xxxx KB

EXPANSION MEMORY TEST
xxxx KB

TOTAL MEMORY XXXX KB

The routines test the entire memory. Base memory is normally memory below 640KB; expansion memory is the memory area above 1MB. The memory from 640KB to 1MB (for example, CRT RAM and add-on ROM) is tested during other tests. The amount of good memory is shown by xxxx KB, in steps of 64KB. Total memory is the sum of base memory and expansion memory.

The following representations are used in the memory error display examples.

- xxxxxx = Address of observed memory error
- eeee = Expected data
- oooo = Observed data

xxxxxx Memory Error Bit eeee oooo
One or more bits of a memory cell are faulty.

xxxxxx Memory Error Address eeee oooo
An error has been detected in the address test.

xx0000 Memory Error Parity
A parity error has been detected in a 64KB memory bank.

Memory Address Error (System Halt)
An address error for address lines A16 - A23 has been detected. This is a fatal error, and the system stops processing.

_KEYBOARD
The keyboard interface is tested to verify that a compatible keyboard is attached. Also, the keyboard performs a self-check-test and initialization. When an error is detected, the system displays one of the following error messages.

Keyboard Clock Line Error
Keyboard clocking is not functional.

Keyboard Controller Error
The keyboard controller does not accept keyboard commands.

Keyboard Interface Error
The keyboard controller can not control the keyboard interface lines.

xx Key Code Received
The system received a unexpected scan code from the keyboard: xx is the received scan code.

Keyboard Error
The keyboard failed the self-check test.

System Keylock is Locked
The Keyboard Lock is in the locked position.

Press <F1> IF HARDWARE SETUP IS DESIRED
This is a prompt to remind the user that entering <F1> on the keyboard causes the system to execute SETUP of CMOS RAM.

NOTE: If a ^D is pressed at this time, Level 1 Diagnostics will be executed at the completion of level 0 diagnostics.

_FLEX DISK
The flex disk controller and drives are tested and initialized. The heads of drives are moved; however, bit read or write cycles are not performed. If an error is detected, the routine displays one of the following messages.

Disk A Error
Access to disk drive A failed (controller or drive error).

Disk B Error
Access to disk drive B failed (controller or drive error).

Flex Controller Error
Error on flexible disk drive controller.

FIXED DISK
The fixed disk controller is tested and initialized. If an error is detected, the routine displays one of the following error messages.

Disk 0 Failure
Disk drive 0 configured, but not present.

Disk 1 Failure
Disk drive 1 configured, but not present.

Disk 0 Error
Disk not formatted, or controller error.

DISK 1 ERROR
Disk not formatted, or controller error.

_EXTERNAL ROMS xxxx
This message appears only when an external ROM is installed.

xxxx ROM ERROR
The external ROM checksum is not correct: xxxx is the code segment address of the ROM.

_80287 COPROCESSOR INSTALLED
Coprocessor is installed.

_80287 COPROCESSOR NOT INSTALLED
Coprocessor is not installed.

System Configuration Verification

After the diagnostic routines initialize the system, the routines compare actual hardware found with the definition of expected hardware contained in battery-protected CMOS memory. If they are the same, Level 0 Diagnostics are complete. If they are different, the system displays one of the following messages for each error and then displays the SETUP message.

** Battery Power Lost (Run SETUP)
Battery power has been lost. Reconfigure the system with the Setup Utility.

** Configuration not Set (Run SETUP)
The configuration of the system is not set correctly.

** Time & Date not Set (Run SETUP)
The Real-Time-Clock does not run.

** Memory Size Error (Run SETUP)
Detected and configured memory sizes do not agree. Check the memory configuration in the CMOS RAM.

** Disk Configuration not correct
Disk configuration in CMOS and detected disk configuration in Level 0 do not agree.

** Check Keyboard (System Halt)
The keyboard does not function properly.

** Unlock System Keylock
The system is locked, unlock and restart with keyboard available.

Press <F1> for SETUP or <ENTER> to go on

SETTING THE SYSTEM CONFIGURATION

The system has a battery that maintains a part of ROM memory and the time-of-day clock. This memory provides time, date, memory and attached device information to the system.

SETUP is the name of a resident utility that initializes configuration data in this memory. This memory is initialized during assembly so that the system can be used for the first time.

During system startup, at the completion of Level 0 Diagnostics, the contents of the ROM memory are checked for changes. If a change is detected, the system asks if reinitializing is desired. Pressing <F1> automatically executes the SETUP utility. Once the data is initialized, it is battery maintained even while the computer system is turned off.

When the battery must be replaced or a change is made in the configuration of memory or attached devices, press <F1> to execute the SETUP utility to reinitialize the configuration data to the current values.

The SETUP utility is made up of a series of easy to understand displays which:

- set the date and time
- define the flexible disk drive configuration
- define the fixed disk drive configuration,
- define the base and extension memory sizes,
- define the primary video display adapter
- define the screen width

The upper portion of the SETUP screen, as shown in figure 4-1, contains three sections. Each device that can be connected to the system is shown on the left-hand third of the screen. The center third of the screen defines the current settings for each of these devices. Following a change to a current setting, the right-hand third of the screen contains the "New settings" for each change.

In the lower midsection of the screen are two windows. These windows change contents as the up and down arrow keys are used to move the indicator at the left of the device list from one device to another. The right-hand window contains the format of data, or data choices to describe each device. The left-hand window is where the entered input data is shown. After descriptive data is entered and <ENTER> is pressed, the new data is shown under "New settings" in the upper right-hand third of the screen.

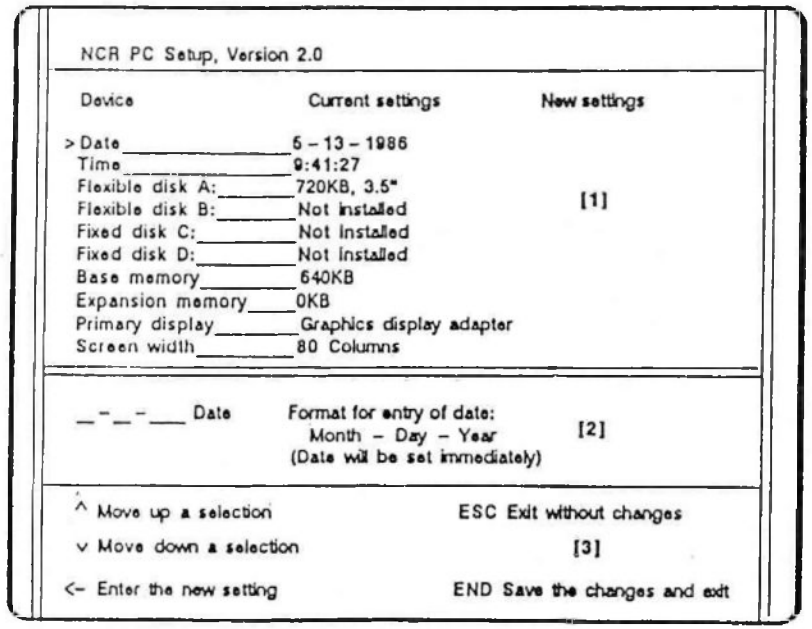


Figure 4-1 SETUP menu

For example, Figure 4-1 shows the Date selected. The lower-right window shows the date format to be Month - Day - Year. The lower-left window is set to accept a date such as, 10-23-86.

TESTPOINTS

At the start of each test, the level 0 diagnostic routines load a testpoint number into the system. This number remains in the system until the diagnostic routines successfully complete the related tests.The following section describes how to read test points for troubleshooting.

Reading Testpoints

If the system fails to load operating system software and does not display a message, Level 0 Diagnostics outputs an error code (testpoint number) to address 80H. These codes can be monitored with a diagnostic test LED board. It has 8 LEDs to indicate the code in binary form (ON = 1) and three LEDs for voltage indication. Figure 4-2 shows the board and location and arrangement of the LEDs.

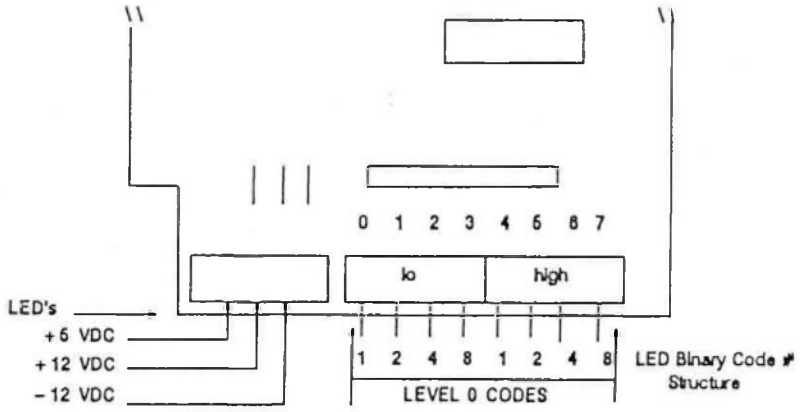


Figure 4-2 Diagnostic LED test board (component side up)

If the diagnostic test LED board is not available, use a voltmeter to test between ground and Pins 2 through 9 (ON=high) of the 62 pin edge connector (P1) on the processor board. Pin 2 is the least significant digit (corresponding to LED 0) and Pin 9 is the most significant digit (corresponding to LED 7).

Testpoint Code Numbers

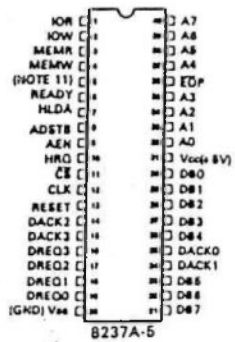
The following list shows all testpoint code numbers.

CODE	TEST
01	CPU Register Test
02	System I/O Port 61H Test
03	ROM Checksum
04	DMA Page Register Test
05	Timer 1 Test
06	Timer 2 Test
07	Refresh Logic
08	Basic RAM Test
09	Bus Converting Logic 8 (=) 16 Bit
0A	Interrupt Controller 1 Test Address 20H
0B	Interrupt Controller 2 Test Address A0H
0C	Checksum of 8742 Controller (U37)
0D	CMOS RAM Verify Test
0E	Test Battery Power Lost
0F	CMOS Configuration Checksum
10	Protected Mode of CPU 80286
11	CRT Configuration
12	Initialization and Test of CRT Controller
13	Primary CRT Controller Error - Test Second Controller
14 - 1F	Reserved
20	Board Test Minimum Complete
21	DMA Controller 1 Test Address 00H
22	DMA Controller 2 Test Address C0H
23	Timer Zero
24	Initialization of the Interrupt Controllers
25	Wait for Unexpected Interrupt
26	Wait for Expected Interrupt
27 - 2F	Reserved
30	Memory Size Base Memory
31	Memory Size Extension Memory
32	Address Test A16 - A23
	Base Memory Test
	Extension Memory Test
35 - 3F	Reserved
40	Keyboard Enable/Disable
41	Keyboard Clock and Data Test
42	Send Reset Command to Keyboard
43	Wait for Reset Answer
44	Set Address A20 to Zero
45 - 4F	Reserved
50	Write Hardware Interrupt Vectors
51	Enable Timer Interrupt
52	CA ROM Installed Test
53 - 5F	Reserved
60	Flex Controller and Drive Test
	Test Fix Flex Controller
62	Initialization Flex Drives
63	Initialization Fix Drives
64 - 6F	Reserved
70	Test Real Time Clock
71	Set Real Time Clock
72	Parallel Interfaces
73	Serial Interfaces
74	Look for External ROM Drivers
75	Coprocessor
76	Enable Keyboard and RTC Interrupt
77 - 7F	Reserved
F0	Display System Messages
F1	System Code on Address E0000H
	Bootstrap System Loading
F2 - FF	Reserved

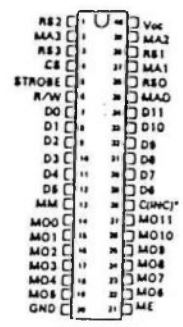
Integrated Circuit Component Pin-Out Configurations

Integrated Circuit Component Pin-Out Configurations

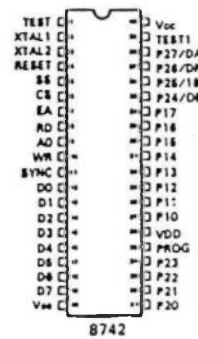
The following diagrams present the pin-out identifications for all of the integrated circuit components used in the NCR 286 Card.



8237A-5

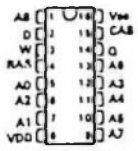


SN74LS612

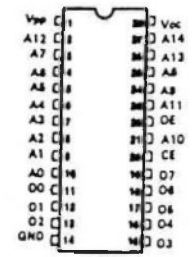


8742

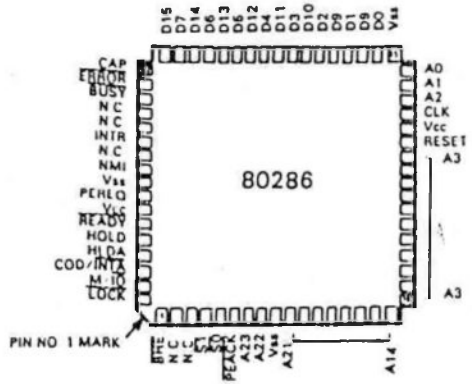
8259A

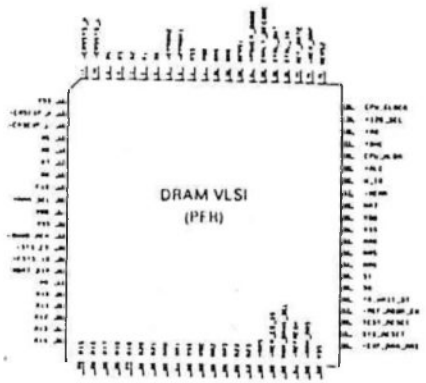


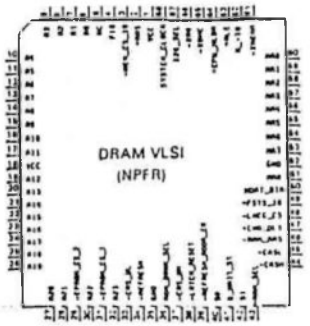
TMS4256

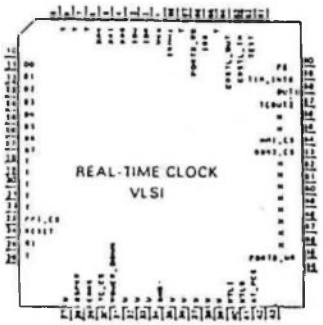


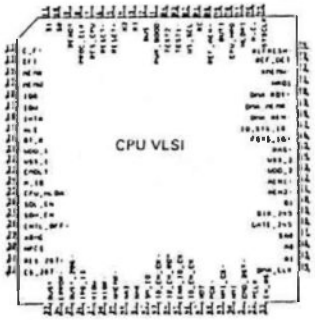
27256











Specifications

Specifications

Specifications for the processor board and its components are presented in the following pages.

PROCESSOR BOARD

INTEL 80286-10 MICROPROCESSOR

- 16-megabyte address bus
- 16-bit data bus
- 16-bit registers
- Integrated memory management
- Four level memory management
- High bandwidth bus interface
- Two operating modes:
  - Real Address mode
  - Protected Virtual Address mode
- large address space:
  - 16 megabytes physical
  - One gigabyte virtual per task

8259A-2 PROGRAMMABLE INTERRUPT CONTROLLER

- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Single +5V supply (no clocks)
- NMOS construction
- Input current: 85mA
- Input voltage: Signal 0.8V low, Vcc+0.5V high
- Surface Mount Technology

82288 BUS CONTROLLER

- Three status lines
- Surface Mount Technology
- NMOS construction
- Single +5V supply

8237A-5 PROGRAMMABLE DMA CONTROLLER (2)

- Four independent channels
- Designed for use with an external 8-bit address register
- 64K address and word capacity on each channel
- Cascaded to 16-bit transfers
- Surface Mount Technology

27256 ERASABLE/PROGRAMMABLE READ-ONLY MEMORY (EPROM)

- 32K byte storage capacity
- Two-line control
- HMOSII-E construction
- Moisture resistant

TMS4256-12 DYNAMIC RANDOM ACCESS MEMORY (DRAM)

- 256K x 1 bit format
- N-channel, SMOS construction
- Power consumption: 1W
- Surface Mount Technology
- Access time: 120ns maximum
- Input voltage: Signal 0.8V low, 6.5V high

PROCESSOR BOARD INTERFACE

- Type: 62-pin standard I/O channel card edge
  36-pin standard I/O channel card edge
- Power: Supplied via 62-pin and 36-pin connectors
  +5V DC @ 2.25 amps

8742 UNIVERSAL PERIPHERAL INTERFACE MICROCONTROLLER

- 8-bit CPU with ROM, RAM, I/O, timer/counter, and clock
- 2048 x 8 ROM/EPROM, 128 X 8 RAM, 8-bit time/controller, 18 programmable I/O pins
- One 8-bit status and two data registers for asynchronous slave-to-master interface

SN74LS612 MEMORY MAPPER

- Paged memory mapping
- 3-state output
- Expands four address lines to 12 address lines

DRAM CONTROLLER VLSI

- 256K x 1 bit format
- Battery backup - provides refresh to battery supported system DRAM when power is removed (PFR board only)
- Power up/down reset timer (PFR board only)
- Input voltage: Signal 0.8V low, Vcc high

RTC VLSI

- Two operating modes
- Programmable Real Time Clock with static RAM and battery backup capabilities
- Programmable counter/timer functionally equivalent to Intel 8254-2
- Glue logic
- Input voltage: Signal -.3V low, 7V high

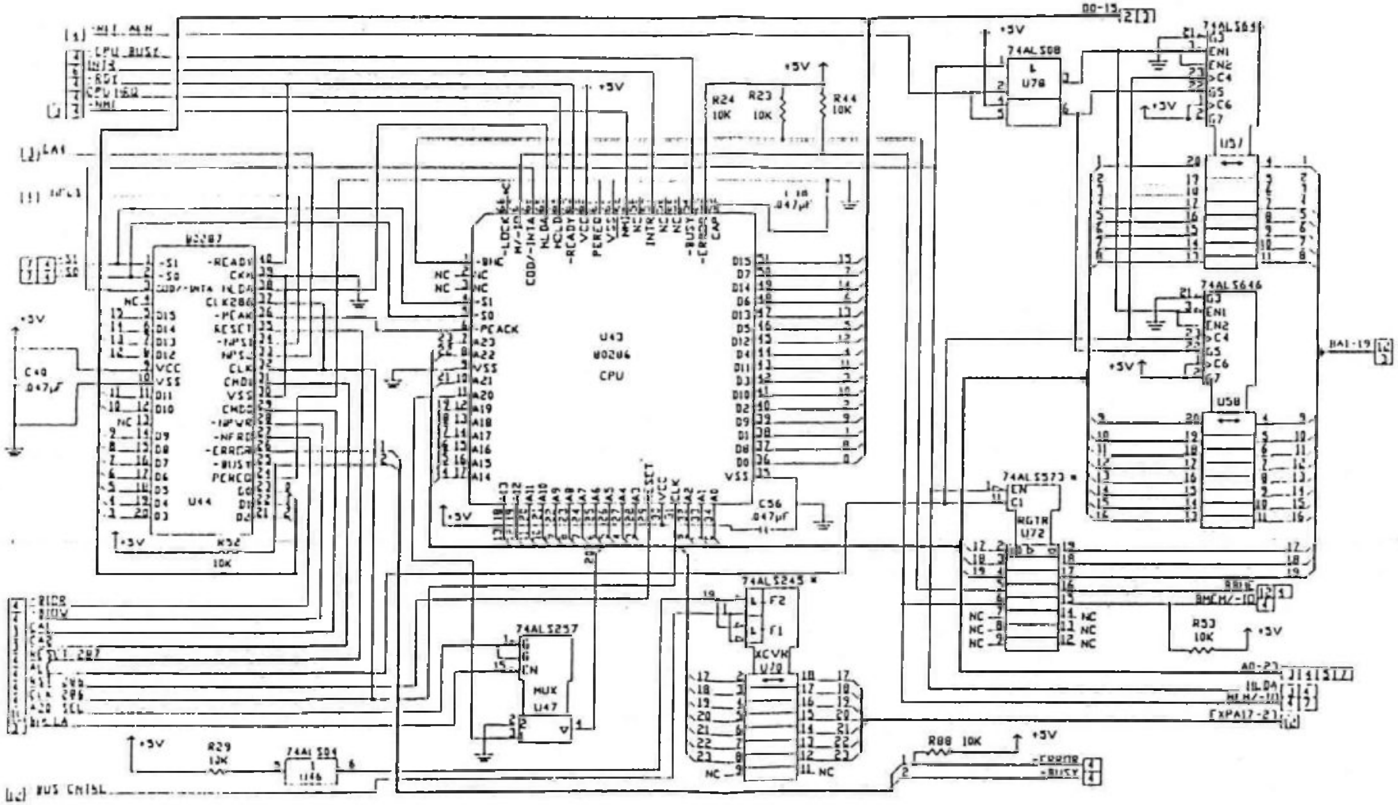
CPU VLSI

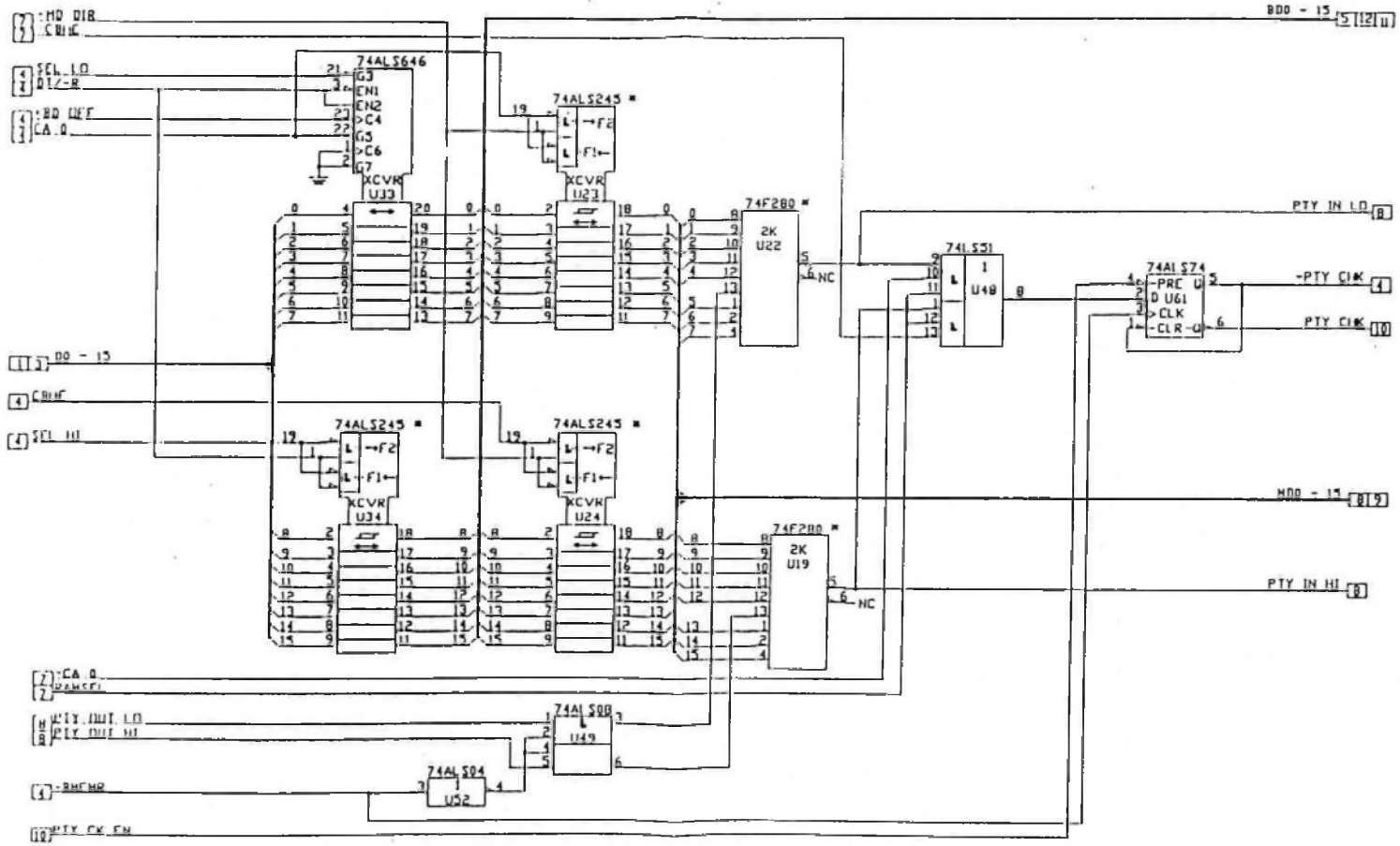
- CMOS construction
- Glue logic
- System clock and control signal generation
- NMI control
- Shut down logic

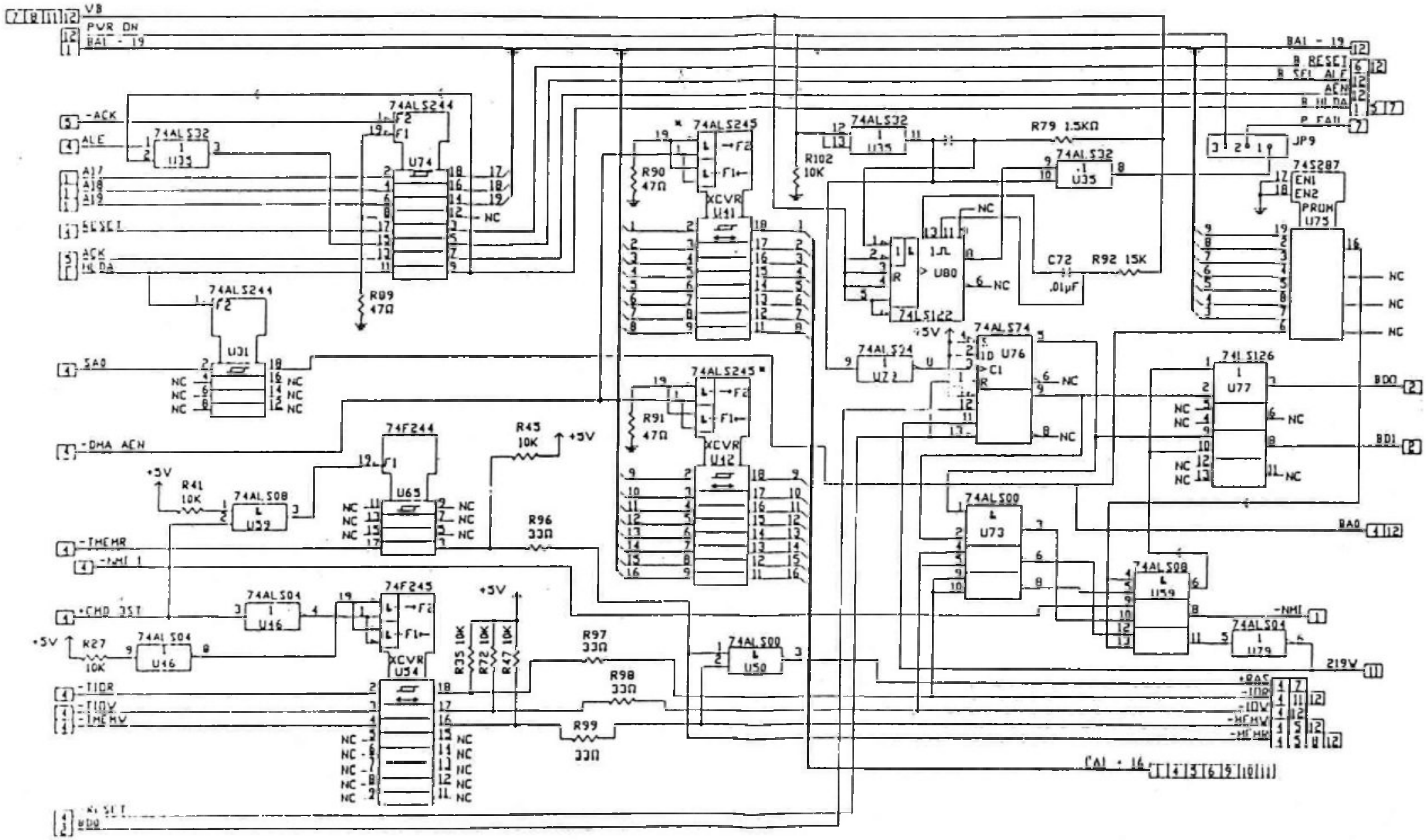
Logic Diagrams

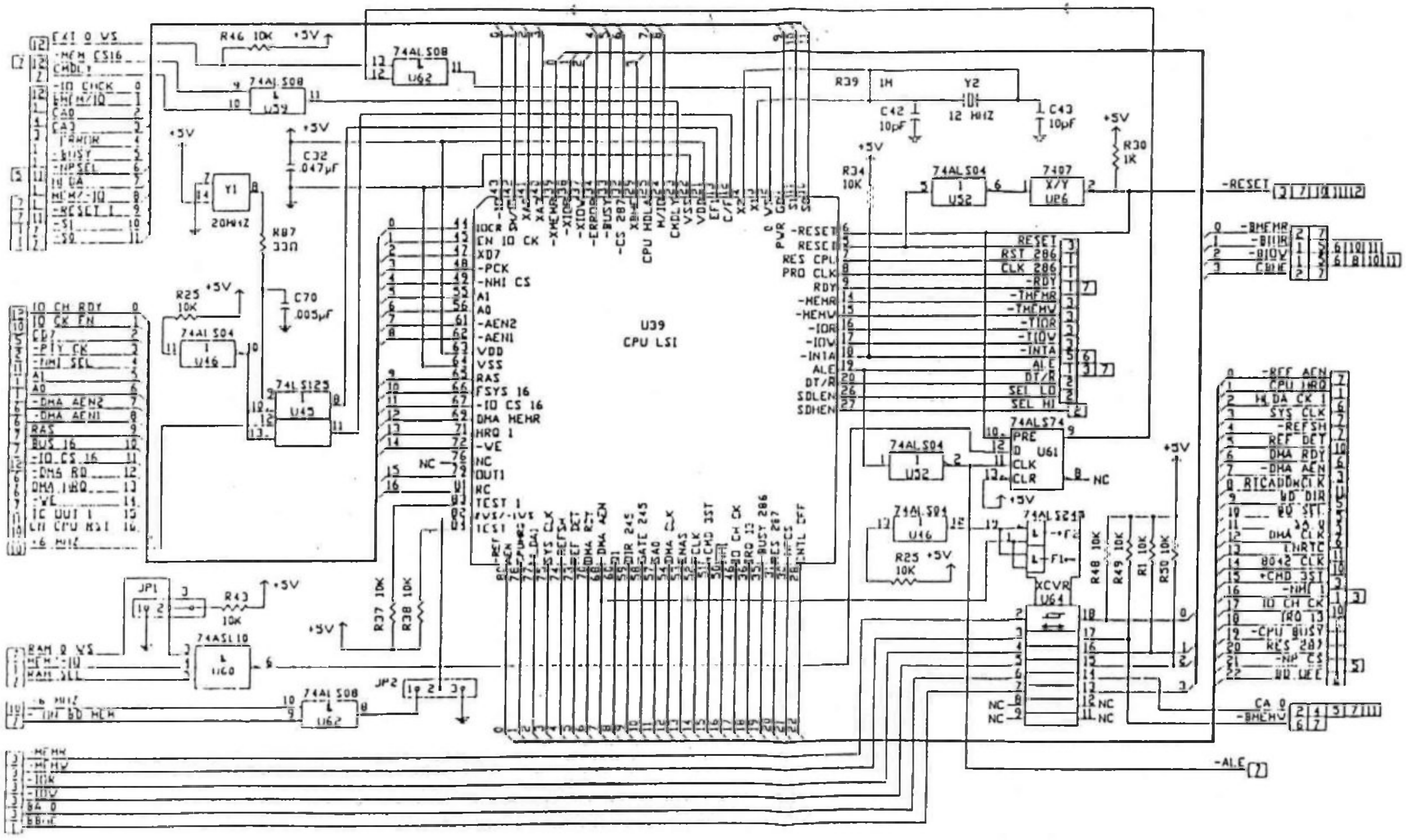
Logic Diagrams

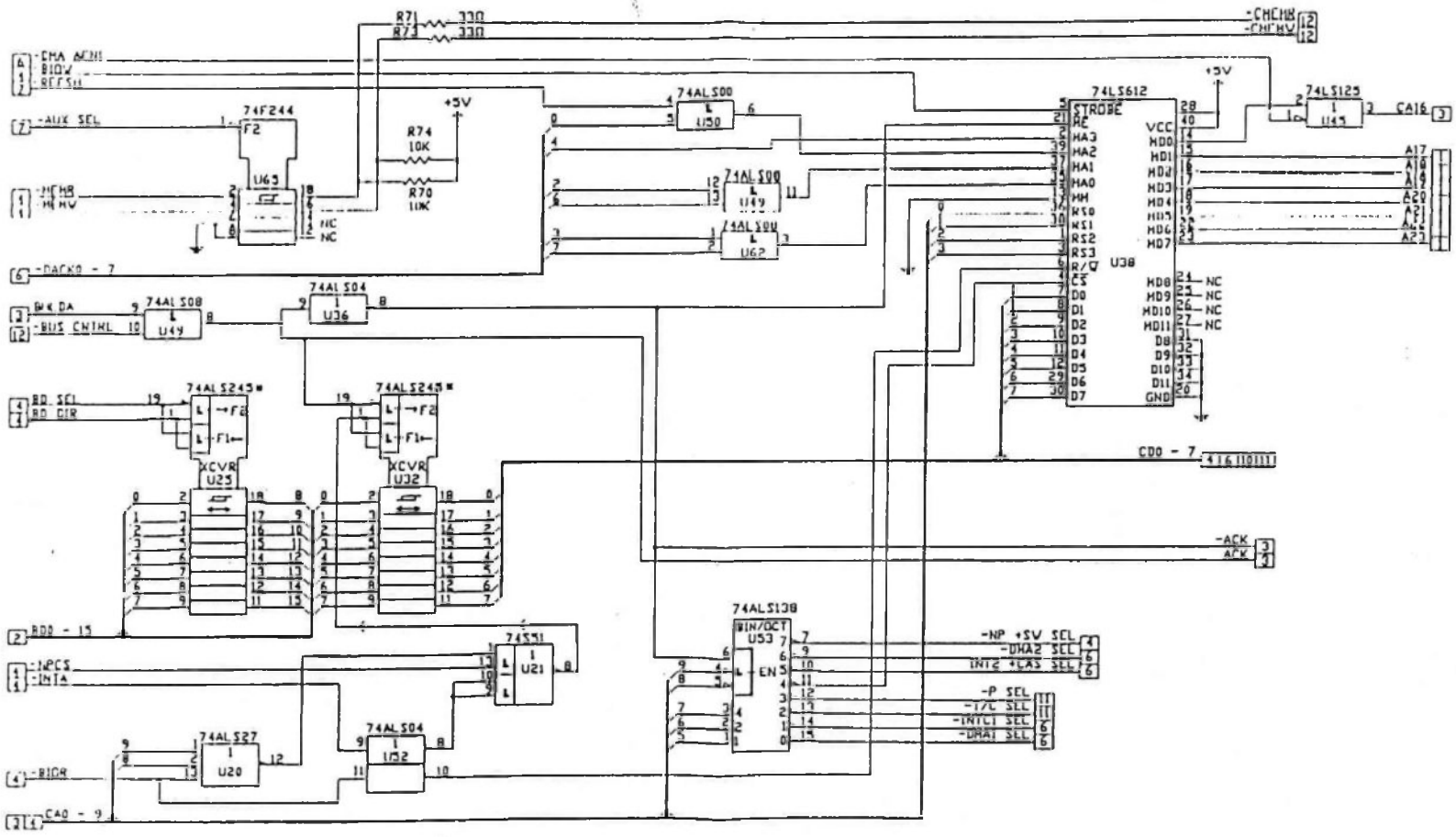
Logic diagrams for the power fail recovery processor board are presented in the following pages.

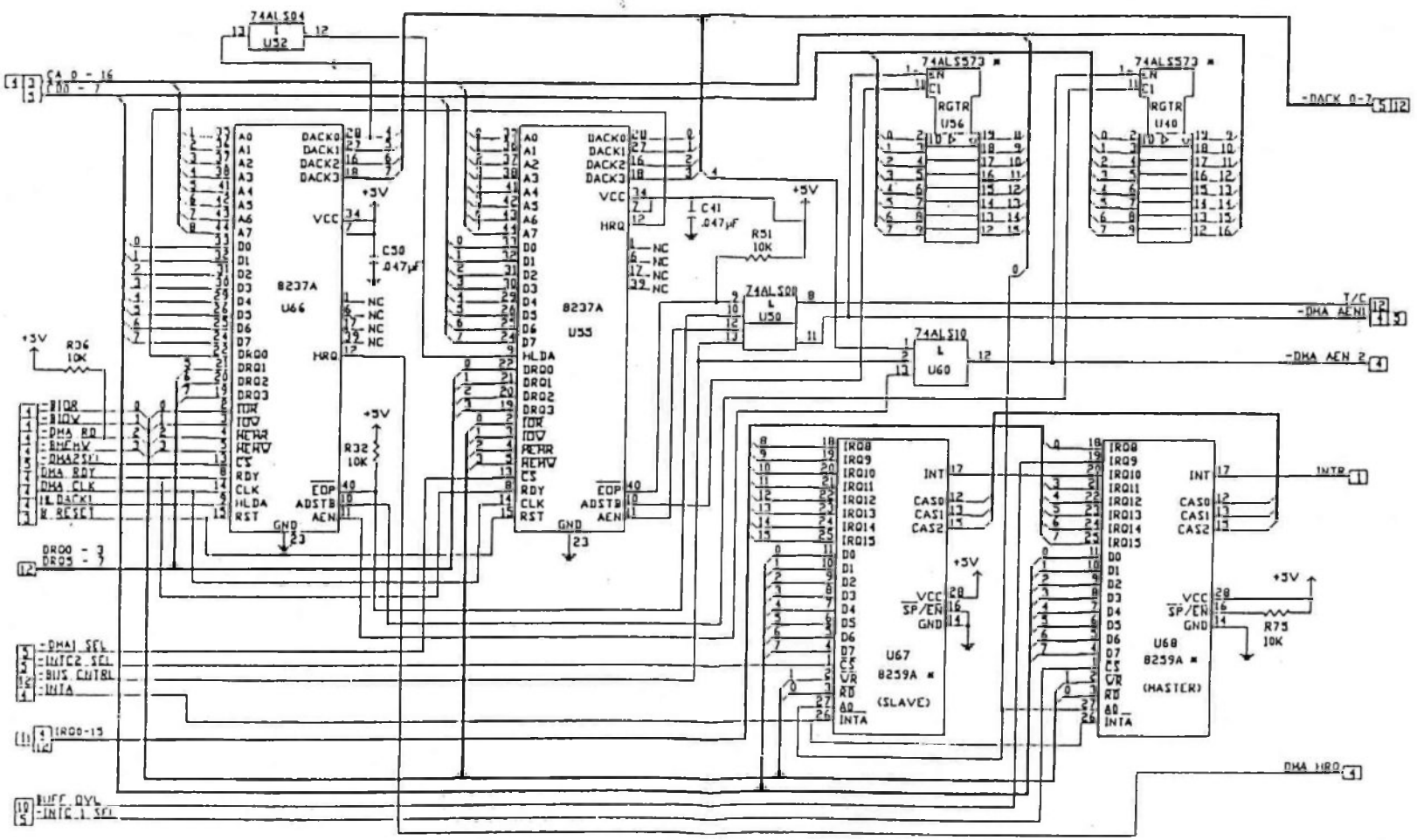

U43
80286
CPU
U44
74ALS08
U78
74ALS646
U57
U58
74ALS573
U72
74ALS245
U70
74ALS257
U47
MUX
74ALS04
U46
R24 10K
R23 10K
R44 10K
R52 10K
R53 10K
R29 10K
R88 10K
C56 .047µF
C49 .047µF
+5V

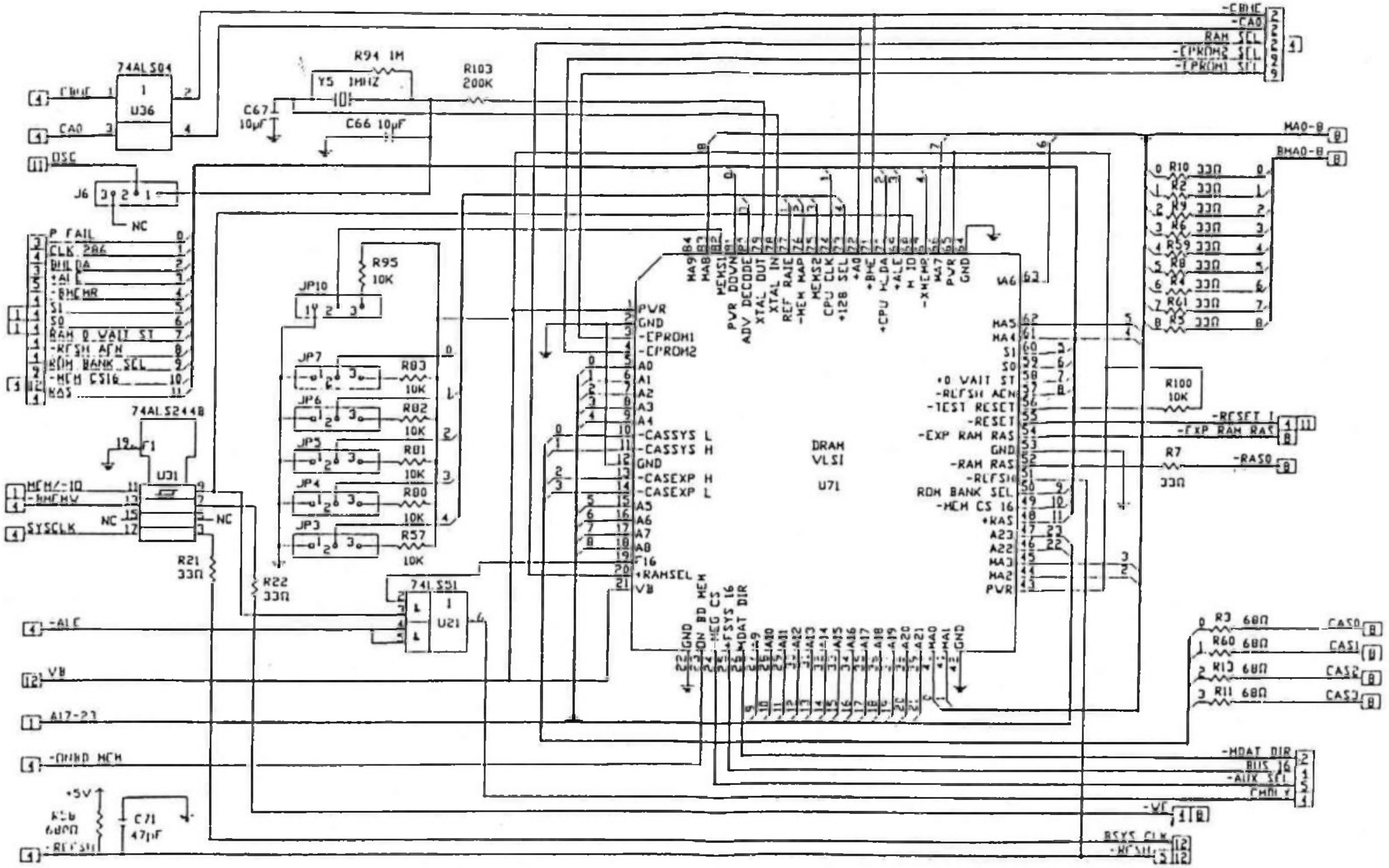

MD DIR
CBUSC
SCL LO
DIZ-R
BD DEF
CA 0
DO - 15
CBUSC
SCL HI
CA 0
PARITY
PTY OUT LO
PTY OUT HI
-BHFHR
PTY CK EN
74ALS646
XCVR U33
74ALS245 *
XCVR U23
74ALS245 *
XCVR U34
74ALS245 *
XCVR U24
74F280 *
2K U22
74F280 *
2K U19
74LS51
U48
74ALS74
-PRE
D U61
>CLK
-CLR
74ALS08
U49
74ALS04
U52
BDO - 15
PTY IN LO
-PTY CLK
PTY CLK
MDO - 15
PTY IN HI
NC
NC

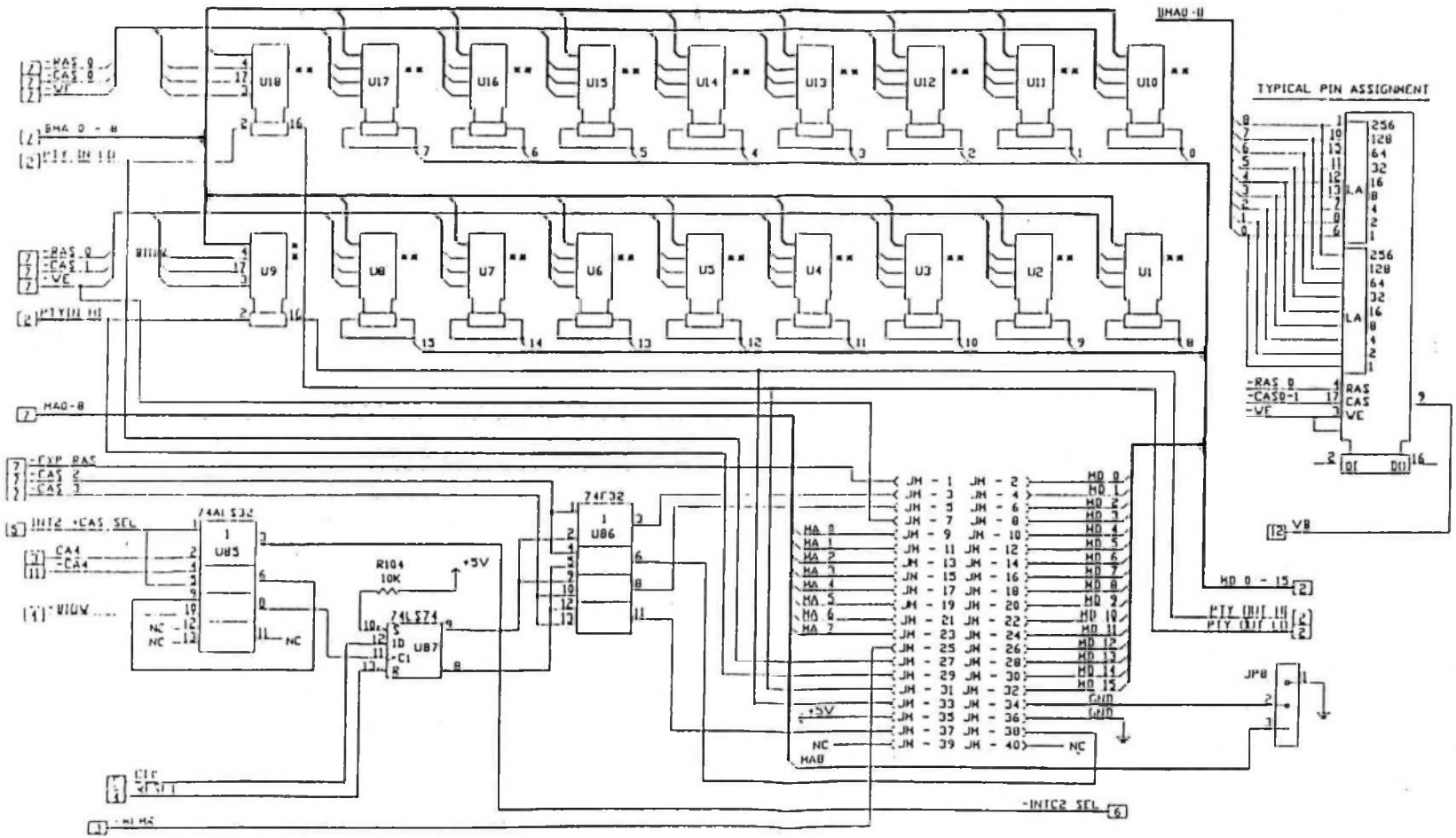

74ALS244
74ALS32
U74
U35
74ALS245
XCVR
U41
U42
R90
47Ω
R91
R89
R102
10K
R79 1.5KΩ
C72
.01µF
R92 15K
74LS122
U80
JP9
74S287
PROM
U75
74ALS74
U76
74ALS24
U72
74LS126
U77
74ALS00
U73
74ALS08
U59
74ALS04
U79
74F244
U65
74F245
U54
R43
R41
U52
U46
R27
R96
R97
R98
R99
33Ω
R35
R72
R47
U50
U31
+5V
NC
BA1 - 19
B RESET
B SEL ALE
AEN
B HLDA
P FAIL
BD0
BD1
BA0
-NMI
219V
CA1 - 16
-ACK
ALE
RESET
HLDA
SA0
-DMA AEN
-IMEMR
-NMI 1
-CHD RST
-TIOR
-TIOW
-IMEMW
VB
PWR ON

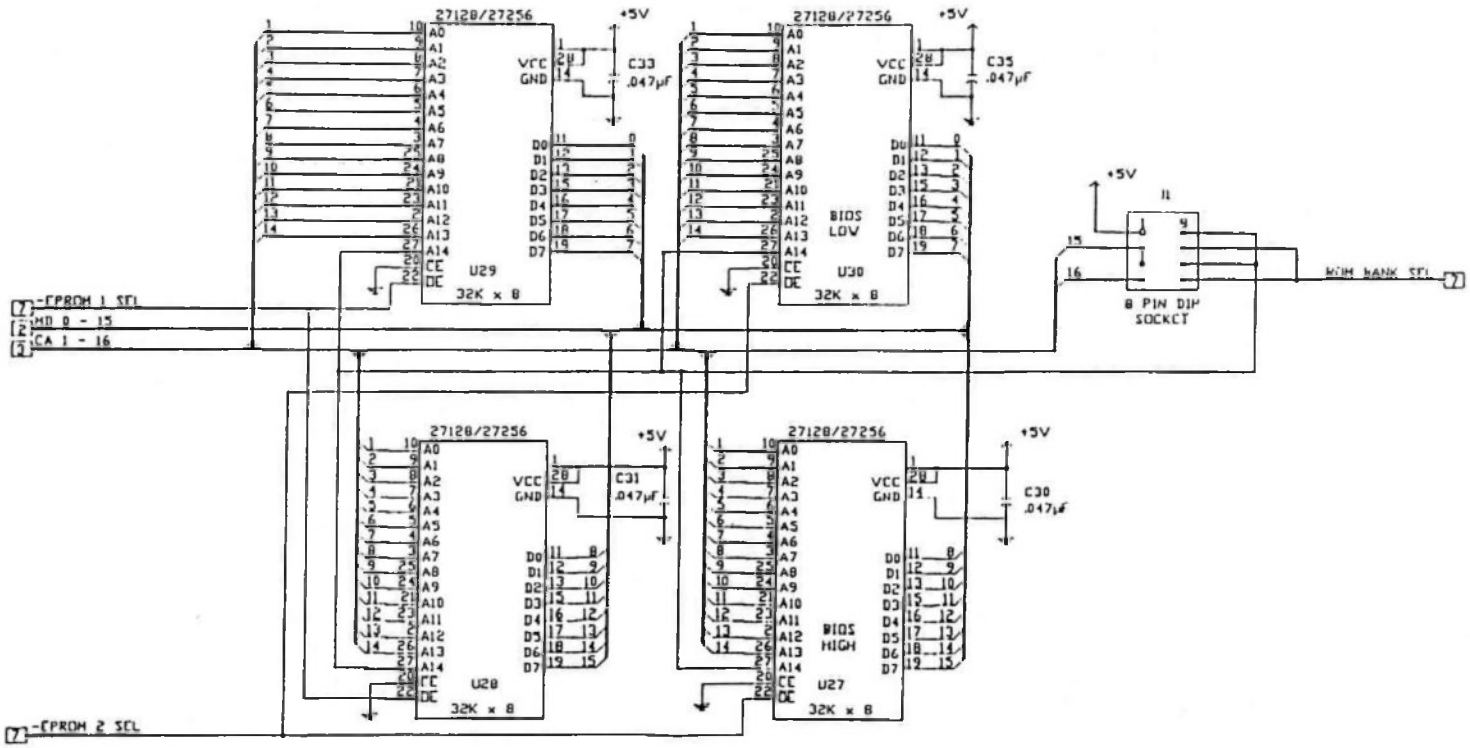

U39
CPU LSI
74ALS08
74ALS04
74LS125
74ALS74
74ALS10
7407
12 MHZ
20MHZ
-RESET
-ALE

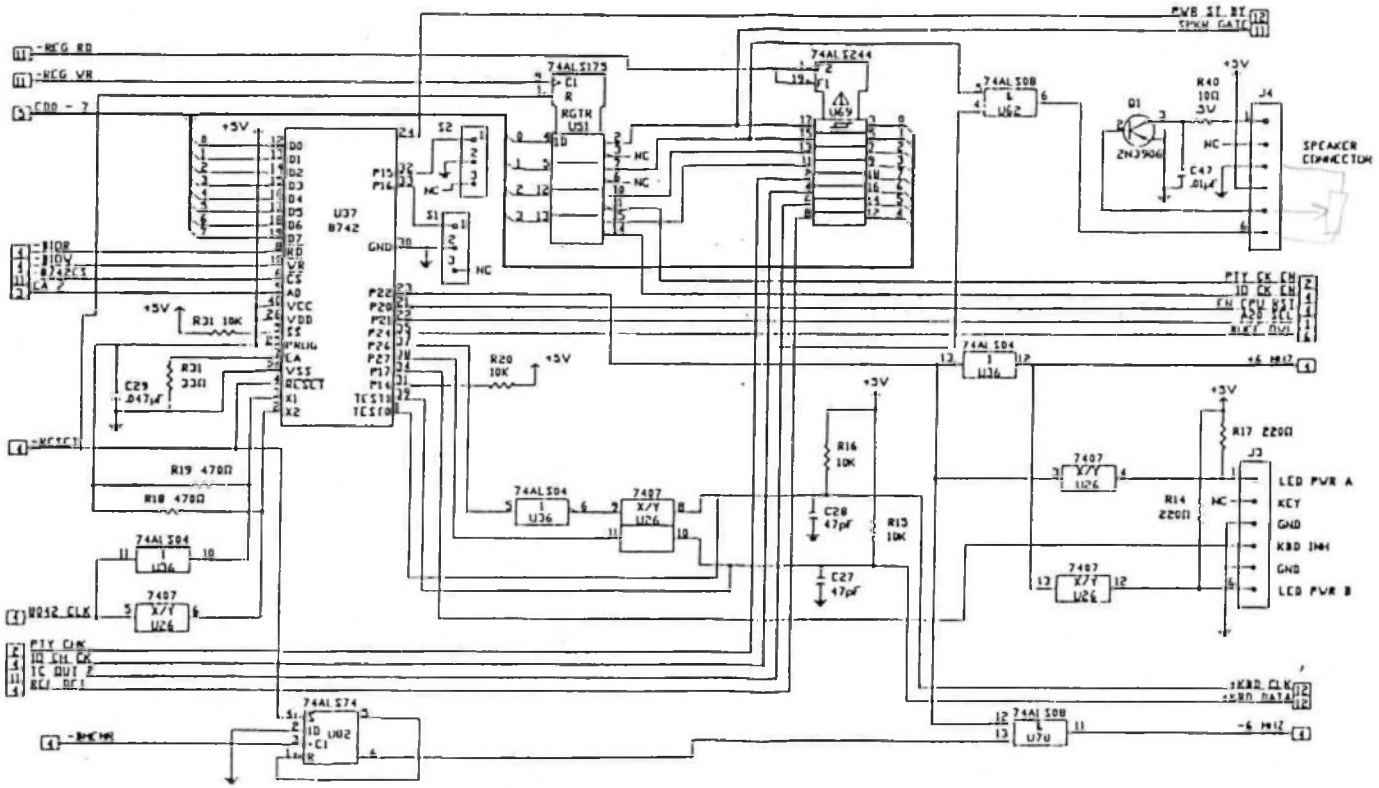

R71 330
R72 330
-CHCMB
-CHCMV
-DMA ACK
BIOW
REFSH
-AUX SEL
74F244
F2
U63
R74 10K
R70 10K
+5V
74ALS00
U50
74ALS00
U49
74ALS04
U62
-DACK0 - 7
74ALS612
STROBE
HE
HA3
HA2
HA1
HA0
MH
MS0
MS1
MS2
MS3
R/W
CS
D0
D1
D2
D3
D4
D5
D6
D7
VCC
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
GND
U38
MD8 NC
MD9 NC
MD10 NC
MD11 NC
74ALS125
U45
CA16
A17
A18
A19
A20
A21
A22
A23
BK DA
-BUS CNTRL
74ALS08
U49
74ALS04
U36
74ALS245
RD SEL
RD DIR
XCVR
U25
U32
CD0 - 7
-ACK
ACK
RD0 - 15
-MCS
-INTA
74ALS51
U21
74ALS138
DIN/OCT
U53
EN
-NP +5V SEL
-DMA2 SEL
INT2 +CAS SEL
-P SEL
-I/O SEL
-INTC1 SEL
-DMA1 SEL
74ALS27
U20
74ALS04
U52
-BIOR
CA0 - 9

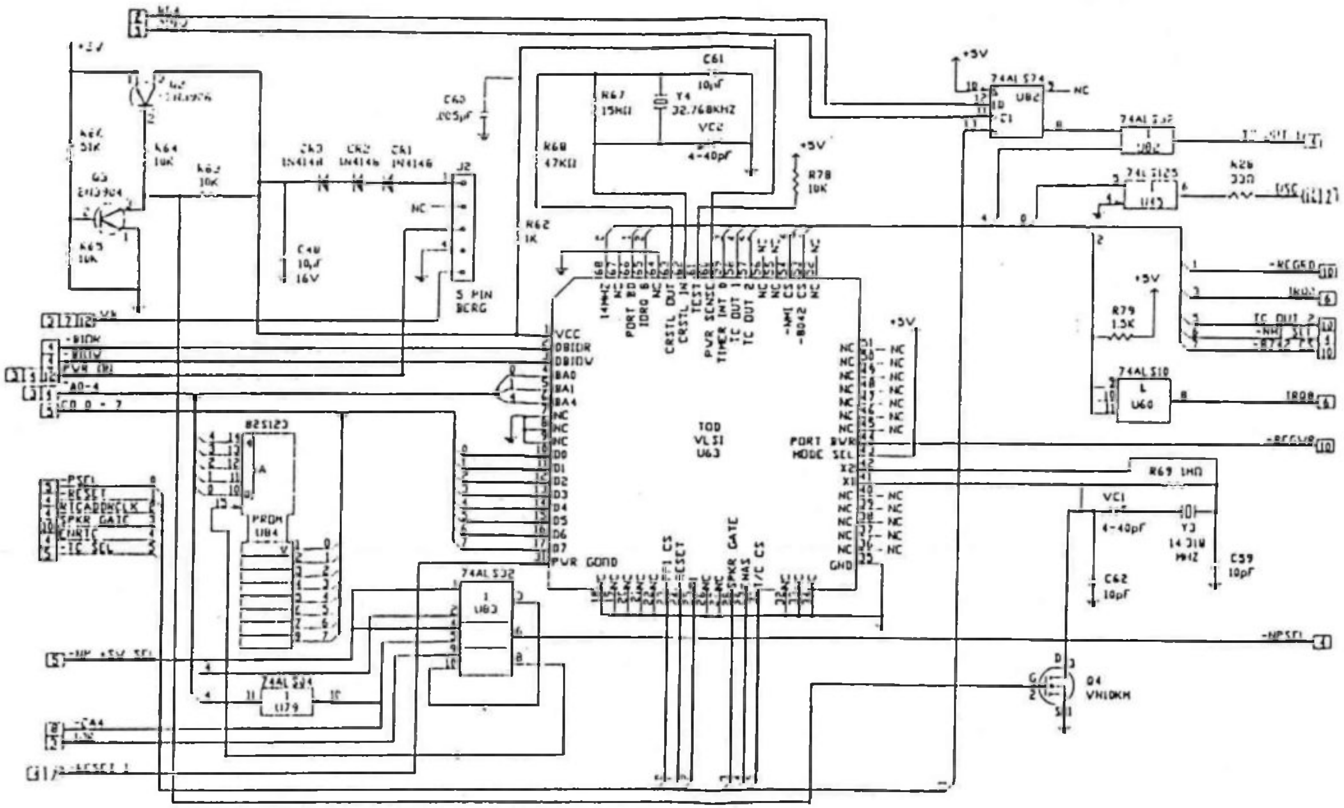

74ALS04
U32
74ALS573 *
RGTR
U56
74ALS573 *
RGTR
U40
-DACK 0-7
8237A
U66
8237A
U55
+5V
C30
.047µF
C41
.047µF
R51
10K
R36
10K
R32
10K
74ALS08
U50
74ALS10
U60
T/C
-DMA AEN1
-DMA AEN 2
INTR
DRQ0 - 3
DRQ5 - 7
-DMA1 SEL
-INTC2 SEL
-BUS CNTRL
-INTA
IRQ0-15
-INTC 1 SEL
DMA HRQ
U67
8259A *
(SLAVE)
U68
8259A *
(MASTER)
R75
10K

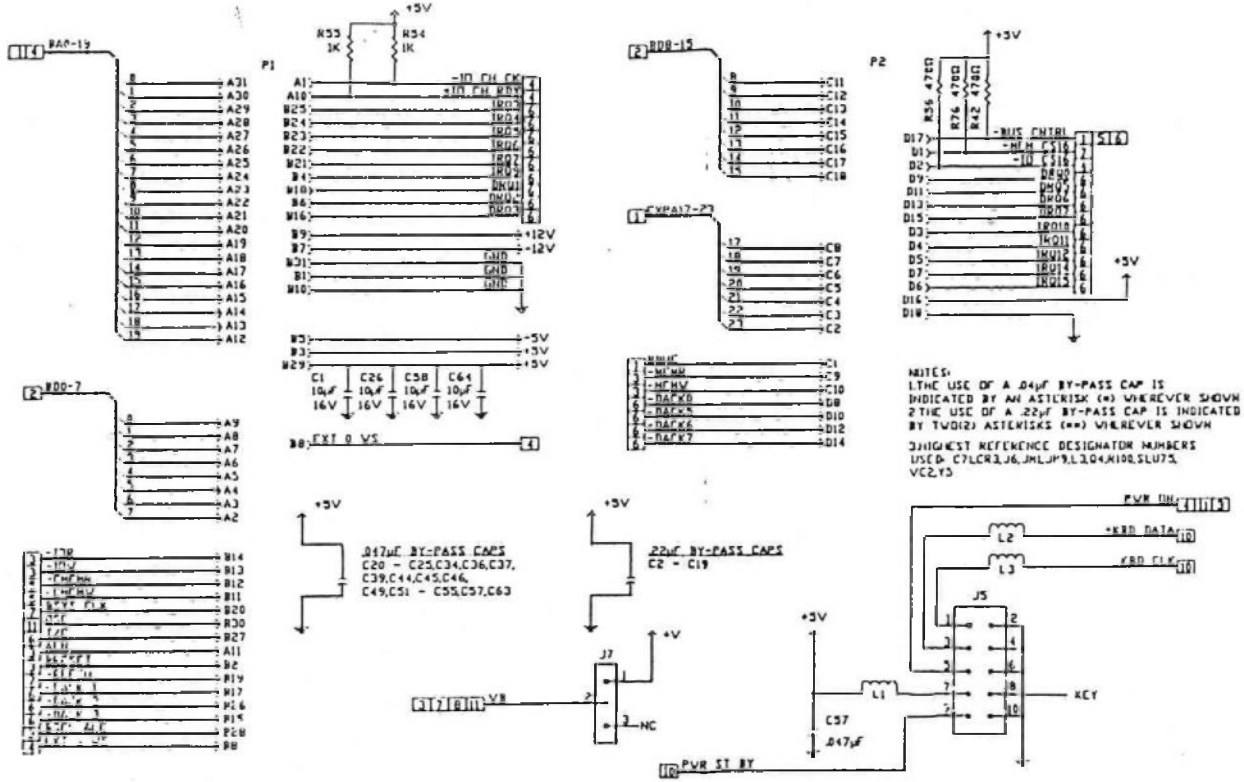

74ALS04
U36
R94 1M
Y5 1MHZ
R103
200K
C67
10µF
C66 10µF
OSC
J6
NC
P FAIL
CLK 286
-REFSH AEN
ROM BANK SEL
-MEM CS16
RAS
JP10
R95
10K
JP7
JP6
JP5
JP4
JP3
74ALS244B
U31
SYSCLK
R21
33Ω
R22
33Ω
74LS51
U21
-ALE
V8
A17-23
-ONBD MEM
+5V
C71
47pF
RAM SEL
MA0-8
RMA0-8
R10 33Ω
R100
10K
-RESET I
-EXP RAM RAS
R7
33Ω
-RAS0
R3 68Ω
R60 68Ω
R13 68Ω
R11 68Ω
CAS0
CAS1
CAS2
CAS3
-MDAT DIR
BUS 16
-AUX SEL
BSYS CLK
DRAM
VLSI
U71
PWR
GND
-EPROM1
-EPROM2
A0
A1
A2
A3
A4
-CASSYS L
-CASSYS H
-CASEXP H
-CASEXP L
A5
A6
A7
A8
F16
+RAMSEL
V8
+0 WAIT ST
-REFSH AEN
-TEST RESET
-RESET
-EXP RAM RAS
-RAM RAS
-REFSH
ROM BANK SEL
-MEM CS 16
+RAS
A23
A22
MA3
MA2
MA5
MA4
S1
S0
MA6
MA9
MA8
MEMS1
PWR DOWN
ADV DECODE
XTAL OUT
XTAL IN
REF RATE
-MEM MAP
MEMS2
CPU CLK
+128 SEL
+A0
+BHE
+CPU HLDA
+ALE
M IO
-XMEMR
MA7
GND
ON BD MEM
MEG CS
+FSYS 16
MDAT DIR
MA0
MA1


TYPICAL PIN ASSIGNMENT
U18
U17
U16
U15
U14
U13
U12
U11
U10
U9
U8
U7
U6
U5
U4
U3
U2
U1
U85
U86
U87
74LS32
74LS74
R104
10K
+5V
JP8
-INIT2 SEL
MD 0 - 15
VB


27128/27256
+5V
C33
.047µF
U29
32K x 8
BIOS
LOW
U30
C35
.047µF
8 PIN DIP
SOCKET
WOM BANK SEL
EPROM 1 SEL
MD 0 - 15
CA 1 - 16
C31
.047µF
U28
BIOS
HIGH
U27
C30
.047µF
EPROM 2 SEL




TOD
VLSI
U63
PROM
U84
82S123
74ALS32
74ALS74
74ALS10
74ALS04
5 PIN
BERG
Y4
32.768KHZ
Y3
14.318 MHZ
Q4
VN10KM
-REGSEL
IRQ3
IRQ8
-REGSVR
-NPSEL


+5V
P1
P2
R33 1K
R34 1K
R35 470Ω
R36 470Ω
R42 470Ω
BAD-19
BDD-7
BDD-15
EXPA17-27
+12V
-12V
C1 10μF 16V
C26 10μF 16V
C58 10μF 16V
C64 10μF 16V
EXT 0 VS
.047μF BY-PASS CAPS
C20 - C25,C34,C36,C37, C39,C44,C45,C46, C49,C51 - C55,C57,C63
.22μF BY-PASS CAPS
C2 - C19
J7
J5
L1
L2
L3
C57 .047μF
PWR SI BY
PWR ON
+KBD DATA
KBD CLK
KEY
NC
NOTES:
1.THE USE OF A .01μF BY-PASS CAP IS INDICATED BY AN ASTERISK (*) WHEREVER SHOWN
2.THE USE OF A .22μF BY-PASS CAP IS INDICATED BY TWO(2) ASTERISKS (**) WHEREVER SHOWN
3.HIGHEST REFERENCE DESIGNATOR NUMBERS USED: C71,CR3,J6,JM1,JP9,L3,Q4,R108,SLU75, VC2,Y3

U NUMBER	PIN NUMBERS +5	GND	UNUSED
1	9	18	5,14
2	9	18	5,14
3	9	18	5,14
4	9	18	5,14
5	9	18	5,14
6	9	18	5,14
7	9	18	5,14
8	9	18	5,14
9	9	18	5,14
10	9	18	5,14
11	9	18	5,14
12	9	18	5,14
13	9	18	5,14
14	9	18	5,14
15	9	18	5,14
16	9	18	5,14
17	9	18	5,14
18	9	18	5,14
19	14	7	3,6
20	14	7	3-6,8-11
21	14	7	11,12
22	14	7	3,6
23	20	10	-
24	20	10	-
25	20	10	-
26	14	7	-
27	8	14	-
28	28	14	-
29	28	14	-
30	28	14	-
31	20	10	4-6,8,12,14-16
32	20	10	-
33	24	12	-
34	24	12	-
35	14	7	-
36	14	7	-

U NUMBER	PIN NUMBERS +5	GND	UNUSED
37	40	20	11,27,28,29,36
38	44	22	6,12,26-28,33
39	63,21	4,22	-
40	20	10	-
41	20	10	-
42	20	10	-
43	30,62		2,3,34-36,38,61
44	9	10,30	4,13
45	14	7	-
46	14	7	1,2
47	16	8	5,6,7,9-14
48	14	7	2-6
49	14	7	-
50	14	7	-
51	16	8	3,6
52	14	7	-
53	16	8	-
54	20	10	5-9,11-15
55	7,34	23	1,6,17,39
56	20	10	-
57	24	12	-
58	24	12	-
59	14	7	-
60	14	7	-
61	14	7	-
62	14	7	-
63	1	35	36-40,45-52,55,56
64	20	10	8,9,11,12
65	20	10	5,7,9,11-15
66	7,34	23	1,6,17,39
67	28	14	-
68	28	14	-
69	20	10	-
70	20	10	9,11
71	[illegible]	[illegible]	-
72	20	10	7,8,9,12-14

U NUMBER	PIN NUMBERS +5	GND	UNUSED
73	14	7	1,2,3,11-13
74	20	10	12
75	20	10	1,9,11-15
76	14	7	6,8
77	14	7	4-6,11-13
78	14	7	-
79	14	7	12,13
80	14	7	6,9,10,12
81	16	-	-
82	14	7	9
83	14	7	-
84	16	8	-
85	14	7	11,12,13
86	14	7	-
87	14	7	1-6
88			
89			
90			
91			
92			
93			
94			
95			
96			
97			
98			
99			
100			
101			
102			
103			
104			
105			
106			
107			
108			

U NUMBER	PIN NUMBERS +5	GND	UNUSED
109			
110			
111			
112			
113			
114			
115			
116			
117			
118			
119			
120			
121			
122			
123			
124			
125			
126			
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136			
137			
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139			
140			
141			
142			
143			
144			

U NUMBER	PIN NUMBERS +5	GND	UNUSED
145			
146			
147			
148			
149			
150			
151			
152			
153			
154			
155			
156			
157			
158			
159			
160			
161			
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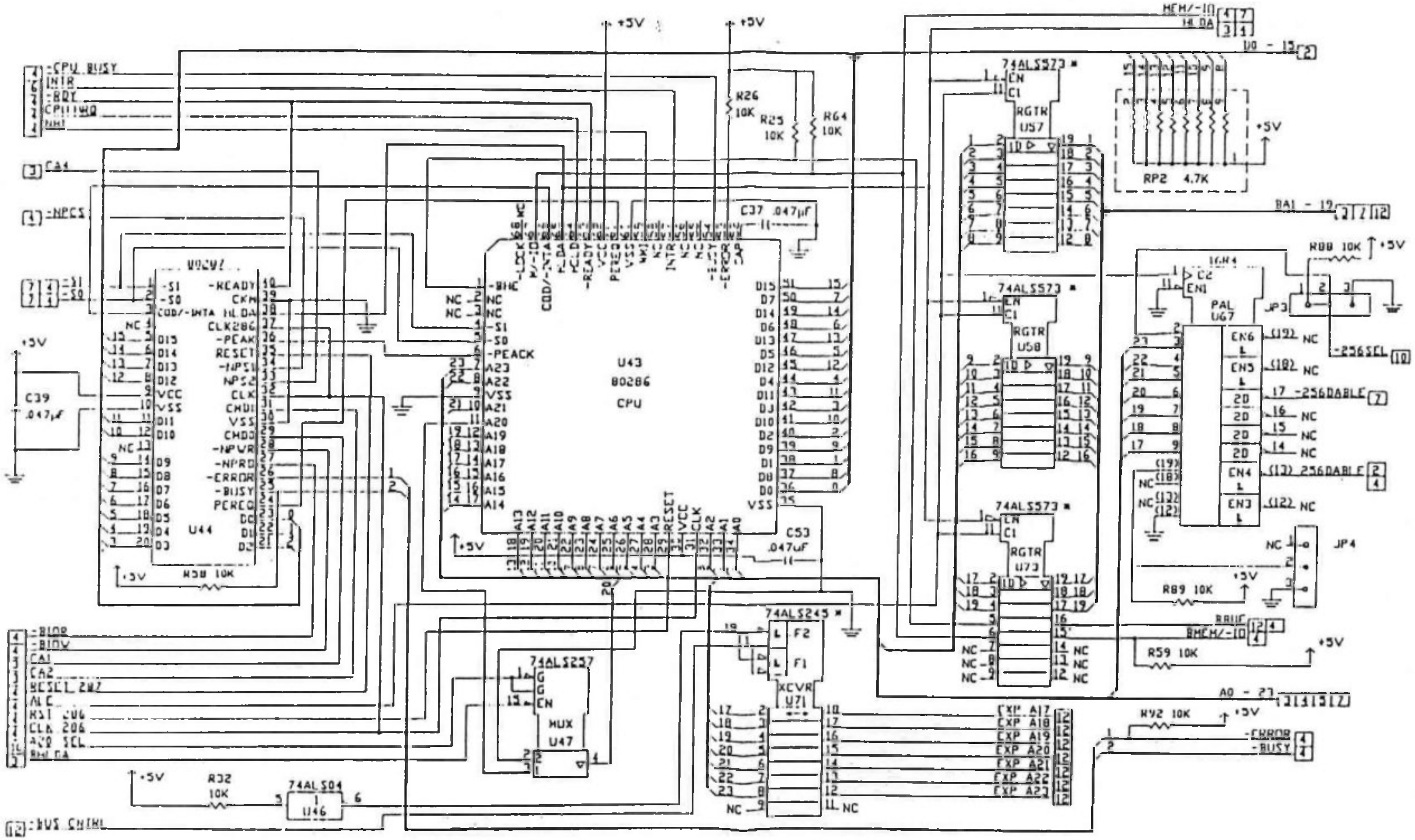
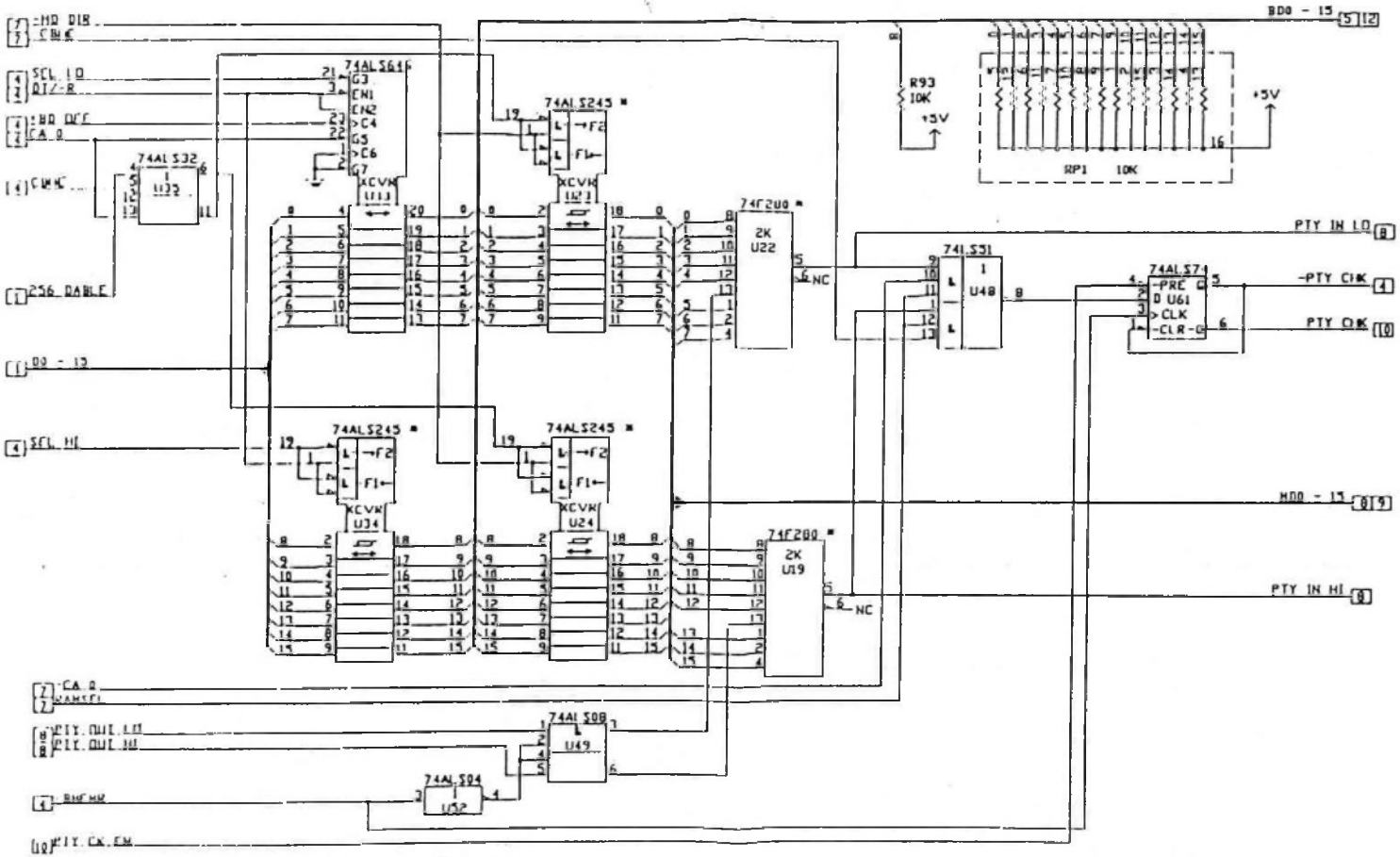
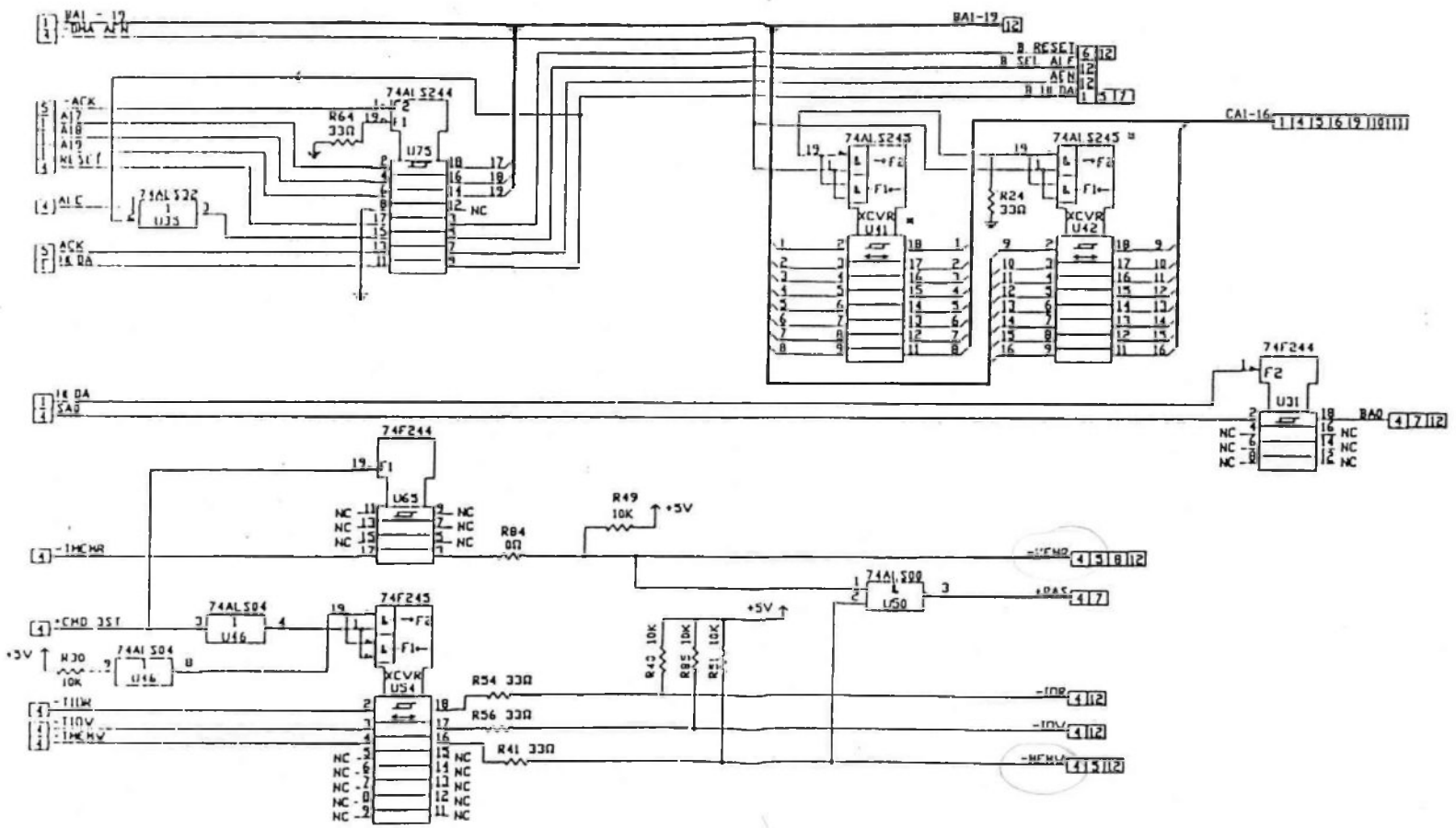
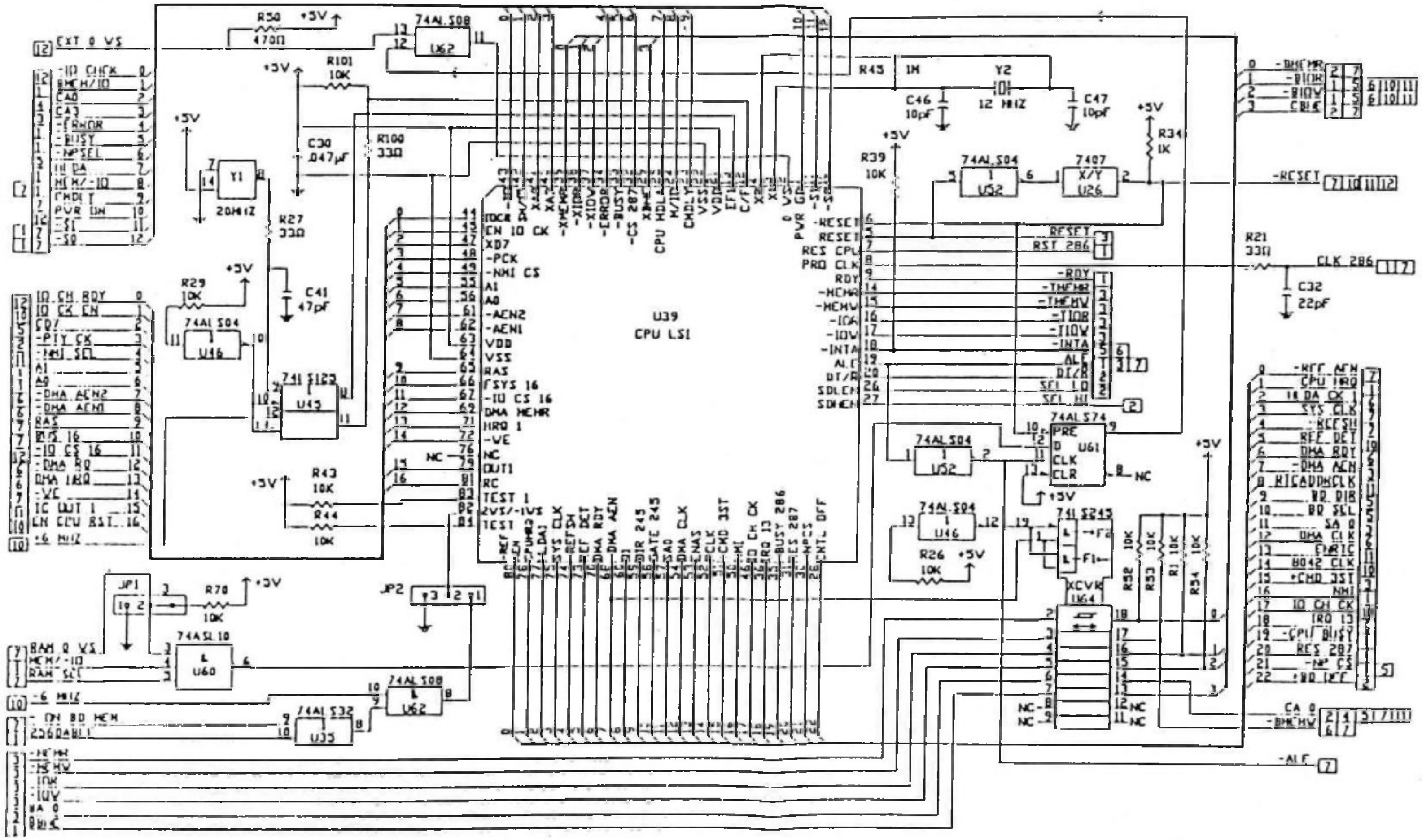
180			

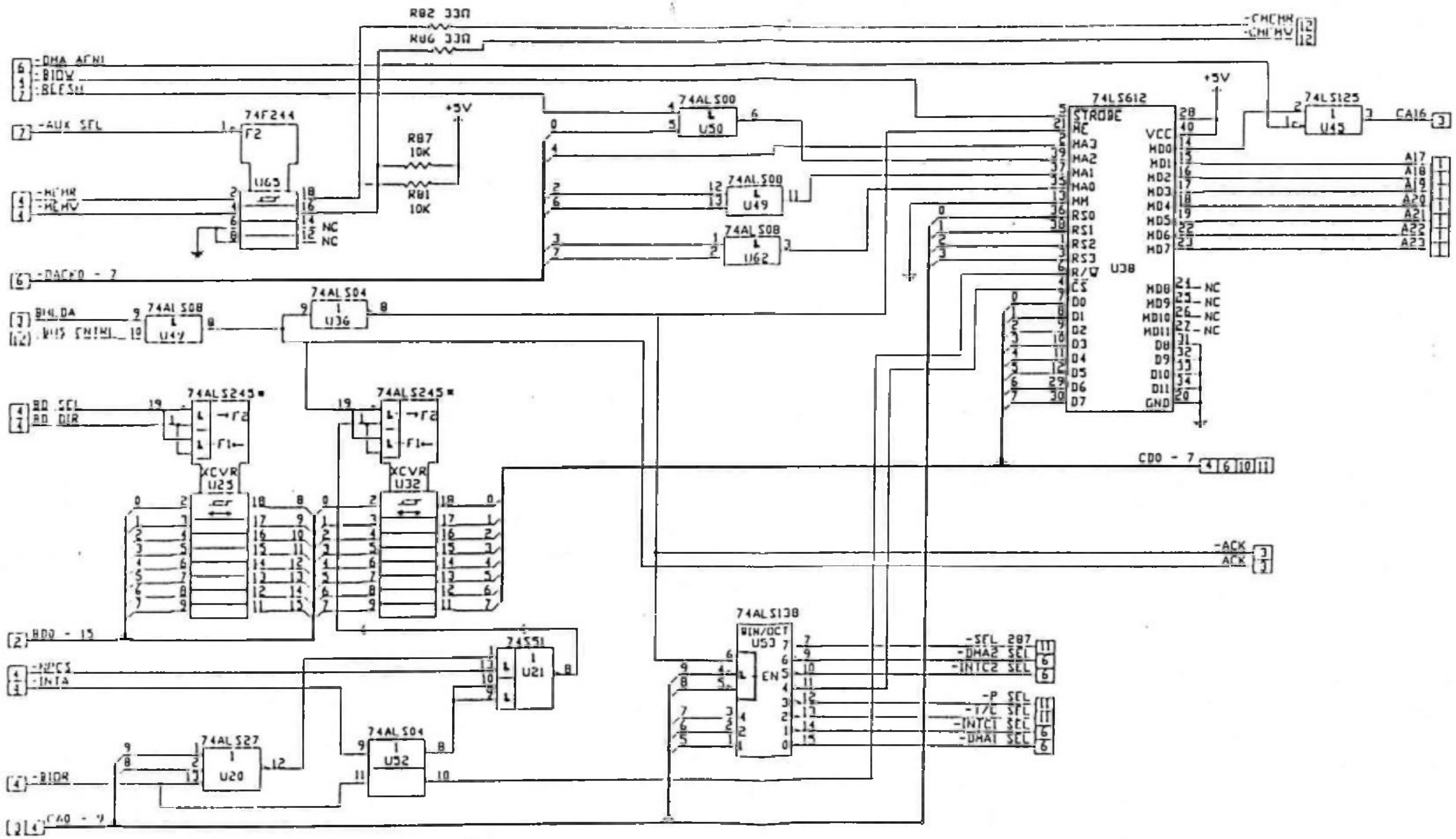
Logic diagrams for the non-power fail recovery processor board are presented in the following pages.

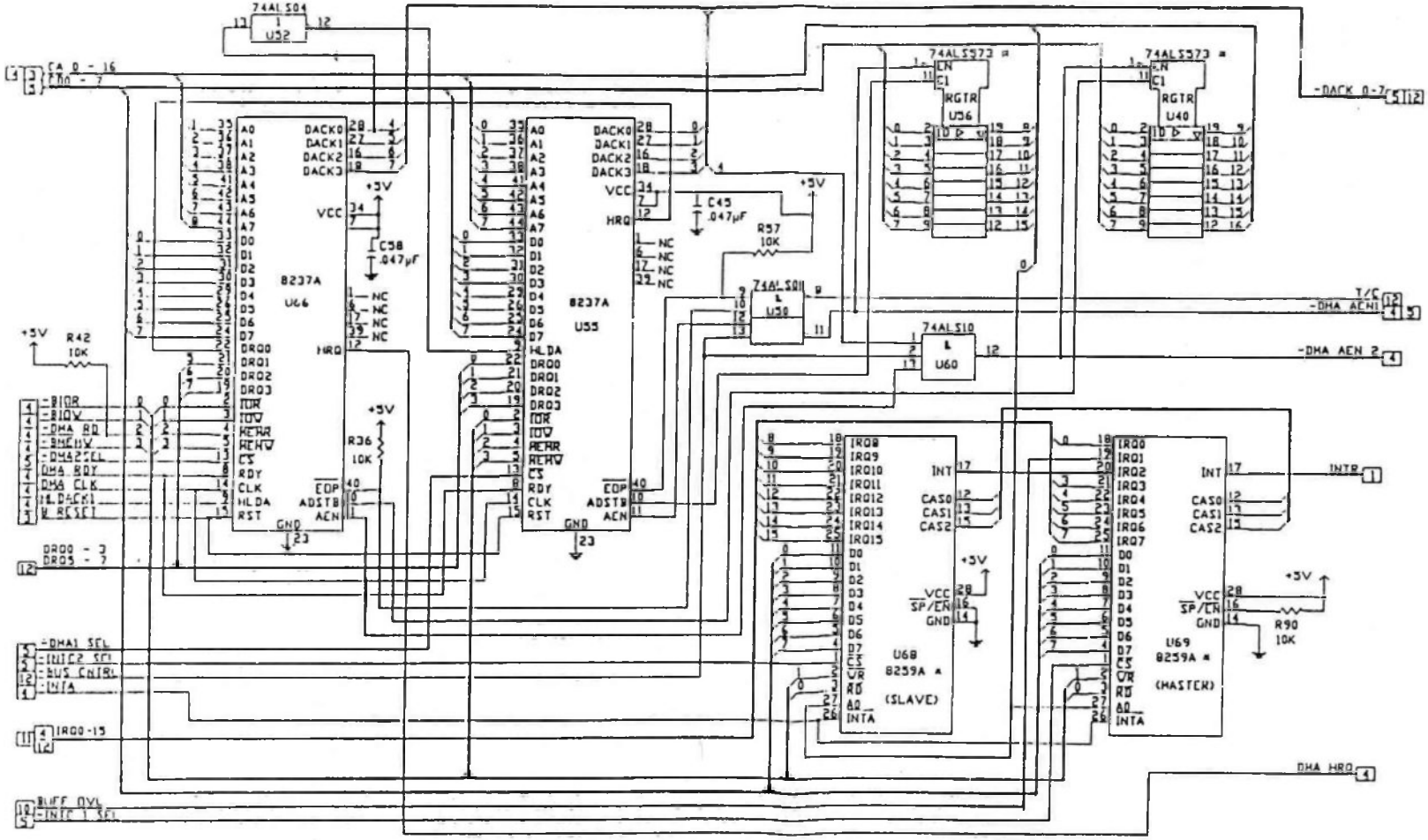

U43
80286
CPU
U44
74ALS573
RGTR
U57
U58
U73
74ALS245
XCVR
74ALS257
MUX
U47
74ALS04
U46
PAL
U67
RP2 4.7K
JP3
JP4
C37 .047μF
C53 .047uF
C39 .047μF
R26 10K
R25 10K
R64 10K
R88 10K
R89 10K
R59 10K
R92 10K
R32 10K
R58 10K
+5V
EXP A17
EXP A18
EXP A19
EXP A20
EXP A21
EXP A22
EXP A23
-ERROR
-BUSY
-256SEL
-256DABLE
NC

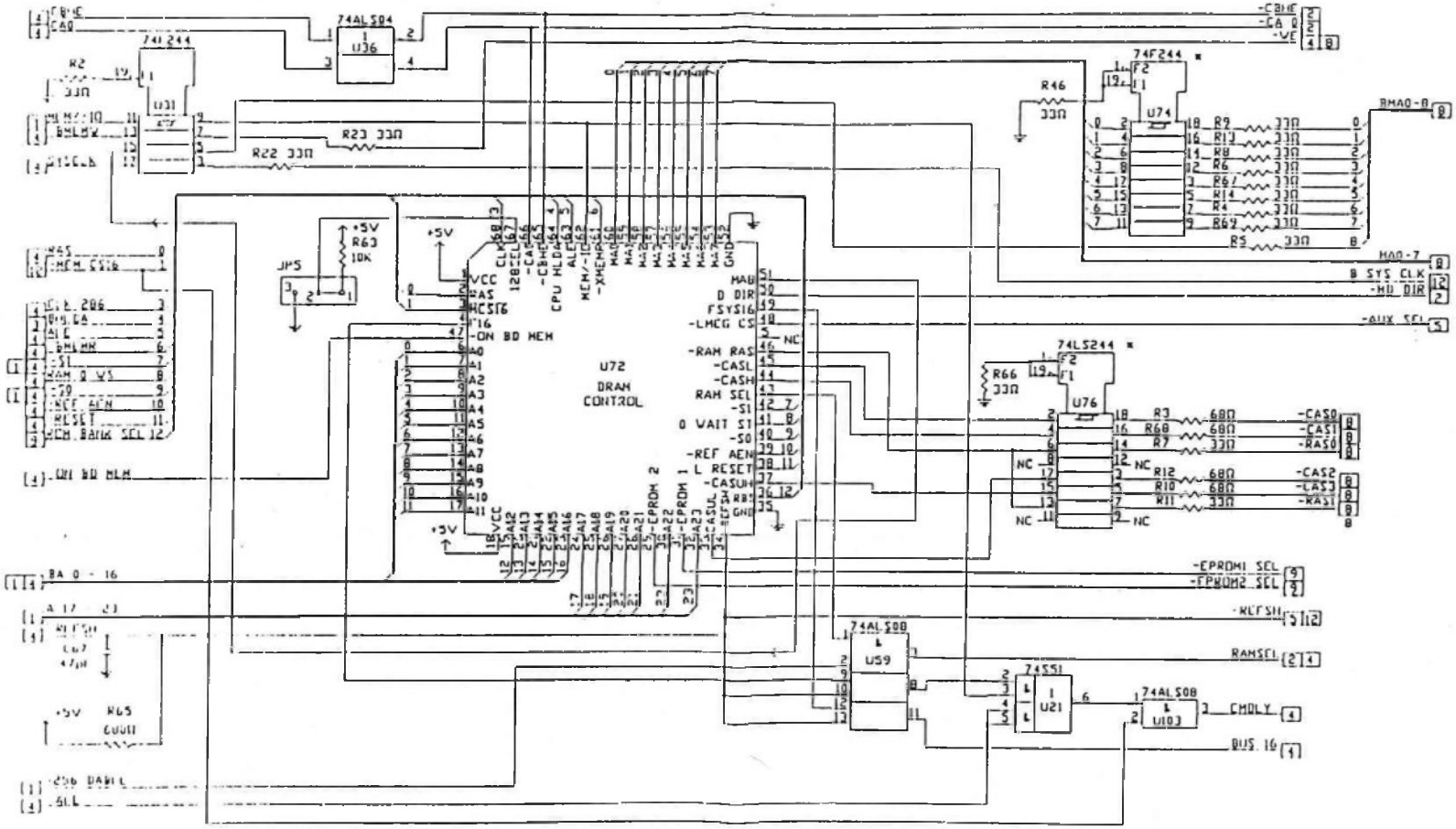

BD0 - 15
R93
10K
+5V
RP1 10K
74ALS641
74ALS245
74ALS32
74F200
2K
U22
74LS31
U48
74ALS74
-PRE
D U61
>CLK
-CLR
PTY IN LO
-PTY CLK
PTY CLK
256 DABLE
BD0 - 15
SCL HI
MDD - 15
PTY IN HI
NC
74ALS245
XCVR
U34
U24
2K
U19
74ALS08
U49
74ALS04
U32

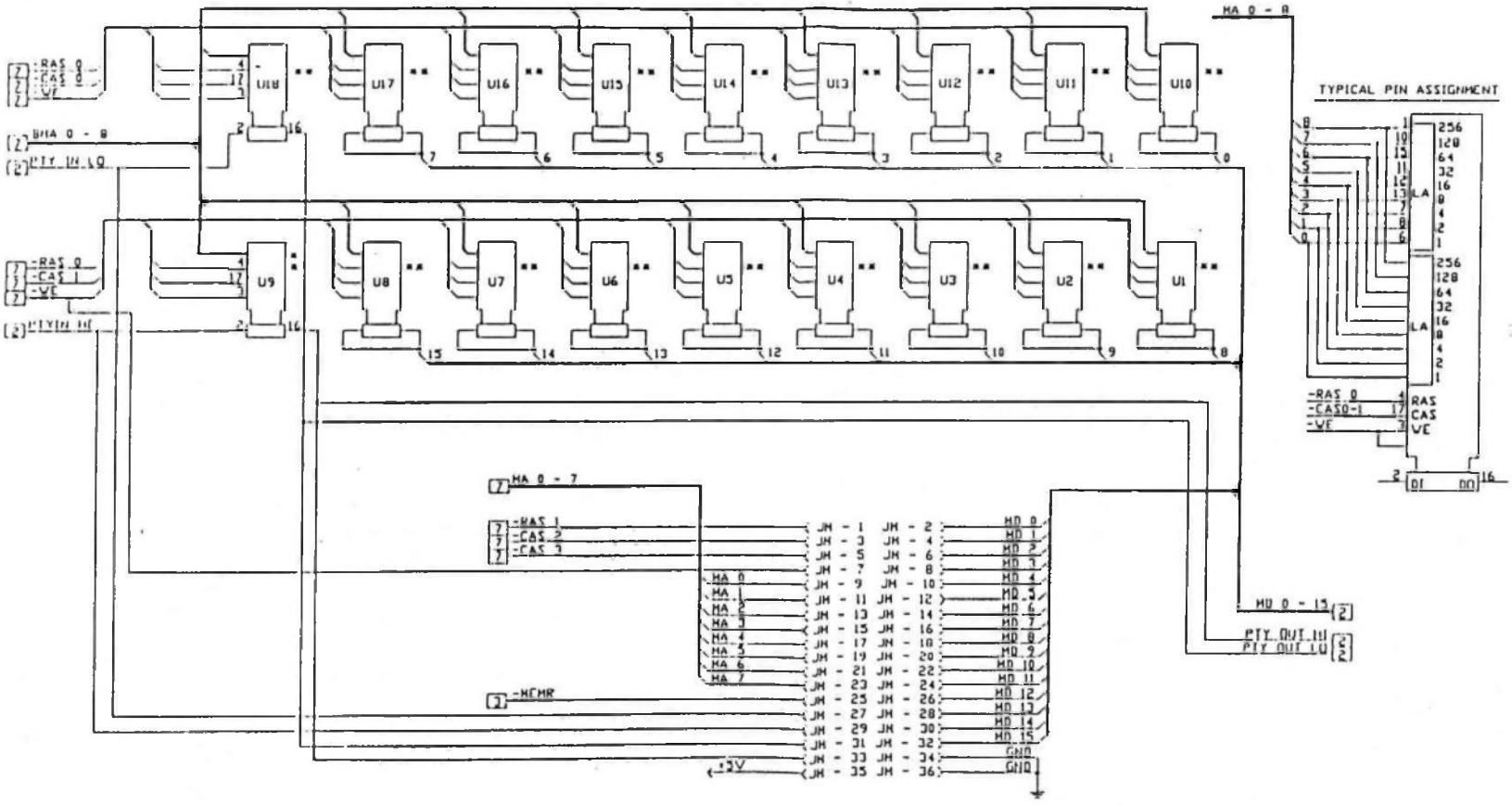

74ALS244
74ALS245
74F244
74F245
74ALS32
74ALS04
74ALS00
XCVR
R64 33Ω
R24 33Ω
R49 10K
+5V
R84 0Ω
R54 33Ω
R56 33Ω
R41 33Ω
R43 10K
R85 10K
R81 10K
R30 10K
NC




R82 33Ω
R86 33Ω
-DMA ACKL
-BIOW
-AUX SEL
74F244
+5V
R87 10K
R81 10K
74ALS00
U50
74ALS00
U49
74ALS08
U62
74LS612
STROBE
VCC
U38
74LS125
U45
CA16
A17
A18
A19
A20
A21
A22
A23
NC
74ALS04
U36
74ALS08
U47
74ALS245
XCVR
U25
U32
CD0 - 7
-ACK
ACK
74ALS138
BIN/OCT
U53
-SEL 287
-DMA2 SEL
-INTC2 SEL
-P SEL
-T/C SEL
-INTC1 SEL
-DMA1 SEL
74S51
U21
74ALS27
U20
74ALS04
U52
-BIOR
-INTA


74ALS04
U52
74ALS573 B
U56
74ALS573 A
U40
8237A
U66
8237A
U55
74ALS11
U39
74ALS10
U60
U68
8259A A
(SLAVE)
U69
8259A A
(MASTER)
R42
10K
R36
10K
R57
10K
R90
10K
C38
.047µF
C43
.047µF
+5V
-DACK 0-7
T/C
-DMA ACK1
-DMA AEN 2
INTR
DMA HRQ
-BIOR
-BIOW
-DMA RD
-DMA WR
-DMA2CEL
DMA RDY
DMA CLK
-DACK1
-RESET
DRQ0 - 3
DRQ5 - 7
-DMA1 SEL
-INIT2 SEL
-BUS CNTRL
-INTA
IRQ0-15
BUFF OVL
-INIT 1 SEL


74ALS04
U36
74F244
U74
74LS244
U76
U72
DRAM
CONTROL
74ALS08
U59
74S51
U21
74ALS08
U103
R46
33Ω
R66
33Ω
R63
10K
JP5
+5V
-ON BD MEM
-EPROM1 SEL
-EPROM2 SEL
RAMSEL
CMDLY
BUS 16
MA0-7
B SYS CLK
-MU DIR
-AUX SEL
-CAS0
-CAS1
-RAS0
-CAS2
-CAS3
-RAS1


MA 0 - 8
TYPICAL PIN ASSIGNMENT
-RAS 0
-CAS 0
-WE
MA 0 - 7
-RAS 1
-CAS 2
-CAS 3
-MCMR
+5V
MD 0 - 15
PTY OUT HI
PTY OUT LO
GND