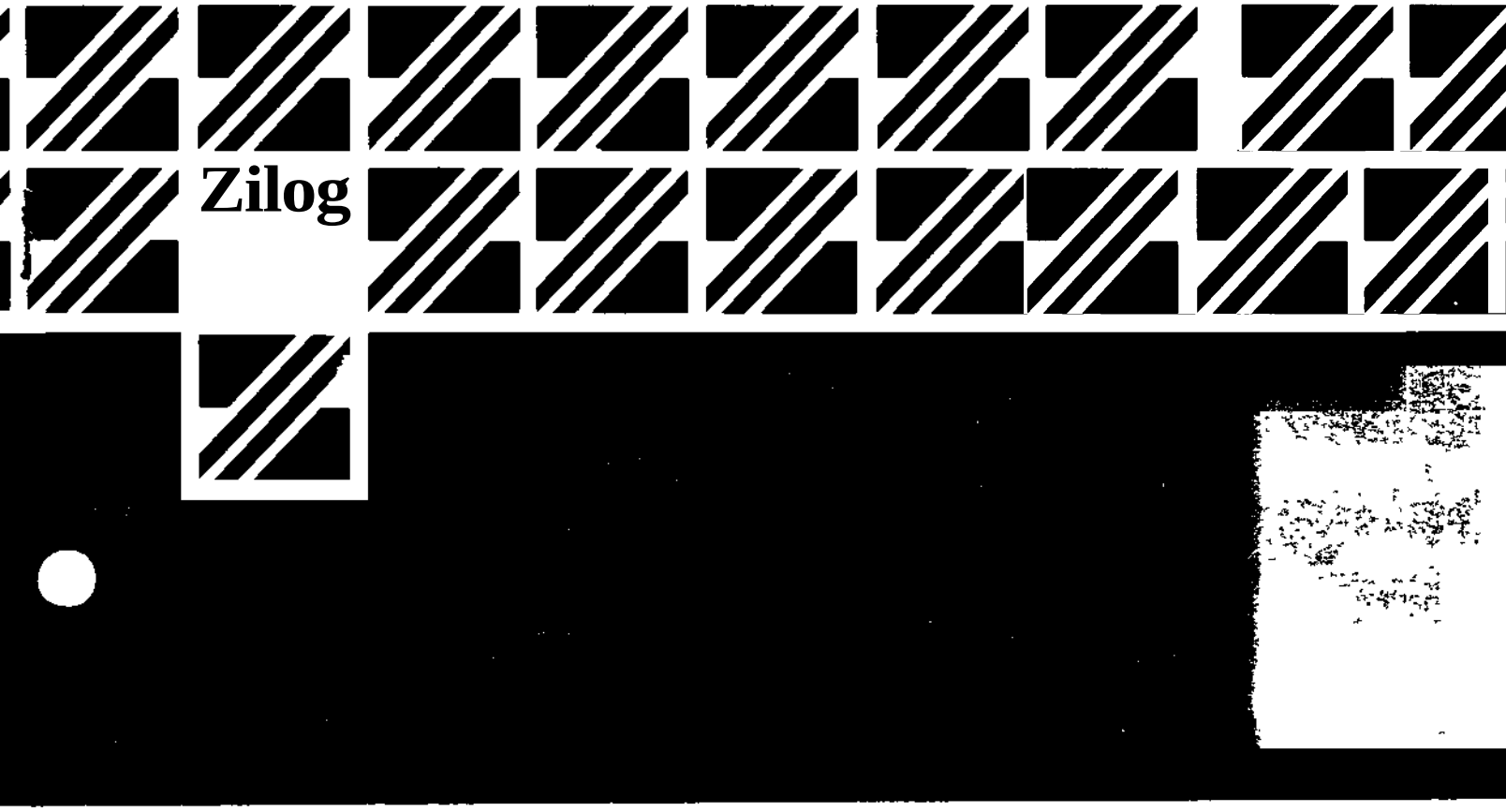
Zilog

# Z80®-AIO/AIB

## Hardware User's Manual



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# Z80 - AIO/AIB
HARDWARE USER'S MANUAL

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# Z80-AIO USER'S MANUAL

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SECTION PAGE

# AIO USER'S MANUAL

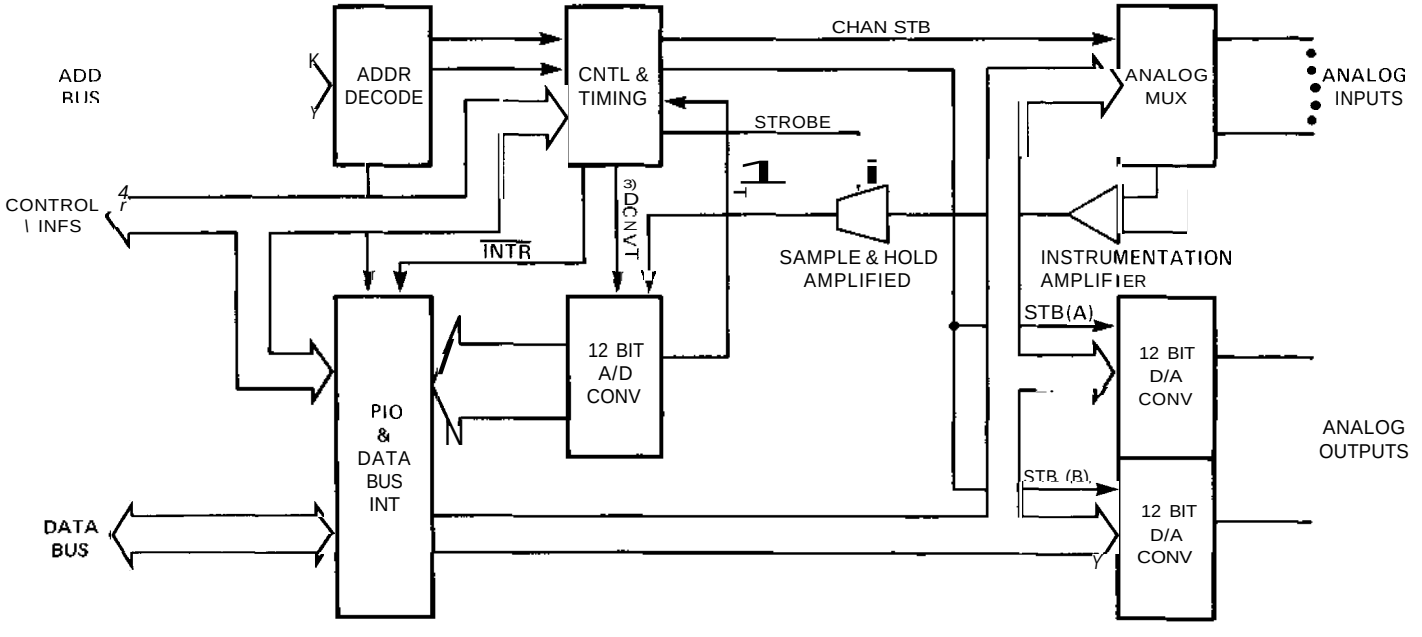
## SECTION 1; GENERAL INFORMATION

### 1.1 Product Description

The Z80-AIO is a 12-bit analog input/output card, compatible with the Z80 Microcomputer Board Series.

The analog to digital portion can accept 16 differential or 32 single-ended channels with input voltages ranging from (+/-) 2.5mV full scale to (+/-) 10V full scale. The digital to analog portion provides two, 12-bit D/A Converters with double buffering to minimize output switching transients. The Output voltage is selectable for bipolar or unipolar Operation with Output voltages ranging from (+/-) 2.5V full scale to (+/-) 10V full scale. This analog system is interfaced as I/O to the CPU and may operate in a polling or interrupt mode. I/O addressing may be changed by on-board jumper selections.

### 1.2 Block Diagram



## SECTION 2: INSTALLATION

### 2.1 Introduction

The following section contains Information on initial unpacking and inspection, power and Signal connections to the MCB, and Installation of the AIO Board or AIB in the MCZ l series Systems.

### 2.2 Initial Unpacking and Inspection

Inspect the product for shipping damage as soon as it is unpacked. Check for any physical damage that may be attributed to abuse and handling during shipment. If the product is damaged in any way, notify the carrier immediately.

### 2.3 Installation (MCZ-1)

The Analog Boards may be installed in either of the prewired I/O board positions in the MCZ-1/20 or MCZ-1/25 Systems. These positions are J2 and J3 as described in the MCZ Hardware User's Manual. Jl, an undedicated and unwired position, may also be used. In the MCZ-1/30 System, Jl, J2 and J3 of each card cage, may be used in the identical manner as previously described. In the MCZ-1/05, -1/10 and PDS, Jl (User's Option) and J4 (Video Display Board) will directly accommodate the Analog Boards.

## 2.4 Power and Signal Connections

The Z80 AIO and AIB are pin-compatible with the Z80 MCB bus structure. For convenience, the wire list for interconnection between the MCB and the Analog Boards is provided:

| TO | FROM | DESCRIPTION |
|---|---|---|
| AIO:l-3, 59-51 | MCB:l-3, 59-61 | +5V P.S. |
| AIO:4 | MCB:4 | IORQ- |
| AIO:5 | MCB:5 | DATA BIT (5) |
| Next IEI | AIO:6 | IEO of AIO/AIB |
| AIO:7 | Last used IEO | IEI Of AIO/AIB |
| AIO:8 | MCB:8 | DATA BIT (3) |
| AIO:12 | MCB:12 | DATA BIT (6) |
| AIO:13 | MCB:13 | DATA BIT (0) |
| AIO:23 | MCB:23 | WR- |
| AIO:26 | MCB:26 | ADDR. BIT (7) |
| AIO:29 | MCB:29 | ADDR. BIT (5) |
| AIO:30 | MCB:30 | ADDR. BIT (6) |
| AIO:62-64, 120-122 | MCB:62-64, 120-122 | COMMOM |
| AIO:68 | MCB:68 | DATA BIT (4) |
| AIO:71 | MCB:71 | DATA BIT (2) |
| AIO:73 | MCB:73 | DATA BIT (7) |
| AIO:75 | MCB:75 | DATA BIT (1) |
| AIO:79 | MCB:79 | INT- |
| AIO:98 | MCB:98 | ADDR. BIT (4) |
| AIO:99 | MCB:99 | PHI- |
| AIO:100 | MCB:100 | ADDR. BIT (3) |
| AIO:101 | MCB:101 | ADDR. BIT (2) |
| AIO:102 | MCB:102 | ADDR. BIT (1) |
| AIO:103 | MCB:103 | ADDR BIT (0) |
| AIO:115 | MCB:115 | Ml- |
| AIO:116 | MCB:115 | RD- |

TABLE 2.3.1: MCB TO AIO OR AIB WIRE LIST

## SECTION 3: OPERATION

### 3.1 Introduction

This section contains a general description of the Analog Boards' Operation, and provides some application Software for initializing and communicating to the AIO and AIB.

### 3.2 Description

Interfacing the AIO or AIB to the System bus is accommodated by the on-board PIO and is addressed as I/O. The ADDRESS DECODER uses ten addresses to direct all board operations.

By selecting the PIO port A or B control addresses, the PIO may be programmed to Interrupt the CPU System and supply an Interrupt vector address upon completion of an A/D conversion. The CONTROL and TIMING will gate the requested analog input channel to the ANALOG MULTIPLEXER, strobe the SAMPLE and HOLD AMPLIFIER and request conversion of the A/D CONVERTER. Upon completing the conversion, the A/D CONVERTER will respond to the PIO through the CONTROL and TIMING that the converted data is ready. At this time, the PIO may Interrupt the System or the System may read the Status register to find that the conversion data is ready and the results have not previously been read.

Each 12-bit D/A converter has two I/O ports for the eight least significant bits and the four most significant bits of the data word. The 12-bit data word is formed and presented to the DAC inputs for conversion when the most significant byte is output.

## 3.3 Address Modification

The AIO or AIB Interfaces to the Z80 MCB I/O bus, occupying ten locations in the I/O address space. The first four locations are required for the PIO. The next two locations are used to transfer the input channel address and board Status while the remaining locations are used for passing data to the two D/A Converters.

| I/O ADDR. | FUNCTION |
|---|---|
| 80 | PORT A data |
| 81 | PORT B data |
| 82 | PORT A Control |
| 83 | PORT B Control |
| 88 | Address Register (Sel. Ch. No.) |
| 89 | Status Register |
| 8C | Low byte DAC l Register |
| 8D | High byte DAC l Register |
| 8E | Low byte DAC 2 Register |
| 8F | High byte DAC 2 Register |

TABLE 3.3.1: PREWIRED I/O ADDRESSES

The board, as received from the factory, is wired to occupy those locations shown in Table 3.3.1. However, it is possible to move the onboard PIO and the board registers independently throughout the I/O address space. The only limitations upon address selection are that the PIO and board registers cannot occupy the same locations, and the three most significant address bits must be the sänne.

Address modification is achieved by removing the existing address selection Jumpers and then installing those indicated in Tables 3.3.2 and 3.3.3 for the desired address. Wherever a "one" occurs in the address, the High jumper should be installed. Wherever a "zero" occurs, the Low jumper should be installed.

| ADDRESS BIT | HIGH | LOW |
|---|---|---|
| 2 | JP39 | JP38 |
| 3 | JP41 | JP40 |
| 4 | JP30 | JP31 |
| 5 | JP32 | J`33 |
| 6 | JP27 | JP26 |
| 7 | JP28 | JP29 |

TABLE 3.3.2. PIO Address Selection Jumpers.

| ADDRESS BIT | HIGH | LOW |
|---|---|---|
| 3 | JP37 | JP36 |
| 4 | JP34 | JP35 |
| 5 | JP32 | JP33 |
| 6 | JP27 | JP26 |
| 7 | JP28 | JP29 |

TABLE 3.3.3. Register Address Selection Jumpers.

## 3.4 Input/Output Handling

Inputting of data can be accomplished in one of two modes; Polling and Interrupt. These modes operate as follows:

Polling Mode - During initialization of the PIO, the Interrupt enable flag must be reset to prevent the generation of Interrupts. When a conversion is desired, it is initiated by writing the Analog Channel Address to the address register. The program must then periodically test the conversion bit in the status register to determine v/hen the conversion is complete.

Interrupt Mode - After setting the board's PIO Interrupt enable and vector address, conversion is started by writing to the address register. The program execution can then continue until the end of conversion has occurred. At that time, the PIO generates an Interrupt vector causing the CPU to begin execution of the Interrupt Service routine.

Outputting Data - Outputting of data to the AIO's two D/A Converters is straight-forward. The two 12-bit D/A Converters have separate I/O addresses for the upper and lower bytes of the data word. A word is formed by loading the eight least significant bits into a latch where they are buffered from the D/A inputs until the final four bits of the data word are received. The combined 12-bits of data are

then gated simultaneously to the D/A inputs. This double buffering scheme prevents conversion of partial words, and therefore, eliminates spiking in the Output Signal.

## 3.5 Application

### 3.5.1 Input Range Selection

The data acquisition System has been jumpered for (+/-)10V Operation. Other ranges are possible and can be selected as shown in Table 3.5.1.1.

| RANGE | JUMPERS |
|---|---|
| (+/-)10V | W8*, W7*, W9*, W10* |
| (+/-)5V | W8*, JP21, W9*, W10* |
| (+/-)2.5V | W8*, JP20, JP21, W9*, W10* |
| 0 to +10V | JP23, JP21, JP25, JP43 |
| 0 to +5V | JP23, JP20, JP21, JP25, JP43 |

TABLE 3.5.1.1. Input Range Setting Jumpers.

All jumpers marked with an asterisk (*) are installed at the factory and are implemented by a plated-through hole connecting pads on the upper and lower surfaces of the board. These can be removed by careful manual drilling with a 0.055" (#54) drill. All other jumpers are wire and should be sleeved wherever a possible short could occur.

When the range is changed, those existing jumpers that are not used for the new range must first be removed, and then the installation of the additional jumpers performed.

The analog to digital Converter Output data is normally presented in 2's complement format for bipolar ranges. For straight binary Operation remove wire Jumper W9 and install JP25.

### 3.5.2 Output Range Selection

Each DAC is jumpered at the factory for (+/-)10 volt Operation and two's complement coding (Table 3.5.2.2). However, it is possible to alter these jumpers as shown in Table 3.5.2.1 for other Output voltages. Jumpers indicated by an asterisk are plated-through holes on the board and should be removed by careful manual drilling with a 0.055"

(#54) drill. When making a change, first remove those jumpers indicated for the present range, and replace them with those jumpers required for the desired range.

| RANGE | JUMPERS DAC 1 | DAC 2 |
|---|---|---|
| (+/-)10V | W1*, W2* | W3*, W4* |
| (+/-)5V | JP11, W2* | |
| (+/-)2.5V | JP11, W2*, JP9 | JP15, W4*, JP13 |
| 0 to +10V | JP11, JP8 | JP15, JP12 |
| 0 to +5V | JP11, JP8, JP9 | JP15, JP12, JP13 |

TABLE 3.5.2.1. Output Range Selection Jumpers.

When converting from bipolar to unipolar Operation, W5* should be removed and JP7 installed. This converts from two's complement Operation to straight binary.

Bipolar - Two's Complement

| Digital Input/Output | (+/-)10V | (+/-)5V | (+/-)2.5V |
|---|---|---|---|
| 0111...11 (7FFH) | +9.9951V | +4.9975V | +2.4988V |
| 100...00 (800H) | -10.0000V | -5.0000V | -2.5000V |

Unipolar - Straight Binary

| Digital Input/Output | 0 to +10V | 0 to +5V |
|---|---|---|
| 111...111 (FFFH) | 9.9975V | 4.9988 |
| 000...00 (000H) | 0.0000V | 0.0000V |

TABLE 3.5.2.2. Analog Input and Output Full Scale Range Values.

3.5.3 Differential-Single Ended Selected

The board, as received from the factory, is wired for differential input. The input System can be changed from differential to single-ended or vice versa by simply changing several jumpers. W6* is required for differential Operation, and JP16 and JP18 are required for single-ended Operation. W6* is a plated-through connection and should be removed by careful manual drilling with a 0.055" (#54) drill.

Differential Operation is generally used to minimize common mode noise during low level Operation. Single-ended operation is suitable for large input Signals. However, a noise reduction of ten-to-one can be achieved in single-ended

Operation by making a "pseudo differential" connection. This involves sensing the ground at the signal source rather than at the board. To use this method, all input Signals must be on the same ground System at their source.

Pseudo-differential Operation occurs when jumper JP18 has been removed and JP1 is installed.

### 3.5.4 Input System Low Level Operation

When it is desired to operate the input system instrumentation amplifier at other than unity gain for low level Signals, a simple change of the gain setting resistor is all that is required. R8 and the optional parallel resistor R9 form this resistance. The value of the gain setting resistor can be calculated from the following formula:

$$R = \frac{20K}{G - 1}$$

Stable (10 ppm/deg C) wire-wound resistors should be used.

Increasing the amplifier gain also increases its settling time. As a result, the System delay timer must be extended by increasing the value of R15 and the optional parallel resistor R14. Delays and values of R15 versus Gain are shown in Table 3.5.4.1.

| Amplifier Gain | Delay Time (us) | R15 (+20%) |
|---|---|---|
| 1 | 20 | 9.5K |
| 10 | 30 | 14.3K |
| 100 | 40 | 19K |
| 1000 | 100 | 47.5K |

TABLE 3.5.4.1. Delay Time vs. Amplifier Gain.

### 3.5.5 Input System Application

The data acquisition System, incorporated into the AIO or AIB, uses a fixed timing sequence between channel selection and the Start of data conversion. If desired, this time may be increased by the addition of an external resistor and capacitor. This procedure is described in the low level Operation section.

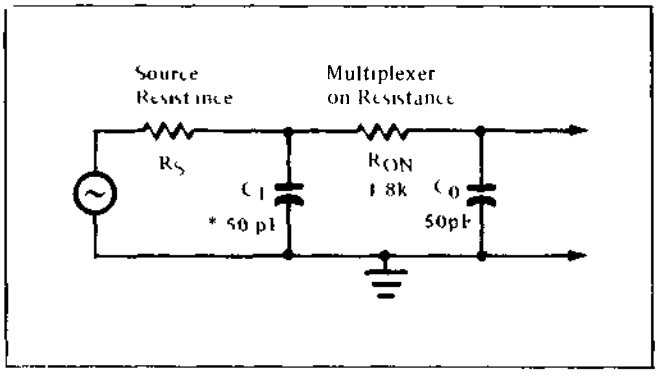



FIGURE 3.5.5.1. On Channel Multiplexer Circuit for Single-Ended Operation.

For a gain of 1 (set at factory), multiplexer settling time is 20us which is sufficient for most application. The only external factor which affects the multiplexer settling time is the output impedance (Rs) of the source connected to a channel. A circuit roodel of an "Cn" channel is shown in Figure 3.5.5.1. The input capacitance (C1) of 50pF for single-ended Operation does not affect the settling time since it is continuously connected to the source. The Signal at the Output of the multiplexer must be allowed to settle to (+/-)0.01% (nine time constants) to maintain the full accuracy of the System. The multiplexer time constant can be calculated with the formula: Ts = (Rs + Ron) Co. For a source resistance of 1k, Ts = (1 + 1.8k) x 50pF = 14 Ons. Thus, 1.20us is needed to settle to +0.01%. This is well below the fixed 10us allowed for multiplexer settling. The accuracy of the System, is therefore, preserved.

If the source bandwidth can be limited, high impedance sources may be accurately handled by placing a large capacitor across the multiplexer input. An analysis of such a circuit shows that a capacitor of 0.5uF is sufficient. For such a capacitance, the multiplexer time constant becomes 90ns. If this method cannot be used, the time allowed for settling can be increased as described in the section on low level Operation.

For switching of large Signals, it must be remembered that the on resistance is the channel resistance of a FET which is a nonlinear function of the applied voltaqes. As a result, the previous calculations are only an approximation derived from a linearized mode. Another factor not considered in the above calculation is the addressing delay of the multiplexer. This is typically 250ns and is additive to the above calculated times.

For differential units, the same considerations apply. Even though two input circuits are involved, there is sufficient component matching within the multiplexer to prevent measurable differences in the transfer functions for each half of the Signal. When operated in the differential mode, Co in Figure 3.5.5.1 becomes 12.5pF with an Ron = 1.8k in each leg. Therefore, the time constant becomes one-half the time constant for the single-ended channel.

The analog inputs have reversed-biased diode circuits which prevent damage from discharge of static electricity. However, it is still wise to take reasonable precautions against static discharge.

### 3.5.6 Thermocouple Temperature Acquisition

Thermocouples are often used as temperature sensors for process control Systems. Thermocouples are characterized by temperature coefficients of 10 to 70uV/deg C and operating ranges of minus hundreds to plus thousands of degrees centrigrade. When the AIO or AIB is operated with an Instrumentation amplifier gain of 100 or more, it may be connected directly to these devices. The wires running from thermocouple measuring devices often pick up large common-mode noise Signals of 60 Hz or higher frequencies.

The high common-mode rejection of the Instrument amplifier will reject common-mode noise. To minimize differential mode noise, the Signal wire should be twisted, and if possible, shielded. As a rule, an unshielded twisted pair is better than a coax but a shielded twisted pair is best.

The remote sensor should be earth-grounded to prevent common-mode voltages from exceeding the +5 volt ränge of the multiplexer. To complete a thermocouple System, it is necessary to terminate all thermocouple wire pairs at an isothermal box or connector strip of some type. An ordinary

barrier strip may be monitored to allow the observed thermocouple cmf to be cold-junction compensated. Figure 3.5.6.2 shows a circuit for this purpose. The Output is connected to one of the input channels to supply ambient temperature data to the System computer. Output sensitivity is approximately 2 mV/deg C.

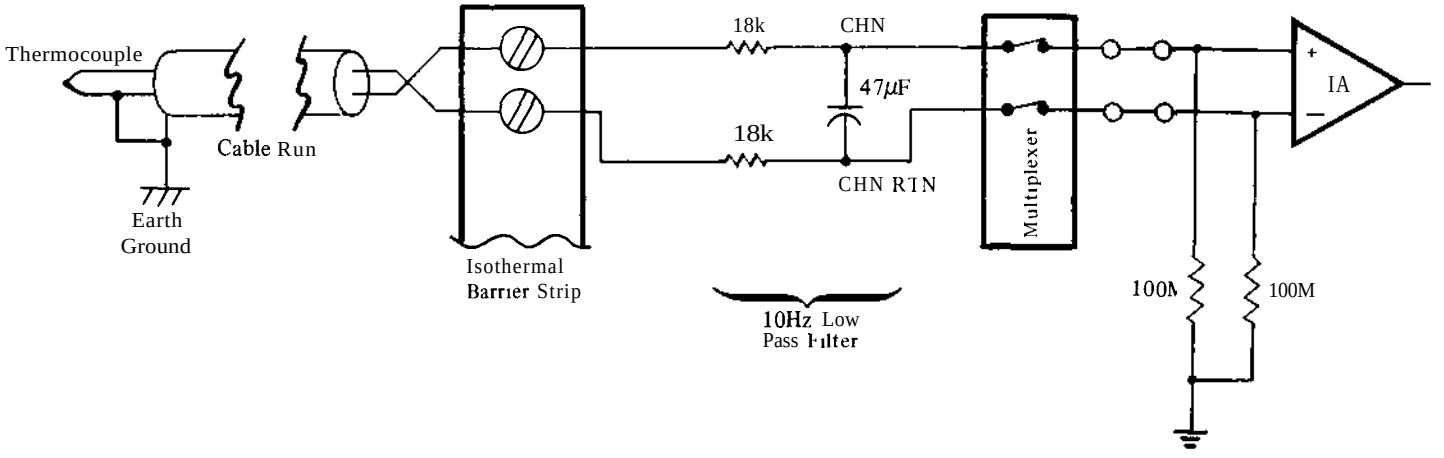
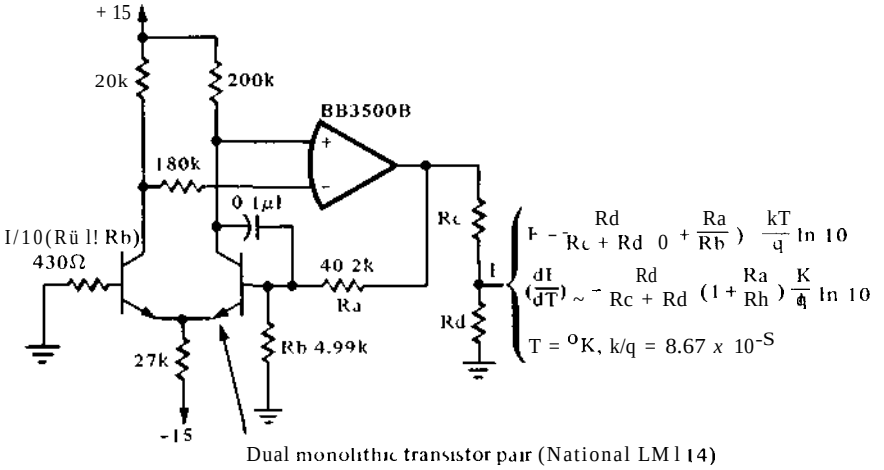



FIGURE 3.5.6.1: Thermocouple Input System




Dual monolithic transistor pair (National LM114)
Mounted Near Isothermal
Barner Strip

FIGURE 3.5.6.2: Ambient Temperature Sensor

## SECTION 4: PROGRAMMING AND INITIALIZATION

### 4.1 Introduction

The following section contains information and programming examples for analog input/output Operation.

### 4.2 Input Programming

The first four locations (80H-83H), are used to program the onboard PIO. A detailed description of the PIO's Operation can be found in the Zilog Z80-PIO Product Specification. Normal Operation of the board reauires programming the PIO as follows:

Polling Mode - Both A and B Mode Control registers must be set for input (mode 1). When Mode l is active, data from the analog to digital Converter can be input to the processor. In addition, the Interrupt Enable must be turned off. The following initialization program illustrates the procedure.

```
DI                  ;  DISABLE INTERRUPT
LD A, 4FH
OUT 82H, A          ;  SET PORT A FOR MODE l
OUT 83H, A          ;  SET PORT B FOR MODE l
LD A, 07H
OUT 82H, A          ;  DISABLE PORT A INTERRUPT
OUT 83H, A          ;  DISABLE PORT B INTERRUPT
IN A, 80H           ;  INITIALIZE CONVERSION READ F.F.
IN A, 81H           ;  INITIALIZE CONVERSION READ F.F,
```

The remaining board locations are treated as described in the following paragraph discussing non-PIO locations.

Interrupt Mode - As in the Polling Mode, the A and B Mode Control Registers must be set for Input (Mode 1). The PIO Interrupt System is enabled by loading the interrupt vector address and setting the interrupt enable. Only Port 3 interrupt enable should be set. The following program illustrates the procedure. In addition to initializing the PIO, the program also loads the Z80's Interrupt Vector Register.

```
DI                  ;  DISABLE INTERRUPT
LD A, N
LD I, A             ;  (LOAD I VECTOR REGISTER
                       WITH NUMBER (N))
LD A, M             ;  SET PIO INTERRUPT VECTOR
OUT 83H, A
LD A, 4FH
OUT 82H, A          ;  SET PORT A FOR MODE 1
OUT 83H, A          ;  SET PORT B FOR MODE 1
LD A, 07H           ;  DISABLE PORT A INTERRUPT
OUT 82H, A
LD A, 87H           ;  SET PORT B INTERRUPT
OUT 83H, A
IN A, 80H           ;  INITIALIZE PORT A DATA
IN A, 81H           ;  INITIALIZE PORT B DATA
IM 2                ;  SET INTERRUPT MODE 2
EI
```

The remaining non-PIO locations are programmed as follows:

Non-PIO Location - Location 88H specifies the particular analog input channel to be digitized. Writing the channel number (0-20H) into the Address Register at this location will cause a conversion to be performed.

The Status Register (See Figure 4.3.1) at location 89H provides data on A/D Performance. Bit 0 indicates that a conversion is in progress by displaying a 0 during this time and a 1 at all other times. Bit 1 is 0 after a conversion has been performed and then changes to 1 after the first complete reading of the converted data.

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | READ STATUS | A/D STATUS |

(X: indicates unused)

FIGURE 4.3.1 STATUS REGISTER BIT LOCATIONS

## 4.3 Output Programming

As shown in Table 3.3.1, the two digital to analog Converters occupy locations 8CH - 8FH. Either Converter is programmed by loading the least significant eight bits of data into its Low Byte location. The most significant four bits of data are then loaded into the right most bit locations of the converter's high data byte. The most significant four bits of this byte are unused. Figure 4.3.2 illustrates this bit placement.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | LOW BYTE PORT ADDRESS (8CH OR 8EH) | | | | | | |
| DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | HIGH BYTE PORT ADDRESS (8DH OR 8FH) | | | | | | |
| X | X | X | X | DB11 | DB10 | DB9 | DB8 |

FIGURE 4.3.2. DAC BIT PLACEMENT

## SECTION 5: TESTING

### 5.1 Introduction

The following section contains information on suggested test equipment and test aids, calibration procedure, and a description of the available calibration and test routines for the AIO and AIB on the MCZ-1.

### 5.2 Test Equipment and Aids

Calibration is performed by connecting a precision voltage source capable of 0.005% accuracy or by using a DC voltage source of less absolute accuracy, the Output of which is monitored by a five digit DVM capable of (+/-) 0.005% accuracy. To utilize the MCB-1 system-based loop test described in section 5.4, test routines 15 and 16, a test plug is used to Jumper the analog Output of DAC l to the single- ended analog inputs of channeis 0-15 and the analog Output DAC 2 to the single-ended analog inputs channeis 16-31. The wire list for connecting the back panel connectors 2 and 3 to accommodate this test arrangement is as follows:

| TO | FROM | DESCRIPTION |
|---|---|---|
| J2:6-9, 18-21 | J2:3 | DAC 1-OUT TO CH 0-7 |
| J3:l-4, 14-17 | J2:3 | DAC 1-OUT TO CH 8-15 |
| J2:10-13, 22-25 | J2:15 | DAC 2-OUT TO CH 16-23 |
| J3:5-8, 18-21 | J2:15 | DAC 2-OUT TO CH 24-31 |

TABLE 5.2.1: Test Plug Wire List

## 5.3 Calibration

### Input System Calibration

System calibration is typically performed on a single channel while running the following program. The program assumes that the Polling Mode initialization has been performed as described in the Programming section.

```
AD:     LD BC, OH
        LD D, 64H
AE:     LD A, 0          ;LOAD ADDR. REG WITH CH. #
        OUT 88H, A
AC:     IN A, 89H        ;IS CONVERSION COMPLETE?
        AND 01H
        JP NZ, AC        ;NO.
        IN A, 80H        ;YES. READ DATA
        LD L, A
        IN A, 81H
        LD A, L          ;IS DATA = LOW REF.?
        SUB REF          ;REF = OH FOR OFFSET ADJ.
                         REF = FFH FOR GIAN ADJ.
        JP Z, AA
        INC C            ;NO. INCREMENT COUNT
        JP AB
AA:     INC B            ;YES. INCREMENT COUNT
AB:     DEC D            ;HAVE 100 CONVERSIONS BEEN
                         ;PERFORMED?
        JP NZ, AE
AF:     JP AD            ;YES. REPEAT
        END
```

The program has been written to accommodate factory preset addresses. If the board responds to other addresses, the program references to I/O locations must be made to conform with these new locations.

After assembling and loading, insert a breakpoint at location AF. The offset and gain adjustments on the System are made while applying the voltages shown in Table 5.3.1. The offset voltage adjustment is made at the most negative value of the ränge, less 1/2 least significant bit (LSB). An LSB is equal to the span (full scale ränge) divided by 4096 for 12-bit resolution. The gain adjustment is made at the most positive ränge, less 3/2 LSB. Thus, for a ränge of (+/-) 10V

an LSB is 20V/4096 = 4.88mV. The offset adjustment is made at -10V + 2.44mV = -9.9976V and the gain adjustment at +10V -7.32mV = +9.9926V. Before making these adjustments, however, the unit should be allowed to reach thermal equilibrium (about 30 minutes under power).

The offset adjustment is made first. The calibration program is then run, and after 100 conversions, it will halt at the break point. The contents of B and C registers should be compared. The contents of Register B is the number of times the conversion results exactly matched the reference value. The contents of Register C is the number of times the conversion results did not match the reference value. Ideally, Register B should have a value of 64H and Register C should have a value of 0. However B = 50 and C = 50 indicates an acceptable offset or gain adjustment setting.

The gain adjustment is roade in much the same manner. However, the value of REF is changed from 0 to FF. The appropriate gain voltage is then applied, and the calibration procedure performed as described for the offset adjustment.

| Range | Offset | Gain |
|---|---|---|
| (+/-)10V | -9.9976V | +9.9926V |
| (+/-)5V | -4.9988V | +4.9963V |
| (+/-)2.5V | -2.4994V | +2.4981V |
| 0 to +10 | +1.22mV | +9.9953V |
| 0 to +5 | +0.61mV | +4.9981V |

TABLE 5.3.1: Data Acquisition Calibration Values

Note: RV5: ADC gain adjustment
RV6: ADC offset adjustment

## Output System Calibration

The Output system is calibrated through the use of the following program.

```
START:  LD A, LSB           ;LSB = 0H FOR OFFSET ADJ.
                             LSB = FFH FOR GAIN ADJ.

        OUT (DACL),A        ;OUTPUT LSB TO DAC LOW BYTE REG.
        LD A, MSB           ;MSB = 0F8H FOR BIPOLAR OFFSET
                             MSB = 0H FOR UNIPOLAR OFFSET
                             MSB = 7H FOR BIPOLAR GAIN
                             MSB = 0FH FOR UNIPOLAR GAIN

        OUT (DACH), A       ;OUTPUT MSB TO HIGH BYTE REG.
        JP START
        DACL EQU XX         ;XX IS THE I/O ADDR OF DACL I.E. 8CH
                            ;OR 8EH
        DACH EQU XX         ;XX IS THE I/O ADDR OF DACH I.E. 8DH
                            ;OR 8FH
        END
```

Before tbe program is assembled, DACL and DACH must be set to the I/O addresses of the low and high bytes of the digital to analog Converter to be calibrated.

After assembling and loading, a breakpoint should be set at the Jump instruction. When the program has been run, the desired Converter will be set at its most negative Output. The DAC should then be set by its offset control for its most negative full scale Output value, as shown in Table 5.3.2. However, before making this adjustment, the board should be allowed to reach thermal equilibrium -- about 30 minutes under power.

After the Offset adjustment has been made, the appropriate values of LSB and MSB for Gain adjustment must be deposited into the program. The previous procedure must then be repeated, but adjust the gain control for the most positive full scale Output value.

| Range | Low | High | l LSB |
|---|---|---|---|
| (+/-)10V | -10.000V | +9.9951V | 4.8848mV |
| (+/-) 5V | -5.000V | +4.9976V | 2.4414mV |
| (+/-) 2.5V | -2.500V | +2.4987V | 1.2207mV |
| 0 to +10V | 0.0V | +9.9975V | 2.4414mV |
| 0 to +5V | 0.0V | +4.9988V | 1.2207mV |

TABLE 5.3.2: DAC Calibration Values

Note: RV1: DAC1 gain adjustment
RV2: DAC2 gain adjustment
RV3: DAC2 offset adjustment
RV4: DAC1 offset adjustment

## 5.4 System Test

The following tests are provided with the Analog Board and are applicable to the operating Systems available in the MCZ-1 Series Systems. The test's titles and descriptions are given in the table below.

Test l - DAC l Bilpolar Offset

Description

When the program has been run, DAC l will be set at its most negative Output. The DAC should then be set by its offset control for its most negative full scale Output value as indicated in Table 5.3.2. RV4 is the offset adjustment control for DAC 1.

Test 2 - DAC l Bipolar Gain

Description

When the program has been run, DAC l will be set at its most positive output value. The DAC should then be set to its most positive full scale Output value for the selected range, as indicated in Table 5.3.2. The gain control for DAC l is RVl.

Test 3 - DAC l Unipolar Offset

Description

This test is performed in the same manner as Test 1.

Test 4 - DAC l Unipolar Gain

Description

This test is performed in the same manner as Test 2.

## Test 5 - DAC 2 Bipolar Offset

### Description

This test is performed in the same manner as Test 1. The offset adjustment control for DAC 2 is RV3.

## Test 6 - DAC 2 Bipolar Gain

### Description

This test is performed in the same manner as Test 2. The gain control for DAC 2 is RV2.

## Test 7 - DAC 2 Unipolar Offset

### Description

This test is performed in the same manner as Test 5.

## Test 8 - DAC 2 Unipolar Gain

### Description

This test is performed in the same manner as Test 6.

Note: Before making any of these adjustments, the board should be allowed to reach thermal equilibrium, about 30 minutes under power. Additionally, the gain and offset controls may contain some lash-back and should be alternately rechecked after initial adjustment.

## Test 9 - Data Acauisition - Bipolar Offset

### Description

The offset adjustment is made at the most negative value of the selected ränge less one-half the least significant bit. The values are shown for the selected range in the Data Acguisition Calibration Table 5.3.1. The test will check the actual conversion value against the expected conversion value and respond with the message "Turn Control Clockwise", or "Turn Control Counter Clockwise". When the actual value is within (+/-)20H of the expected value for 100 consective conversions, the program will exit with the message message "Control set Correctly" and "Test ?". The offset adjustment control is RV 6.

## Test 10 - Data Acauisition - Bipolar Gain

### Description

The gain adjustment is made in much the same manner as the offset adjustment. The appropriate gain value from the Data Acauisition Table for the selected ränge is applied in the calibration procedures performed as described for the offset adjustment. The gain adjustment control is RV5.

## Test 11 - Data Aquisition - Unipolar Offset

### Descr iption

This test is performed in a similar manner to Test 9 using the appropriate values from the Table 5.3.1.

## Test 12 - Data Acauisition - Unipolar Gain

### Description

This test is performed in a similar manner to Test 10 using the appropriate values from the Table 5.3.1.

## Test 13 - Generate Ramp DAC l

### Description

This test generates a ramp from a chronological sequence exercising the DAC to its minimum and maximum values of the conversion ränge. The test is intended for observation only and does not imply that monotinicity and linearity can be measured or accurately observed with standard laboratory equipment.

## Test 14 - Generate Ramp DAC 2

### Description

This test is the same as Test 13 and applies to DAC 2.

## Test 15 - Bipolar Continuity Test - Pulling Mode

### Descr iption

This test checks for missing codes by feeding the analog Output into the analog input and comparing the conversion results of the A/D Converter to the data word of the D/A converter. If the actual conversion word is within (+/-)1 LSB of the expected conversion word, then the test will increment to the next chronological D/A word and perform the test again. This process is continued until the entire ränge of conversion is tested for that analog input channel. The analog input channel is then incremented, and the input ränge is again tested in its entirety. This process is repeated until all analog input channels have been tested. During the couse of the test, if a channel fails to match the expected data word within +1 LSB, the test will respond with the message "Channel A failure data is BCDE should be FGHI", where channel A may ränge from 0-31 and BCDE and FGHI are actual and expected data words. "Do you want test repeated?" A response of "yes" will repeat the test for the same channel and data word. A response of "no" will increment the data word to the next chronological number. After all channels have been exercised, the test will respond with the message "End of test" and "Test number ?" The test fixture to jumper the analog input to the analog Output has been previousiy described. This test operates by checking the Status word or conversion complete. This is known as Polling Mode.

## Test 16 - Bipolar Continuity Test - Interrupt Mode

### Description

This test operates in the same manner as Test 15, except that the program does not check the Status word but is interrupt driven.

Note: To use Test 16, the interrupt enable input to the analog board raust be connected to the previous device in interrupt daisy chain.

## SECTION 6: TECHNICAL DESCRIPTION

### 6.1 Introduction

The following section contains a detailed description of the Operation and logical throughput of the AIO. The reader is directed to use the accompanying schematic at the end of the manual as a reference. The AIB, being a subset of the AIO, is not noticeably discriminated in the description. All references to analog input are applicable to both boards. The boards' specification is also included in this section.

### 6.2 Description

The AIO is programmed as I/O ports. IC20 and IC26 decode address bus lines AB3-AB7 to select the board itself. IC21 decodes address bus lines ABO, AB1, and AB2. Jumpers JP29 through JP40 determine the address of the board.

Conversion of an input channel is started by writing the channel number to the board (location 88H). When address lines AB2, AB1, and ABO are logic 0 and WR- is active, Pin l of IC22 will go high latching the input channel number into IC23. The same signal also triggers the first one-shot in ICH. This one-shot times out 20 microseconds to allow for settling of the input multiplexers, instrumentation amplifier, and sample-hold amplifier. At the end of this time, it turns the sample-hold amplifier to Hold by outputting a pulse from Pin 13, ICH, to Pin 8 of IC12. This same pulse also triggers the second one-shot in ICH at Pin 9. The Output of the second one-shot, Pin 5 of ICH, is connected to Pin 18 of SM3 which immediately Starts conversion in the A/D Converter. The Output of the first one-shot, Pin 13, of ICH, and Pin 22 of SM3 go through an "OR" gate of IC28. The Output of the "OR" gate connects to the data bus (DO) at Pin 13 of IC27 to provide Status information. DO is low during the conversion process. DO is high when conversion is complete and data is ready at the Output of the A/D Converter. Data is Output from the A/D Converter, SM3, on Pins 1-6 and 27-32. The Outputs are then connected through IC33 and IC34 to the PIO, IC32, Pins 7-15 and 27-30. When the AIO is read, address lines AB2 and AB1 are equal to logic 0. The eight least significant bits of data are Output when ABO is logic 0 and the four most significant bits are Output when ABO is logic 1. ABO is connected to the PIO from IC27, Pin 3, to IC32, Pin 6.

The analog input Signals are connected at connectors P2 and P3 through input protection resistors R27-R58 to the input CMOS multiplexers, IC3, 4, 5, and 6. The input multiplexers are shipped connected as 16 channel differential. The Instrumentation amplifier, which consists of amplifiers A1, A2, and A3, is connected in the differential mode. The resistance inserted at R8, in parallel with R9, determines the gain of the instrumentation amplifier.

Data is transferred to the Output D/A Converters, SM1 and SM2 by writing to the board. Address line, AB1, controls to which DAC data is written. With ABO a logic 0, the eight least significant bits are written to the board and stored in IC8 and IC16. With ABO a logic l, the four roost significant bits are written to the board and buffered by IC25.

When ABO is a logic l and WR- is active, data is written to the D/A Converter that is selected by AB1. When AB1 is a logic 0, data is written to IC9 and IC17 which störe data for SMl. When AB1 is a logic l, data is transferred to IC10 and IC18, which Stores data for SM2.

## 6.3 Specification

Typical at 25deg C and rated power supplies unless otherwise noted.

### ANALOG INPUT SECTION (AIO/AIB)

| | |
|---|---|
| **Input characteristics** | |
| Number of Channels | 32 single-ended/16 diff |
| ADC Gain Ranges (Jumper Selectable) | 0-5V, 0-10V, (+/-) 2.5V, (+/-) 5V, (+/-) 10V |
| Amplifier Gain Ranges (Resistor Prog.) | 1 to 1000 |
| Maximum Input Voltage Without Damage | +26 volts |
| Input Impedance | 100Mohm , 10 pF OFF Channel<br>100Mohm , 100 pF ON Channel |
| Bias Current | 20 nA |
| Differential Bias Current | 10 nA |
| **Transfer Characteristics** | |
| Resolution | 12 bits |
| Throughput Time (max.) G = 1 | 45 usec/channel |
| **Accuracy** | |
| System Accuracy at +25deg C (max.), Note 1 | +0.25% FSR, Note 2 |
| Linearity | +1/2 LSB |
| Differential Linearity | +1/2 LSB |
| Quantizing Error | +1/2 LSB |
| Monotonicity, Note 3 | Guaranteed 0deg C to +70deg C |
| **Stability Over Temperature, Note 4** | |
| System Accuracy Drift (max.) G=1 | (+/-) 30 ppm of FSR/deg C |
| **Dynamic Accuracy** | |
| Sample and Hold Aperature Time | 30 ns |
| Aperature Time Uncertainity | (+/-)5 ns |
| Differential Amplifier CMR | 74 dB (DC to 1kHz) |
| Channel Crosstalk | 80 dB down at 1kHz, for OFF channel to On channel |

### ANALOG OUTPUT SECTION (AIO)

| | |
|---|---|
| **Output Characteristics** | |
| Number of Channels | 2 |
| Output Voltage Ranges (Strap Selectable) | 0 to +5V, 0 to +10V<br>(+/-)2.5V, (+/1)5V,<br>(+/-)10V at 5mA Output Output |

| | |
|---|---|
| Impedance | l ohm |
| **Transfer Characteristics** | |
| Resolution | 12 bits |
| Output Settling Time (max.) | 10 usec |
| **Accuracy** | |
| Output Accuracy | (+/-)0.0125% FSR |
| Temperature Coeffient of Accuracy | +30 ppm of FSR/deg C |

## MECHANICAL

| | |
|---|---|
| **Environmental** | |
| Operating Temperature | Odeg C to +70deg C |
| Storage Temperature | -25deg C to +85deg C |
| Relative Humidity | 95% noncondensing |
| **Mechanical** | |
| Length | 7.7 in/19.6 cm |
| Depth | 7.5 in/19.1 cm |
| Thickness | .062 in/0.16 cm |
| Maximum Component Height | .4 in/1.02 cm |

## ELECTRICAL

Power Converter Requirements: +5V (+/-)5% at 1.6A

Available to User*

| DC Output | AIO | AIB | |
|---|---|---|---|
| +15V | Oma* | 50ma* | 70 deg C |
| | 15ma* | 65ma* | 25 deg C |
| -15V | Oma* | 50ma* | 70 deg C |
| | 15ma* | 65ma* | 25 deg C |

Connectors

| VENDOR | PART NO. | DESCRIPTIQN |
|---|---|---|
| Garry Mfg. Co. | **4000-2** | 122-pin edge (100 mil spacing) |
| Augat | 14005-19P1 | 122-pin edge (100 mil spacing) |
| Ansley | 609-2615M | Analog edge |
| Ansley | 171-26 | Cable |
| Ansley | 609-255 | Analog socket |

NOTES
1. Includes offset errors, gain errors, linearity errors at gain = 1.
2. FSR mean Full Scale Range.
3. No missing codes guaranteed.
4. Includes offset drift, gain drift, and linearity drift.

## SECTION 7: MAINTENANCE

### 7.1 Introduction

This section contains information on maintenance of the analog boards.

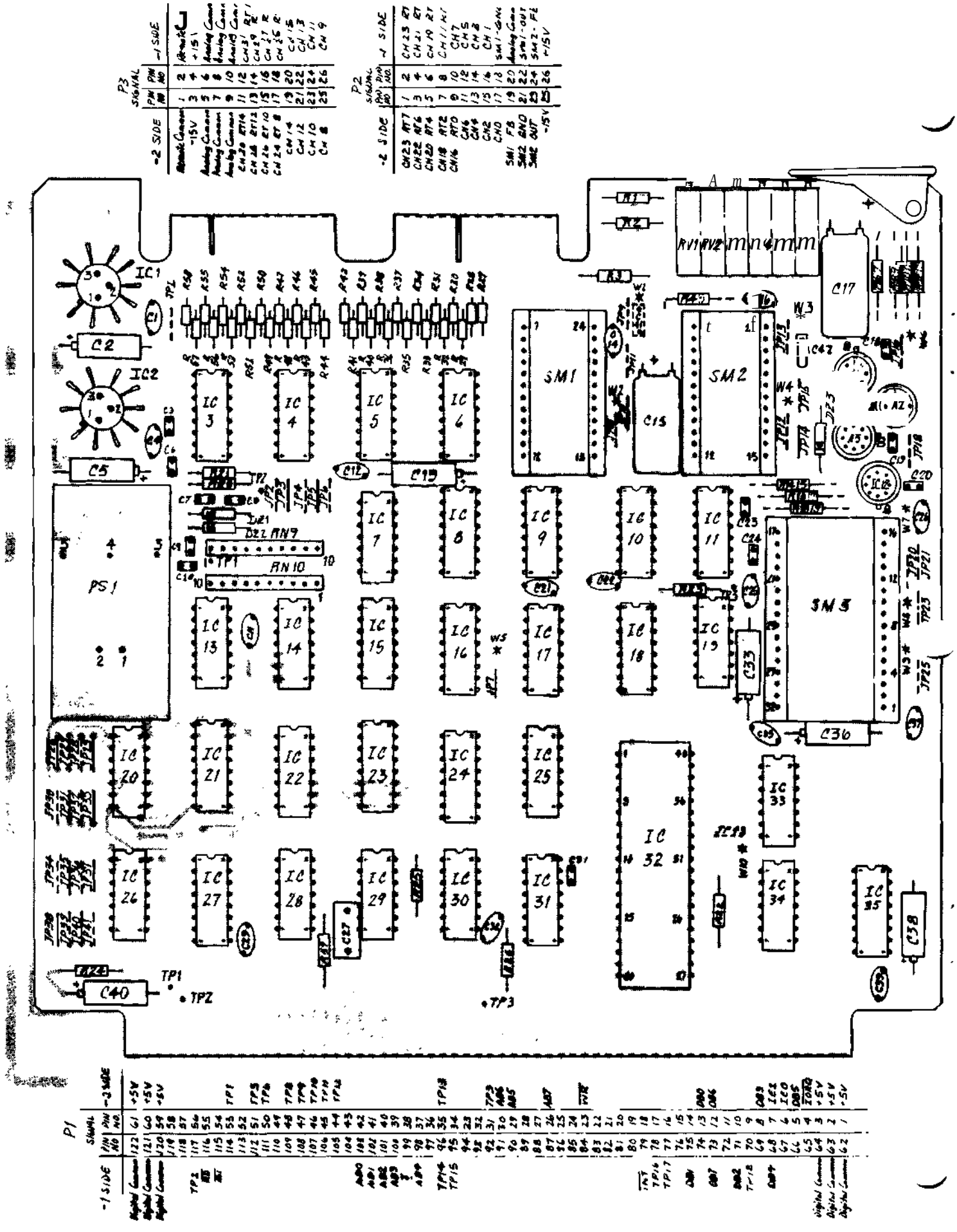
### 7.2 Drift

In any System, powered on Operation will cause the components to drift from their original values. This is particularly evident in analog Systems. The Eurr-Brown components, used on the AIO and AIB, use thin-film laser-trimmed resisters with a typical absolute temperature coefficient of 20-60 parts per million and a ratio temperature coefficient of 3-5 parts per million. Consequently, in one year, the typical drift could be 200-600 parts per million and the typical ratio drift could be 25-50 parts per million. This means that after 400 hours of Operation, the offset could have drifted 1LSB, and that after 43000 hours of Operation, the conversion may no longer be monotonic or linear. The offset and gain adjustments should be checked once every six months.

## SECTION 8: DRAWINGS

### 8.1 Introduction

This section contains the schematic pinout lists and the assembly drawing for the AIO and AIO.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SM3
IC1
IC2
PS1
C2
C5
C15
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C36
C40
TP1
TP2
TP3
RV1
RV2
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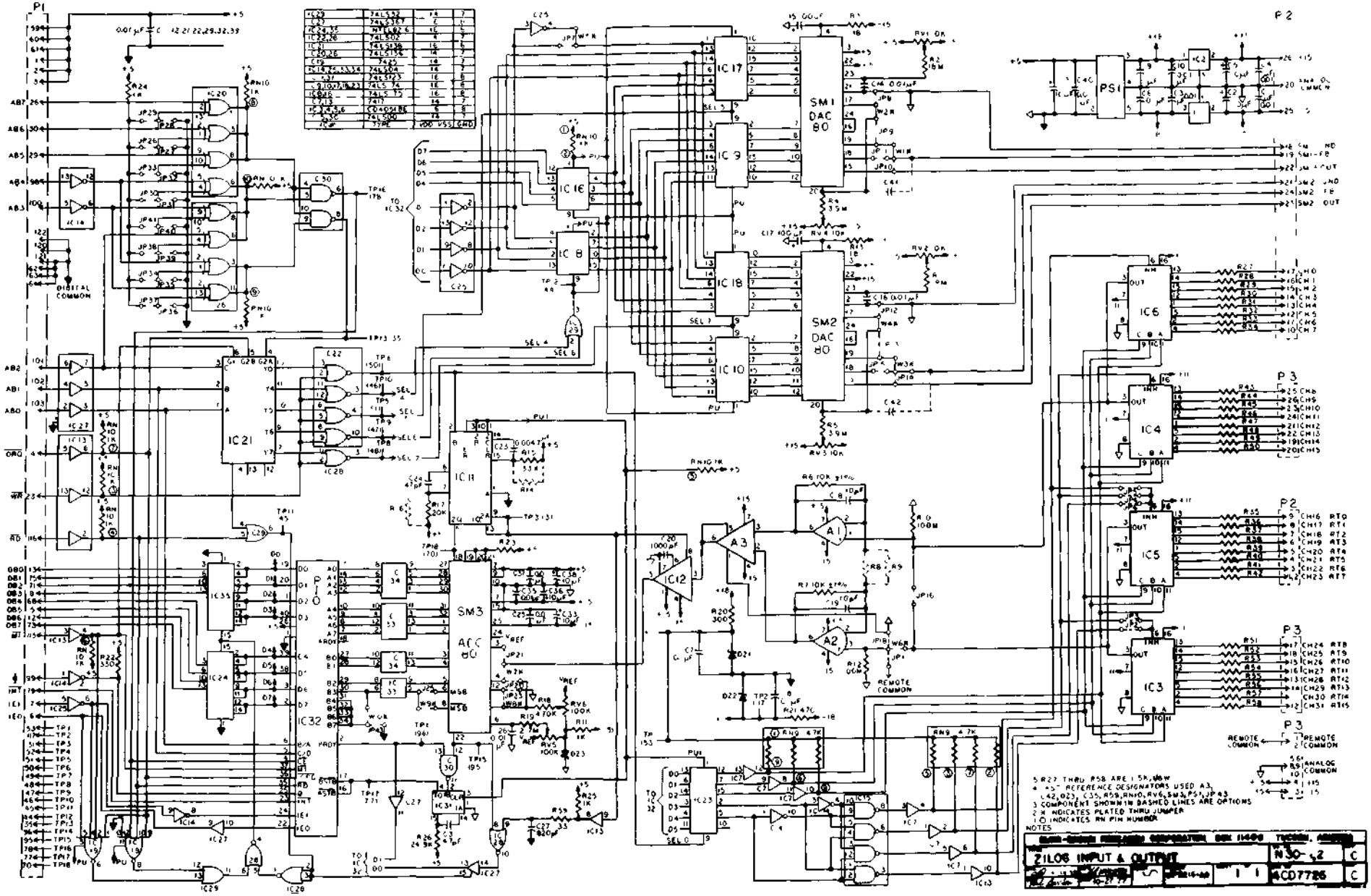
P1
P2
P3
IC 17
IC 9
IC 16
IC 8
IC 18
IC 10
SM1 DAC 80
SM2 DAC 80
IC 6
IC 4
IC 5
IC 3
IC 21
IC 32
IC 11
IC 12
SM3 ACC 80
A1
A2
A3
PS1
ZILOG INPUT & OUTPUT
4CD7726

AIO I/O CABLES P2 AND P3

| WIRE | AIO EDGE CONNECTOR | ANSLEY "D" CONNECTOR | P2 SIGNALS | P3 SIGNALS |
|---|---|---|---|---|
| 1 | 1 | — | CH23 (RT7) | REMOTE COMMON |
| 2 | 2 | 13 | CH23 (RT7) | REMOTE COMMON |
| 3 | 3 | 25 | CH22 (RT6) | -15V |
| 4 | 4 | 12 | CH21 (RT5) | +15V |
| 5 | 5 | 24 | CH20 (RT4) | ANALOG COMMON |
| 6 | 6 | 11 | CH19 (RT3) | ANALOG COMMON |
| 7 | 7 | 23 | CH18 (RT2) | ANALOG COMMON |
| 8 | 8 | 10 | CH17 (RT1) | ANALOG COMMON |
| 9 | 9 | 22 | CH16 (RT0) | ANALOG COMMON |
| 10 | 10 | 9 | CH7 | ANALOG COMMON |
| 11 | 11 | 21 | CH6 | CH30 (RT14) |
| 12 | 12 | 8 | CH5 | CH31 (RT15) |
| 13 | 13 | 20 | CH4 | CH28 (RT12) |
| 14 | 14 | 7 | CH3 | CH29 (RT13) |
| 15 | 15 | 19 | CH2 | CH26 (RT10) |
| 16 | 16 | 6 | CH1 | CH27 (RT11) |
| 17 | 17 | 18 | CH0 | CH24 (RT8) |
| 18 | 18 | 5 | SM1-GND | CH25 (RT9) |
| 19 | 19 | 17 | SM1-FB | CH14 |
| 20 | 20 | 4 | ANALOG COMMON | CH15 |
| 21 | 21 | 16 | SM2-GND | CH12 |
| 22 | 22 | 3 | SM1-OUT | CH13 |
| 23 | 23 | 15 | SM2-OUT | CH10 |
| 24 | 24 | 2 | SM2-FB | CH11 |
| 25 | 25 | 14 | -15V | CH8 |
| 26 | 26 | 1 | +15V | CH9 |

PINOUT FOR AIO BOARD

| PIN # | SIGNAL NAME |
|---|---|
| 001 | (+5V.PRINTED.DISTRIBUTION) |
| 002 | (+5V.PRINTED.DISTRIBUTION) |
| 003 | (+5V.PRINTED.DISTRIBUTION |
| 004 | IORO- |
| 005 | DB5 |
| 006 | IEO |
| 007 | IEI |
| 008 | DB3 |
| 009 | . |
| 010 | . |
| 011 | . |
| 012 | DB6 |
| 013 | DB0 |
| 014 | . |
| 015 | . |
| 016 | . |
| 017 | . |
| 018 | . |
| 019 | . |
| 020 | . |
| 021 | . |
| 022 | . |
| 023 | WR- |
| 024 | . |
| 025 | . |
| 026 | AB7 |
| 027 | . |
| 028 | . |
| 029 | AB5 |
| 030 | AB6 |
| 031 | TP3 |
| 032 | . |
| 033 | . |
| 034 | . |
| 035 | TP13 |
| 036 | . |
| 037 | . |
| 038 | . |
| 039 | . |
| 040 | . |
| 041 | . |
| 042 | . |
| 043 | . |
| 044 | TP12 |

```
045       TP11
046       TP10
047       TP9
048       TP8
049       TP7
050       TP6
051       TP5
052       TP4
053       TP1
054       .
055       .
056       .
057       .
058       .
059       (+5V.PRINTED.DISTRIBUTION)
060       (+5V.PRINTED.DISTRIBUTION)
061       (+5V.PRINTED.DISTRIBUTION)
062       (GND.PRINTED.DISTRIBUTION)
063       (GND.PRINTED.DISTRIBUTION)
064       (GND.PRINTED.DISTRIBUTION)
065       .
066       .
067       .
068       DB4
069       .
070       TP18
071       DB2
072       .
073       DB7
074       .
075       DB1
076       .
077       TP17
078       TP16
079       INT-
080       .
081       .
082       .
083       .
084       .
085       .
086       .
087       .
088       .
089       .
090       .
091       .
092       .
```

```
093       .
094       .
095       TP15
096       TP14
097       .
098       AB4
099       PHI-
100       AB3
101       AB2
102       AB1
103       AB0
104       .
105       .
106       .
107       .
108       .
109       .
110       .
111       .
112       .
113       .
114       .
115       M1-
116       RD-
117       TP2
118       .
119       .
120        (GND.PRINTED.DISTRIBUTION)
121        (GND.PRINTED.DISTRIBUTION)
122        (GND.PRINTED.DISTRIBUTION)
```

## SECTION 9: SUPPLEMENTARY INTRODUCTION

### 9.1 Introduction

The following section contains listings and references to additional sources of Information that may be of assistance in implementing the user's application, and aid in better understanding the Operation of the analog board in a microcomputer-based system.

### 9.2 List of Supplementary Information

Burr-Brown Application Note AN-79
Burr-Brown Product Specification ADC 80
Burr-Brown Product Specification DAC 80
Zilog PIO Product Specification
Zilog PIO Technical Manual
Zilog Interrupt Structure Application Note