Zilog

PMB HARDWARE MANUAL

03-3007-01 REV. A

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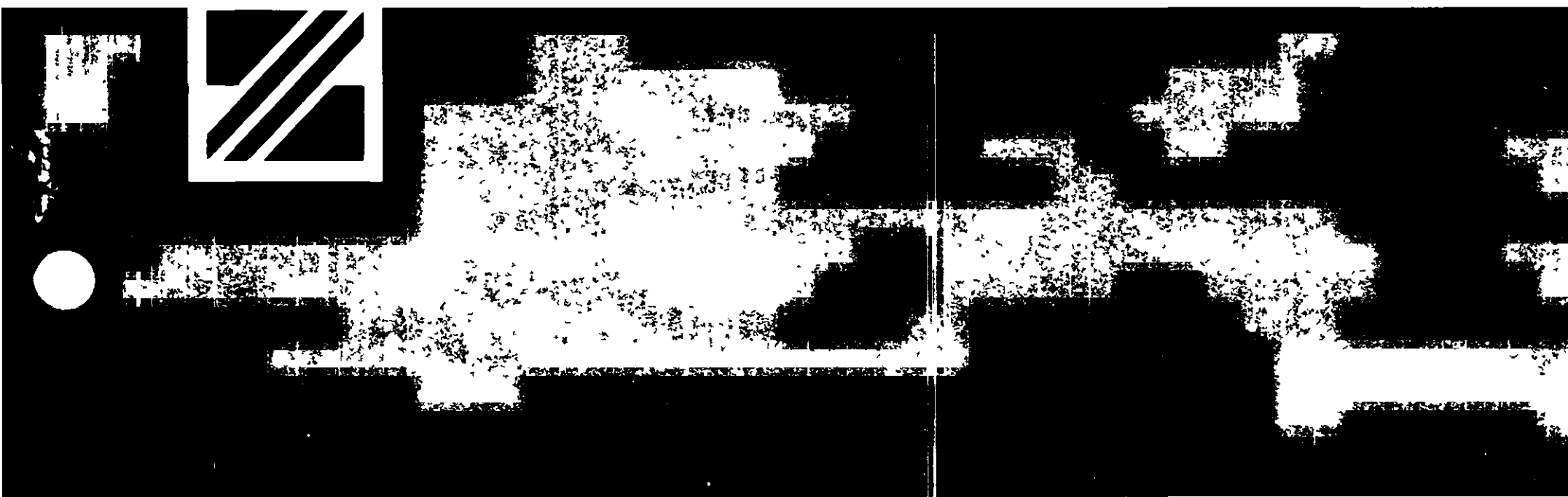

Price: $4.50

03-3007-01

Revision A

PMB USER'S GUIDE

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PMB USER'S MANUAL

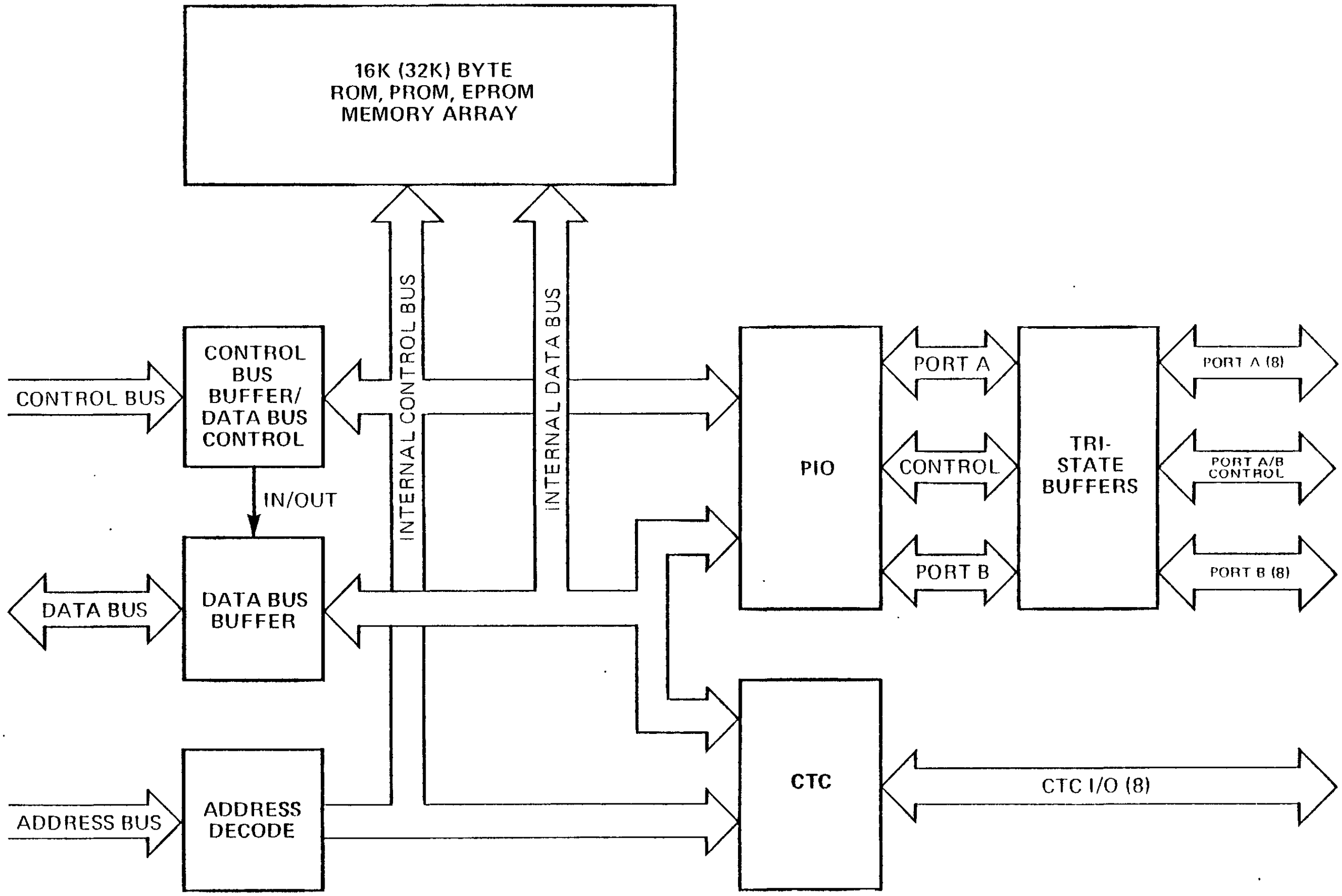
SECTION 1: GENERAL INFORMATION

1.1 Product Description

The Z80-PMB provides the Z80 Microcomputer Board Series with additional PROM or ROM memory and I/O capability.

The board contains sixteen, 24-pin sockets to accommodate up the 32K bytes of program memory using 2716 EPROMs or 2316 ROMs. The PMB will also accommodate 2708 EPROMs, or 6381 (82S181) PROMs for 16K bytes of program memory. Program memory addressing is implemented by using a PROM-based memory address decoder.

The PMB also contains a Z80-PIO and CTC providing 16 lines of parallel I/O with four control lines for byte operation, and four 8-bit counter/timers. The I/O devices are mapped anywhere into the I/O address space by strapping selections.



1.2 BLOCK DIAGRAM

SECTION 2. INSTALLATION

2.1 Introduction

The following section contains information on initial unpacking and inspection, power and signal connections to the MCB, and installation of the PMB in the MCZ-1 series systems.

2.2 Initial Unpacking and Inspection

Inspect the product for shipping damage as soon as it is unpacked. Check for any physical damage that may be attributed to abuse and handling during shipment. If the product is damaged in any way, notify the carrier immediately.

2.3 Installation (MCZ-1)

The PMB may be installed in either of the prewired memory board positions in the MCZ-1/20 or MCZ-1/25 systems. These positions are J6 and J7 as described in the MCZ-1 Hardware User's Manual. In the MCZ-1/30 System, J6 and J7 of each card cage, may be used in the identical manner as previously described. In the MCZ-1/05, -1/10 and PDS, J1 (User's Option) and J4 (Video Display Board) will directly accommodate the PMB.

2.4 Power and Signal Connections

The Z80-PMB is pin-compatible with the Z80 MCB bus structure. For convenience, the wire list for interconnection between the MCB and the PROM Memory Board is provided:

TO	FROM	DESCRIPTION
PMB:1-3, 59-61	MCB:1-3, 59-61	+5V P.S.
PMB:4	MCB:4	IORQ-
PMB:5	MCB:5	DATA BIT (5)
PMB:7	Last used IEO	IEI of PIO
PMB:8	MCB:8	DATA BIT (3)
PMB:12	MCB:12	DATA BIT (6)
PMB:13	MCB:13	DATA BIT (0)
PMB:26	MCB:26	ADDR. BIT (7)
PMB:27	MCB:27	ADDR. BIT (8)
PMB:29	MCB:29	ADDR. BIT (5)
PMB:30	MCB:30	ADDR. BIT (6)
PMB:32	MCB:32	ADDR. BIT (15)
PMB:36	MCB:36	ADDR. BIT (13)
PMB:37	MCB:37	ADDR. BIT (11)
Next IEI	PMB:50	IEO of PIO
Next IEI	PMB:58	IEO of CTC
PMB:62-64, 120-122	MCB:62-64, 120-122	COMMOM
PMB:66, 67	MCB:66, 67	-5V P.S.
PMB:68	MCB:68	DATA BIT (4)
PMB:69, 70	MCB:69, 70	+12V P.S.
PMB:71	MCB:71	DATA BIT (2)
PMB:73	MCB:73	DATA BIT (7)
PMB:75	MCB:75	DATA BIT (1)
PMB:79	MCB:79	INT-
PMB:85	MCB:85	MRQ-
PMB:89	MCB:89	ADDR. BIT (9)
PMB:91	MCB:91	ADDR. BIT (10)
PMB:94	MCB:94	ADDR. BIT (14)
PMB:97	MCB:97	ADDR. BIT (12)
PMB:98	MCB:98	ADDR. BIT (4)
PMB:99	MCB:99	PHI-
PMB:100	MCB:100	ADDR. BIT (3)
PMB:101	MCB:101	ADDR. BIT (2)
PMB:102	MCB:102	ADDR. BIT (1)
PMB:103	MCB:103	ADDR BIT (0)
PMB:115	MCB:115	M1-
PMB:116	MCB:116	RD-
PMB:117	MCB:83	ROM DISABLE-

TABLE 2.3.1: MCB TO PMB WIRE LIST

SECTION 3: OPERATION

3.1 Introduction

This section contains a general description of the PROM Memory Board's operation, and provides some application software for initializing and communicating to the PIO and CTC.

3.2 PROM Type Selection

Jumper area J3 is used to configure the PMB for a particular type of PROM. The following table shows the pin assignments which differ between the three PMB-compatible PROMs:

Pin	2708	2716	6381 (82S181)
18	PRGM	PD/PGM	CE4
19	VDD	A10	CE3
21	VBB	VPP	CE1-

For a 2708, the following jumpers are to be connected at J3:

J3-1 to J3-16 PRGM = GND
J3-2 to J3-15 Disable Bank A during Bank B access
J3-3 to J3-14 Disable Bank B for lower 1K of 2K page
J3-4 to J3-13 VDD = +12V
J3-7 to J3-10 VBB = -5V

For a 2716 and (2316), the following jumpers are to be connected at J3:

J3-1 to J3-16 PD/PGM = GND
J3-3 to J3-13 A10 = IAB10
J3-6 to J3-11 VPP = +5V

For a 6381, the following jumpers are to be connected at J3:

J3-2 to J3-15 Disable Bank A during Bank B access
J3-3 to J3-14 Disable Bank B for lower 1K of 2K page
J3-5 to J3-12 CE3 = +5V
J3-5 to J3-16 CE4 = +5V
J3-8 to J3-10 CE1- = GND

3.3 PROM Address Selection

PROM address selection is accomplished by programming particular bit maps into the decoder PROMs A10 and A11. Inputs to the decoder PROMs are IAB15-IAB11, which address the 32 PROM locations. Each of the 32 PROM locations represents a 2K byte segment of memory space. To place a PROM in a particular 2K segment, program the appropriate data byte at the address corresponding to the desired 2K segment. See Figure 3.3.1 for the data bytes associated with each PROM socket, and Figure 3.3.2 for the correspondence between 2K memory segments and control PROM locations. Unused locations in the address decoder PROMs, A10 and A11, should be programmed with 0FFH. The following two examples illustrate the address selection procedure:

Example 1 - Assume that two 2716's are to be used, one located at 0 to 7FFH, and the other at F800H to FFFFH. Also assume that the 2716's are placed in PROM sockets 0 (A24) and 15 (A22), respectively. Decoder PROM A10 should enable PROM socket 0 (A24) when the addresses 0 to 7FFH are being accessed. For this address range, Figure 3.3.2 shows that address 0 in the decoder PROM should be programmed. Figure 3.3.1 shows that the data byte corresponding to PROM socket 0 (A24) is 0FEH. Therefore, data byte 0FEH should be programmed into address 0 of A10. Decoder PROM A11 should enable PROM socket 15 (A22) when the addresses F800H to FFFFH are being accessed. Again, using Figures 3.3.1 and 3.3.2, data byte 07FH should be programmed into address 1FH of A11.

Example 2 - The above example is now repeated using 2708's. The PROM select logic is such that when using 1K PROMs, the least significant Kbyte of a 2K byte page resides in PROM Bank A. The most significant Kbyte resides in the corresponding socket in PROM Bank B. Shown below is the correspondence between PROM sockets and memory segments. For this example:

PROM SOCKET	MEMORY SEGMENT
0 (A24)	0 to 3FFH
8 (A15)	400H to 7FFH
7 (A31)	F800H to F3FFH
15 (A22)	FC00H to FFFFH

Using Figures 3.3.1 and 3.3.2, it can be seen that data bytes FEH and 7FH should be programmed into locations 0 and 1FH, respectively, in both A10 and A11.

PROM SOCKET	DATA BYTE TO BE PROGRAMMED INTO A10 OR A11
0 (A24) , 8 (A15)	0FEH
1 (A25) , 9 (A16)	0FDH
2 (A26) , 10 (A17)	0FBH
3 (A27) , 11 (A18)	0F7H
4 (A28) , 12 (A19)	0EFH
5 (A29) , 13 (A20)	0DFH
6 (A30) , 14 (A21)	0BFH
7 (A31) , 15 (A22)	07FH

FIGURE 3.3.1: PROM ENABLE PROGRAMMING

MEMORY SEGMENT	LOCATION TO BE PROGRAMMED IN A10 OR A11
0000-07FFH	0H
0800-0FFFH	1H
1000-17FFH	2H
1800-1FFFH	3H
2000-27FFH	4H
2800-2FFFH	5H
3000-37FFH	6H
3800-3FFFH	7H
4000-47FFH	8H
4800-4FFFH	9H
5000-57FFH	0AH
5800-5FFFH	0BH
6000-67FFH	0CH
6800-6FFFH	0DH
7000-77FFH	0EH
7800-7FFFH	0FH
8000-87FFH	10H
8800-8FFFH	11H
9000-97FFH	12H
9800-9FFFH	13H
A000-A7FFH	14H
A800-AFFFH	15H
B000-B7FFH	16H
B800-BFFFH	17H
C000-C7FFH	18H
C800-CFFFH	19H
D000-D7FFH	1AH
D800-DFFFH	1BH
E000-E7FFH	1CH
E800-EFFFH	1DH
F000-F7FFH	1EH
F800-FFFFH	1FH

FIGURE 3.3.2: PROM ENABLE ADDRESS MAPPING

3.4 I/O Address Modification

Jumper areas J1 and J2 are used to assign I/O port addresses to the CTC and PIO. These two devices have the following ports which are addressed in the order indicated:

PIO DATA PORT A	0
PIO DATA PORT B	1
PIO CONTROL PORT A	2
PIO CONTROL PORT B	3
CTC CHANNEL 0	0
CTC CHANNEL 1	1
CTC CHANNEL 2	2
CTC CHANNEL 3	3

Jumper area J2 selects into which range of 32 I/O ports the above eight ports will be located. See Figure 3.4.1 for the possible jumper selections for J2. Once the port range has been established, jumper area J1 is used to position the two groups of four ports at specific locations within the range. See Figure 3.4.2 for the possible jumper selections for J1.

For example, assume that the four PIO ports are to be 6CH, 6DH, 6EH, and 6FH, and that the four CTC ports are to be 74H, 75H, 76H, and 77H. All of these ports are in the range of 60-7FH. Figure 3.4.1 shows that the following jumpers at J2 are to be connected:

J2- 9 to J2-7
J2-10 to J2-4
J2-11 to J2-2

Within this range, the four PIO ports are located from 0CH to 0FH. Figure 3.4.2 shows that jumper J1-13 to J1-5 should be connected. The four CTC ports are located from 14H to 17H within the range 60-70H. Therefore, a jumper is connected from J1-14 to J1-7.

J2-9 TO	J2-10 TO	J2-11 TO	I/O PORT RANGE
J2-7	J2-5	J2-3	0-1FH
J2-7	J2-5	J2-2	20-3FH
J2-7	J2-4	J2-3	40-5FH
J2-7	J2-4	J2-2	60-7FH
J2-6	J2-5	J2-3	80-9FH
J2-6	J2-5	J2-2	A0-BFH
J2-6	J2-4	J2-3	C0-DFH
J2-6	J2-4	J2-2	E0-FFH

FIGURE 3.4.1: I/O PORT ADDRESS RANGE

JUMPER CONNECTION TO J13(PIO) OR J14(CTC)	FOUR PORTS WITHIN 32-PORT RANGE
J1-2	0H to 3H
J1-3	4H to 7H
J1-4	8H to 0BH
J1-5	0CH to 0FH
J1-6	10H to 13H
J1-7	14H to 17H
J1-8	18H to 1BH
J1-9	1CH to 1FH

FIGURE 3.4.2: PORT GROUP ADDRESS ASSIGNMENT

3.5 PIO Input/Output Configuration

Each of the PIO ports A and B may be configured for input or output.

When Port A is used as an input port, jumpers are to be connected at K1 as shown in Table 3.5.1. The bus drivers A5, A6, and A7 should either be disabled or removed. (Note that A6 and A7 are also used for Port B.) The termination resistors may also be installed, depending on the application. In the output mode, the jumpers at K1 are removed, and the bus drivers are enabled.

When Port B is used as an input port, jumpers are to be connected at K2, as shown in Table 3.5.2. As with Port A, the appropriate bus drivers must be disabled or removed. The termination resistor network, A12, may also be installed. In the output mode, the jumpers at K2 are removed, and the bus drivers are enabled.

Connection		Signal
K1-5	to K1-6	A0
K1-10	K1-9	A1
K1-11	K1-7	A2
K1-12	K1-8	A3
K1-13	K1-1	A4
K1-14	K1-2	A5
K1-15	K1-3	A6
K1-16	K1-4	A7

TABLE 3.5.1 PIO PORT A JUMPER

Connection		Signal
K2-1	to K2-16	B0
K2-2	K2-15	B1
K2-3	K2-14	B2
K2-4	K2-13	B3
K2-5	K2-12	B4
K2-6	K2-11	B5
K2-7	K2-10	B6
K2-8	K2-9	B7

TABLE 3.5.2 PIO PORT B JUMPER

SECTION 4: PROGRAMMING AND INITIALIZATION

4.1 Introduction

The following section contains information and programming examples for on-board PIO and CTC operation.

4.2 Reset (PIO)

The Z80-PIO automatically enters a reset state when power is applied. The reset state performs the following functions:

- o Both port mask registers are reset to inhibit all port data bits.
- o Port data bus lines are set to a high impedance state and the Ready 'handshake' signals are inactive (low). Mode 1 is automatically selected.
- o The vector address registers are not reset.
- o Both port interrupt enable flip flops are reset.
- o Both port output registers are reset.

In addition to the automatic power-on reset, the PIO can be reset by applying an M1- signal without the presence of a RD- or IORQ- signal. If no RD- or IORQ- is detected during M1-, the PIO- will enter the reset state immediately after the M1- signal goes inactive. The purpose of this reset is to allow a single external gate to generate a reset without a power down sequence. This approach was required due to the 40-pin packaging limitation.

Once the PIO has entered the internal reset state, it is held there until the PIO receives a control word from the CPU.

4.3 Loading the Interrupt Vector (PIO)

The PIO has been designed to operate with the Z80-CPU using the mode 2 interrupt response. This mode requires that an interrupt vector be supplied by the interrupting device. This vector is used by the CPU to form the address for the interrupt service routine of that port. This vector is placed on the Z-80 data bus during an interrupt acknowledge

cycle by the highest priority device requesting service at that time. (Refer to the Z80-CPU Technical Manual for details on how an interrupt is serviced by the CPU.) The desired interrupt vector is loaded into the PIO by writing a control word to the desired port of the PIO with the following format:

D7	D6	D5	D4	**D3**	**D2**	D1	D0
V7	V6	V5	V4	**V3**	**V2**	V1	0*

* Signifies this control word is an interrupt vector

D0 is used in this case as a flag bit which, when low, causes V7 through V1 to be loaded into the vector register. At interrupt acknowledge time, the vector of the interrupting port will appear on the Z-80 data bus exactly as shown in the format above.

4.4 Selecting an Operating Mode (PIO)

Port A of the PIO may be operated in any of four distinct modes: Mode 0 (output mode), Mode 1 (input mode), Mode 2 (bidirectional mode), and Mode 3 (control mode). Note that the mode numbers have been selected for mnemonic significance; i.e., 0=Out, 1=In, 2=Bidirectional. Port B can operate in any of these modes except Mode 2.

The mode of operation must be established by writing a control word to the PIO in the following format:

D7	D6	D5	D4	**D3**	**D2**	**D1**	D0
M1	M0	X	X	**1**	**1**	**1**	**1**
mode word		not used		signifies mode word to be set			

Bits D7 and D6 form the binary code for the desired mode according to the following table:

D7	D6	Mode
0	0	0 (output)
0	1	1 (input)
1	0	2 (bidirectional)
1	1	3 (control)

Bits D5 and D4 are ignored. Bits D3-D0 must be set to 1111 to indicate "Set Mode".

Selecting Mode 0 enables any data written to the port output register by the CPU to be enabled onto the port data bus. The contents of the output register may be changed at any time by the CPU simply by writing a new data word to the port. Also, the current contents of the output register may be read back to the Z80-CPU at any time through the execution of an input instruction.

With Mode 0 active, a data write from the CPU causes the Ready handshake line of that port to go high to notify the peripheral that data is available. This signal remains high until a strobe is received from the peripheral. The rising edge of the strobe generates an interrupt (if it has been enabled) and causes the Ready line to go inactive. This very simple handshake is similar to that used in many peripheral devices.

Selecting Mode 1 puts the port into the input mode. To start handshake operation, the CPU merely performs an input read operation from the port. This activates the Ready line to the peripheral to signify that data should be loaded into the empty input register. The peripheral device then strobes data into the port input register using the strobe line. Again, the rising edge of the strobe causes an interrupt request (if it has been enabled) and deactivates the Ready signal. Data may be strobed into the input register regardless of the state of the Ready signal if care is taken to prevent a data overrun condition.

Mode 2 is a bidirectional data transfer mode which uses all four handshake lines. Therefore, only Port A may be used for Mode 2 operation. Mode 2 operation uses the Port A handshake signals for output control and the Port B handshake signals for input control. Thus, both A RDY and B RDY may be active simultaneously. The only operational difference between Mode

0 and the output portion of Mode 2 is that data from the Port A output register is allowed on to the port data bus only when A STB- is active in order to achieve a birdirectional capabilty.

Mode 3 operation is intended for status and control applications and does not utilize the handshake signals. When Mode 3 is selected, the next control word sent to the PIO must define which of the port data bus lines are to be inputs and which are outputs. The format of the control word is shown below:

D7	D6	D5	**D4**	**D3**	D2	D1	D0
I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

If any bit is set to a one, then the corresponding data bus line will be used as an input. Conversely, if the bit is reset, the line will be used an an output.

During Mode 3 operation, the strobe signal is ignored and the Ready line is held low. Data may be written to a port or read from a port by the Z80-CPU at any time during Mode 3 operation. When reading a port, the data returned to the CPU will be composed of input data from port data bus lines assigned as inputs plus port output register data from those lines assigned as outputs.

4.5 Setting the Interrupt Control Word (PIO)

The interrupt control word for each port has the following format:

D7	D6	D5	D4	D3	D2	D1	D0
Enable Interrupt	AND/ OR	High/ Low	Masks follows	0	1	1	1
	used in Mode 3 only			signifies interrupt control word			

If bit D7=1, the interrupt enable flip flop of the port is set and the port may generate an interrupt. If bit D7=0, the enable flag is reset and interrupts may not be generated. If an interrupt is pending when the enable flag is set, it will then be enabled onto the CPU interrupt request line. Bits D6, D5, and D4 are used only with Mode 3 operation. However, setting bit D4 of the interrupt control word during any mode of operation will cause any pending interrupt to be reset. These three bits are used to allow for interrupt operation in Mode 3 when any group of the I/O lines go to certain defined states. Bit D6 (AND/OR) defines the logical operation to be performed in port monitoring. If bit D6=1, an AND function is specified, and if D6=0, an OR function is specified. For example, if the AND function is specified, all bits must go to a specified state before an interrupt will be generated, while the OR function will generate an interrupt if any specified bit goes to the active state.

Bit D5 defines the active polarity of the port data bus line to be monitored. If bit D5=1, the port data lines are monitored for a high state while if D5=0, they will be monitored for a low state.

If bit D4=1, the next control word sent to the PIO must define a mask as follows:

D7	D6	D5	D4	D3	D2	D1	D0
MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

Only those port lines whose mask bit is zero will be monitored for generating an interrupt.

4.6 CTC Programming

Before a Z80-CTC channel can begin counting or timing operations, a Channel Control Word and a Time Constant data word must be written to it by the CPU. These words will be stored in the Channel Control Register and the Time Constant Register of that channel. In addition, if any of the four channels have been programmed with bit 7 of their Channel Control Words to enable interrupts, an Interrupt Vector must be written to the appropriate register in the CTC. Due to automatic features in the Interrupt Control Logic, one pre-programmed Interrupt Vector suffices for all four channels.

4.7 Loading the Channel Control Register (CTC)

To load a Channel Control Word, the CPU performs a normal I/O Write sequence to the port address corresponding to the desired CTC channel. Two CTC input pins, namely CS0 and CS1, are used to form a 2-bit binary address to select one of four channels within the device. In many system architectures, these two input pins are connected to Address Bus lines A0 and A1, respectively, so that the four channels in a CTC device will occupy contiguous I/O port addresses. A word written to a CTC channel will be interpreted as a Channel Control Word, and loaded into the Channel Control Register, its bit 0 is a logic 1. The other seven bits of this word select operating modes and conditions as indicated in Figure 4.9.1.

D7	D6	D5	D4	D3	D2	D1	D0
INTERRUPT ENABLE	MODE	RANGE	SLOPE	TRIGGER	LOAD TIME CONSTANT	RESET	1

NOTE: RANGE and TRIGGER used in Timer Mode only

Bit 7=1

The channel is enabled to generate an interrupt request sequence every time the Down Counter reaches a zero-count condition. To set this bit to 1 in any of the four Channel Control Registers necessitates that an Interrupt Vector also be written to the CTC before operation begins. Channel interrupts may be programmed in either Counter Mode or Timer Mode. If an updated Channel Control Word is written to a channel already in operation, with bit 7 set, the interrupt enable selection will not be retroactive to a preceding zero-count condition.

Bit 7=0

Channel interrupts disabled.

Bit 6=1

Counter Mode selected. The Down Counter is decremented by each triggering edge of the External Clock (CLK/TRG) input. The Prescaler is not used.

Bit 6=0

Timer Mode selected. The Prescaler is clocked by the System Clock Φ, and the output of the Prescaler, in turn, clocks the Down Counter. The output of the Down Counter (the channel's ZC/TC output) is a uniform pulse train of periods given by the product

t *P*TC

where t is the period of System Clock Φ, P is the Prescaler factor of 16 or 256, and TC is the time constant data word.

Bit 5=1

(Defined for Timer Mode only.) Prescaler factor is 256.

Bit 5=0

(Defined for Timer Mode only.) Prescaler factor is 16.

Bit 4=1

TIMER MODE - positive edge trigger starts timer operation.
COUNTER MODE - positive edge decrements the down counter.

Bit 4=0

TIMER MODE - negative edge trigger starts timer operation.
COUNTER MODE - negative edge decrements the down counter.

Bit 3=1

Timer Mode only - External trigger is valid for starting timer operation after rising edge of T2 of the machine cycle following the one that loads the time constant. The Prescaler is decremented 2 clock cycles later if the setup time is met, otherwise, 3 clock cycles.

Bit 3=0

Timer Mode only - Timer begins operation on the rising edge of T2 of the machine cycle following the one that loads the time constant.

Bit 2=1

The time constant data word for the Time Constant Register will be the next word written to this channel. If an updated Channel Control Word and time constant data word are written to a channel while it is already in operation, the Down Counter will continue dcrementing to zero before the new time constant is loaded into it.

Bit 2=0

No time constant data word for the Time Constant Register should be expected to follow. To program bit 2 to this state implies that this Channel Control Word is intended to update the status of a channel already in operation, since a channel will not operate without a correctly programmed data word in the Time Constant Register, and a set bit 2 in this Channel Control Word provides the only way of writing to the Time Constant Register.

Bit 1=1

Reset channel. Channel stops counting or timing. This is not a stored condition. Upon writing into this bit, a reset pulse discontinues current channel operation, however, none of the bits in the channel control register are changed. If both bit 2=1 and bit 1=1, the channel will resume operation upon loading a time constant.

Bit 1=0

Channel continues current operation.

4.8 Loading the Time Constant Register (CTC)

A channel may not begin operation in either Timer Mode or Counter Mode unless a time constant data word is written into the Time Constant Register by the CPU. This data word will be expected on the next I/O Write to this channel following the I/O Write of the Channel Control Word, provided that bit 2 of the Channel Control Word is set. The time constant data word may be any integer value in the range 1-256. If all eight bits in this word are zero, it is interpreted as 256. If a time constant data word is loaded to a channel already in operation, the Down Counter will continue decrementing to zero before the new time constant is loaded from the Time Constant Register to the Down Counter.

TIME CONSTANT REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
MSB							LSB

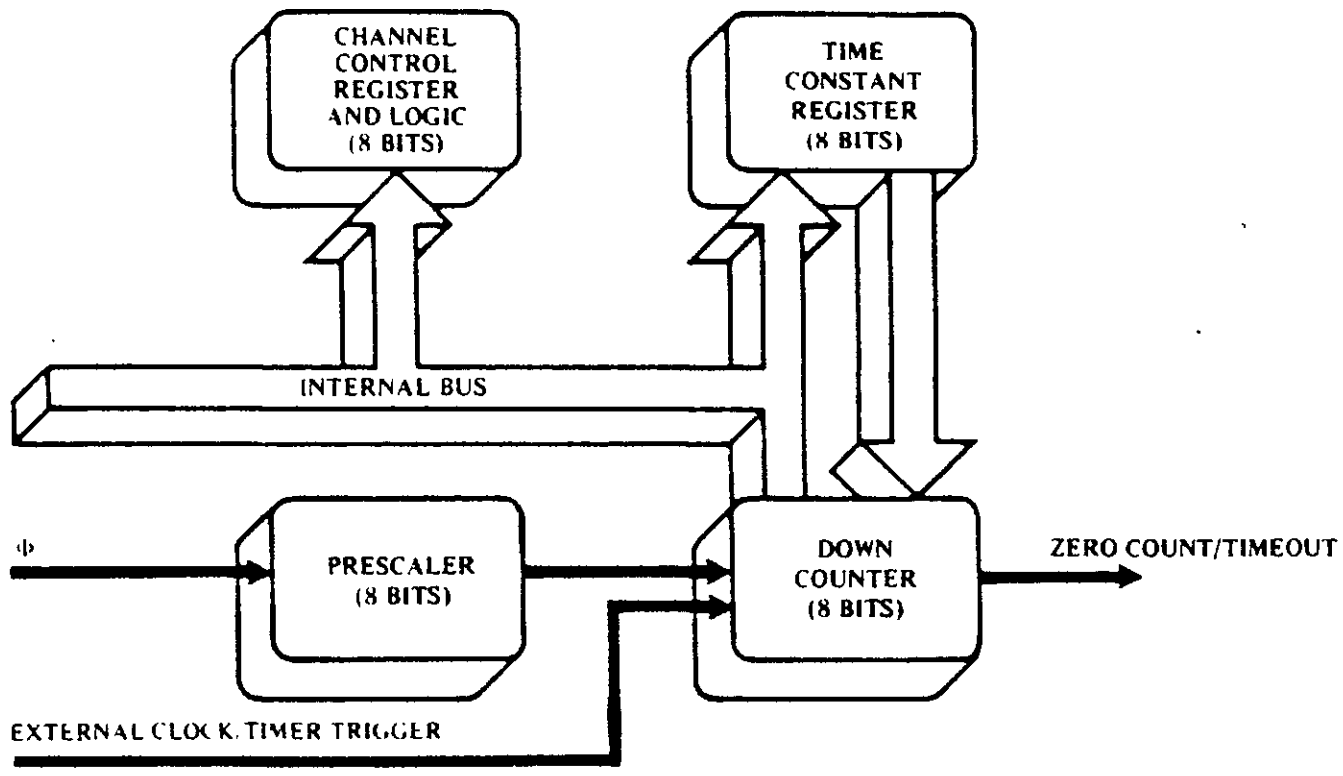


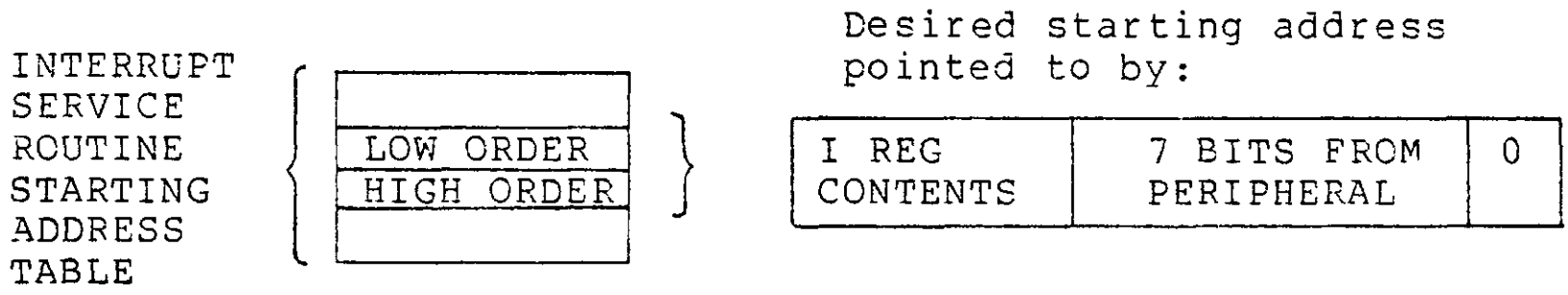
FIGURE 2.0-2
CHANNEL BLOCK DIAGRAM

Figure 4.9.1: Channel Block Diagram

4.9 Loading the Interrupt Vector Register (CTC)

The Z80-CTC has been designed to operate with the Z80-CPU programmed for Mode 2 interrupt response. Under the requirements of this mode, when a CTC channel requests an interrupt and is acknowledged, a 16-bit pointer must be formed to obtain a corresponding interrupt service routine starting address from a table in memory. The upper 8 bits of this pointer are provided by the CPU's I register, and the lower 8 bits of the pointer are provided by the CTC in the form of an Interrupt Vector unique to the particular channel that requested the interrupt.

MODE 2 INTERRUPT OPERATION



The high order 5 bits of this Interrupt Vector must be written to the CTC in advance as part of the initial programming sequence. To do so, the CPU must write to the I/O port address corresponding to the CTC channel 0, just as it would if a Channel Control Word were being written to that channel, except that bit 0 of the word being written must contain an 0. (As explained above in Section 4.7, if bit 0 of a word written to a channel were set to 1, the word would be interpreted as a Channel Control Word, so a 0 in bit 0 signals the CTC to load the incoming word into the Interrupt Vector Register.) Bits 1 and 2, however, are not used when loading this vector. At the time when the interrupting channel must place the interrupt Vector on the Z80 Data Bus, the Interrupt Control Logic of the CTC automatically supplies a binary code in bits 1 and 2 identifying which of the four CTC channels is to be serviced.

INTERRUPT VECTOR REGISTER

Interrupt Vector Register

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	X	X	0

SUPPLIED BY USER

D2	D1	
0	0	CHANNEL 0 (Highest Priority)
0	1	CHANNEL 1
1	0	CHANNEL 2
1	1	CHANNEL 3 (Lowest Priority)

Automaticallly inserted by
Z80-CTC

SECTION 5: STANDARD FACTORY STRAPPING CONFIGURATION

5.1 Introduction

The following sections show how the PIO and CTC port address component carriers are strapped as provided by Zilog. All other required component carriers are provided but are left unstrapped.

5.2 Component Carrier J1

Component carrier J1 (Part No. 33-0173-17) for PIO and CTC port selects: (This part should be supplied with the board)

J1-13	TO	J1-2	PIO = 0, 1, 2, 3
J1-14		J1-2	CTC=4, 5, 6, 7

5.3 Component Carrier J2

Component carrier J2 (Part No. 33-0173-18) for I/O port range select: (This part should be supplied with the board) (PIO ports begin at A0H)

J2-9	TO	J2-6
J2-10		J2-5
J2-11		J2-2

5.4 Component Carrier J3

Component carrier J3 to select 2708 PROMS:

J3-1	TO	J3-16
J3-2		J3-15
J3-3		J3-14
J3-4		J3-13
J3-7		J3-10

5.5 Component Carrier K1

Component carrier K1 to configure PIO port A I/O lines.

K1-1	TO	K1-13
K1-2		K1-14
K1-3		K1-15
K1-4		K1-16
K1-5		K1-6
K1-7		K1-11
K1-8		K1-12
K1-9		K1-10

5.6 Component Carrier K2

Component Carrier K2 to configure PIO port I/O lines:

K2-1	TO	K2-16
K2-2		K2-15
K2-3		K2-14
K2-4		K2-13
K2-5		K2-12
K2-6		K2-11
K2-7		K2-10
K2-8		K2-9

SECTION 6. TECHNICAL DESCRIPTION

6.1 Introduction

The following section contains a detailed description of the operation and logical throughput of the PMB. The reader is directed to use the accompanying schematic at the end of the manual as a reference. The board's specification is also included in this section.

6.2 Detailed Description of Board Schematics

Sheet 1

Sheet 1 consists of the bi-directional data bus buffers, through which data bytes pass between the system data bus and the PMB internal data bus. The direction of the buffers is determined by control PROM A1 whose bit map is shown in Figure 6.2.1. Some address and control lines buffers are also included on this sheet.

```
000 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
010 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
020 FF FF FF FF FE FE FF FF FF FF FF FF FE FE FF FF
030 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
040 FE FE FE FE FE FE FE FE FF FF FF FF FF FF FF FF
050 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
060 FF FF FF FF FE FE FF FF FF FF FF FF FE FE FF FF
070 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
080 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
090 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
0A0 FF FF FF FF FE FE FF FF FF FF FF FF FE FE FF FF
0B0 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
0C0 FE FE FE FE FE FE FE FE FF FF FF FF FF FF FF FF
0D0 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
0E0 FF FF FF FF FE FE FF FF FF FF FF FF FE FE FF FF
0F0 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
100 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
110 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
120 FE FE FF FF FF FF FF FF FE FE FF FF FF FF FF FF
130 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
140 FE FE FE FE FE FE FE FE FF FF FF FF FF FF FF FF
150 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
160 FE FE FF FF FF FF FF FF FE FE FF FF FF FF FF FF
170 FF FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF
180 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
190 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
1A0 FE FE FF FF FF FF FF FF FE FE FF FF FF FF FF FF
1B0 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
1C0 FE FE FE FE FE FE FE FE FF FF FF FF FF FF FF FF
1D0 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
1E0 FE FE FF FF FF FF FF FF FE FE FF FF FF FF FF FF
1F0 FE FF FF FF FE FF FF FF FE FF FF FF FE FF FF FF
```

Figure 6.2.1. BIT MAP FOR DATA BUS CONTROL PROM

Sheet 2

The I/O port select logic for the CTC and PIO is shown on Sheet 2. Jumper area J2 selects one out of eight possible I/O groups, with each group consisting of 32 I/O port addresses. Jumper area J1 is used to located the CTC and PIO ports within the group selected by J2. The two least significant address bits determine which one of the four I/O ports is being addressed in either the PIO or CTC.

Sheet 3

Sheet 3 contains the Z80-PIO and Z80-CTC. They both communicate with the Z80-CPU via the PMB internal data and control busses. The clock/trigger inputs and zero count/time out outputs of the CTC are brought to the PMB card edge connector. The I/O lines of the PIO are connected to a jumper/buffer area shown on Sheets 4 and 5. Interrupts are daisy-chained such that PIO interrupts have priority over those of the CTC.

Sheet 4

I/O options for PIO channel A are shown on Sheet 4. When port A is in the input mode, jumpers are connected at K1, output buffers are disabled and termination resistors are connected. In the output mode, the jumpers at K1 are removed and the output buffers are enabled. Depending upon the application, several different types of I/O buffers may be used.

Sheet 5

I/O options for PIO channel B are shown on Sheet 5. When port B is in the input mode, jumpers are connected at K2, output buffers are disabled, and termination resistors are connected. In the output mode, the jumpers at K1 are removed and the output buffers are enabled.

Sheet 6

Sheet 6 contains the first bank of eight PROMs and an address decoder PROM. IAB15-IAB11 are input to the decoder PROM and select the location of each of the PROMs on 2K boundaries. Output SEL A indicates to the data bus buffer direction control (Sheet 1) that one of the PROMs in this bank has been selected. Sheet 6 also contains the logic to generate the PMB interrupt enable out.

Sheet 7

Sheet 7 contains the second bank of eight PROMs and an address decoder PROM. Output SEL B indicates to the data bus buffer direction control (Sheet 1) that one of the PROMs in this bank has been selected. Sheet 7 also contains buffers for the four most significant address bits.

Sheet 8

Sheet 8 contains the logic for PROM bank selection, and the jumper area for selecting a particular type of PROM. For PROMs requiring +5V and -12V, backplane connections must be made to the MCZ power supply or other external supplies. See Jumper Table 1 (Sheet 8) for a description of the required jumpers for each type of PROM.

REVISIONS

LTR	DESCRIPTION	TE	APPROVED
L	[illegible]	18	D Hammond

HT = 6,7

DB Ø
DB 1
DB 2
DB 3
DB 4
DB 5
DB 6
DB 7

IDB Ø
IDB 1
IDB 2
IDB 3
IDB 4
IDB 5
IDB 6
IDB 7

A33 (1/6)

+5V

SHT 3 SEL Ø
SHT 3 SEL 1
SHT 3,6 IEI Ø
SHT 3,6 IEO 1
SHT 6 SEL A
SHT 7 SEL B

A1 6306

A33 (1/367)

115 M1
116 RD

A36 (1/367)

4 IORQ
29 AB5
30 AB6
26 AB7
27 AB8
89 AB9

IM1 SHT 3
IIORQ SHT 2,3
IRD SHT 3,8
IAB5
IAB6
IAB7 } SHT 2,6,7
IAB8 SHT 6,7
IAB9 SHT 6,7

91 AB10
31 AB11

IAB10 SHT 8
IAB11 SHT 6,7

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 DECIMALS .X ± .010 .XX DEC ± .02	SIGNATURE AND DATE DRWN Rodney Fox 6/77 CHK AA Ca 1/5/78 APVD / / 19
APPLICATION		MATL	FINISH

ZILOG INC
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM
Z 80 PROM MEMORY BOARD

SIZE	DRAWING NO	ISSUE
C	02 0011 01	B

CAGE NONE SHEET 1 OF 3

REVISIONS
LTR | DESCRIPTION | APPROVED

SHT 2 IØ
SHT 2 SEL Ø
SHT 1 IM1
SHT 1 IIORQ
SHT 1 IRD
SHT 2 IABØ
SHT 2 IAB1
SHT 1 IDBØ
IDB1
IDB2
IDB3
IDB4
IDB5
IDB6
IDB7
SHT 1 IEIØ
SHT 1 IEIØ
7
SHT 2 SEL1

A32 Z80 PIO Ø
M1
IORQ
RD
A/B
C/D
DØ
D1
D2
D3
D4
D5
D6
D7
IEO
IEI
ARDY
ASTRB
BRDY
INT

SHT 4
+5V
A13 74125
R16 220
R14 220
R17 330
R15 330
A13 74125
SHT 5
SHT 6
IEOØ
INT → 79

A32 Z80 CTC
Ø
CE
+5V
CLK/TØ → 110
ZC/TOØ → 114
CLK/T1 → 111
ZC/TO1 → 119
CLK/T2 → 112
ZC/TO2 → 118
CLK/T3 → 113
INT → 111
IEO → 58
IEI
SHT 6 IEI1

NOTES:
⚠ THESE COMPONENTS ARE INSTALLED BY CUSTOMER.

NEXT ASSY	USED ON	APPLICATION	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1 FRACTIONS ± 1/64 2 PLACE DEC ± .010 3 PLACE DEC ± .005		MATL	FINISH
SIGNATURE AND DATE: DRWN	DATE		
DSGD CHK			
APVD			

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE: LOGIC DIAGRAM Z80 FROM MEMORY BD

SIZE C | DRAWING NO 12 0 411 01 | ISSUE 13

CAE NOTE | SHT 3 OF 8

REVISIONS
DESCRIPTION | APPROVED

IAB2
IAB3
IAB4
IAB0
IAB1 — SHT 3,6,7

103 > AB0
102 > AB1
101 > AB2
100 > AB3
A33 74LS367
98 > AB4
A34 74LS367

A10 LS138
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
E1 E2 E3
J1
13 → SEL 0 → SHT 1
14 → SEL 1 → SHT 1

J2
IAB5 — A23 74LS04
IAB6 — A23 74LS04
IAB7 — A23 74LS04
SHT1
A14 74LS00
SHT1 IIORQ

A23

99 > Φ — A23 74LS04 — IΦ → SHT 3

1 >
2 >
3 >
59 >
60 >
61 >
+5V
C3 22UF
C1 22UF
C5 C29 1μF
CR1 IN4001
67 >
68 >
69 >
120 >
121 >
122 >

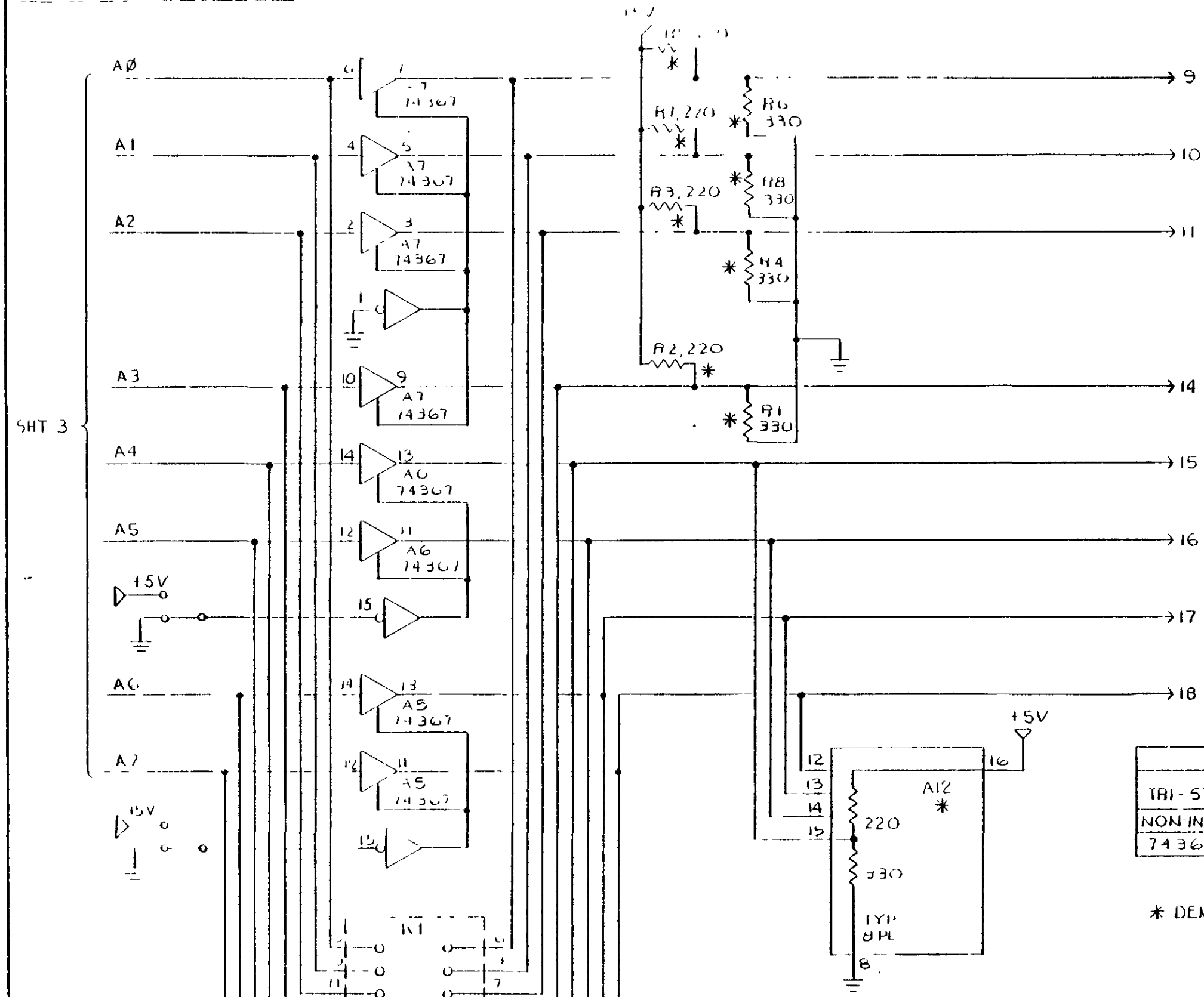
NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± FRACTIONS ± 1/64 DECIMALS .XX ± .010 .XXX ± .005	SIGNATURE AND DATE DRAWN DRFTG CHK APVD
ALTERATION		PART	FINISH

ZILOG INC
1060 BOBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM
Z 80 PROM MEMORY BD

SIZE C | DRAWING NO 02 0011 01 | ISSUE 14
SCALE NONE | SHEET 2 OF 9

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



DRIVER CONFIGURATION			
TRI-STATE DRIVERS		BUFFERS/DRIVERS WITH OPEN COLLECTOR HIGH VOLT OUTPUT	
NON-INVERT	INVERT	NON-INVERT	INVERT
74367	74368	7406	7407

* DENOTES CUSTOMER INSTALLED

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE DRWN Wendy Fox 4/77 DRFTG CHK APVD	ZILOG INC. 10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
APPLICATION		MATL	FINISH	TITLE LOGIC DIAGRAM Z 80 PROM MEMORY BD
				SIZE C DRAWING NO P/ 0041 01 ISSUE B
				SCALE NONE SHEET 4 OF 8

REVISIONS
LTR | DESCRIPTION | E | APPROVED

B0
B1
B2
B3
B4
B5
B6
B7

SHT 3

4 5 A6 74367
2 3 A6 74367
10 9 A6 74367
1
6 1 A6 74367
10 9 A5 74367
6 7 A5 74367
1
4 5 A5 74367
3 A5 74367

→ 24
→ 25
→ 28
→ 31
→ 33
→ 34
→ 38
→ 39

K2

10 +5V 330 220 A1 * TYP 8 PL
11
9
4
1
2
1

* DENOTES CUSTOMER INSTALLED.

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 TWO PLACE DEC ± .010 THREE DEC ± .XXX	SIGNATURE AND DATE DRWN Randy Fox 4/77 DES'D CHK MM 4/18 APVD L Green 4/26
APPLICATION		MATL	FINISH

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE: LOGIC DIAGRAM Z 80 PROM MEMORY BD

SIZE C | DRAWING NO 02 0041-01 | ISSUE B

SCALE NONE | SHEET 5 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

+5V

14

IABØ 9
IAB1 7
IAB2 6
IAB3 5
IAB4 4
IAB5 3
IAB6 2
IAB7 1
IAB8 23
IAB9 22

SHT 2
SHT 1

ROM 18 18
ROM 21 21
ROM 19 19

SHT 8

A24 ROM SOCKET Ø

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9

O0 O1 O2 O3 O4 O5 O6 O7

9 IDBØ
10 IDB1
11 IDB2
13 IDB3
14 IDB4
15 IDB5
16 IDB6
17 IDB7

SHT 1

CE 20

12

A25 ROM SKT 1 — 20
A26 ROM SKT 2 — 20
A27 ROM SKT 3 — 20
A28 ROM SKT 4 — 20
A29 ROM SKT 5 — 20
A30 ROM SKT 6 — 20
A31 ROM SKT 7 — 20

A10 7603 32×8

IAB15 14 A4
IAB14 13 A3
IAB13 12 A2
IAB12 11 A1
IAB11 10 AØ

SHT 7
SHT 1

B0 1
B1 2
B2 3
B3 4
B4 5
B5 6
B6 7
B7 9

CS 15

SHT 3 CONT A

A3 RES PACK 1K

6 5 4 3 7 8 2

RN3 1K +5V

RN8 1K +5V

11 12 13 14 10 6 7 15

1 2 3 4 5

A2 LS133 9 SEL A SHT 1

SHT 1 IEI Ø
IEO Ø
SHT 3
IEI 1
IEO 1
SHT 1

A9 /4LS11 3 4 5 6

A9 /4LS11 11 9 10 8

IEO/4B 50

NOTES:
ALL ROM SOCKETS WIRED
TYPICAL TO SOCKET Ø (A--)

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 3 PLACE DEC ± .010 2 PLC DEC ± .02	SIGNATURE AND DATE DRAWN DRFTG CHK APVD	ZILOG INC. 10460 BUBB ROAD CUPERTINO CALIFORNIA 95014
APPLICATION		MATL	FINISH	TITLE LOGIC DIAGRAM Z 80 PROM MEMORY BD
				SIZE C DRAWING NO 02 00-11 01 ISSUE B
				SCALE NONE SHEET 6 OF 8

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

+5V
14

IAB0 3
IAB1 7
IAB2 6
IAB3 5
IAB4 4
IAB5 3
IAB6 2
IAB7 1
IAB8 23
IAB9 22

SHT 2
SHT 1

ROM 18 18
ROM 21 21
ROM 19 19

SHT 8

A15 ROM SKT 8

$\overline{E4}$
$\overline{E1}$
E3
$\overline{E2}$
20
12

IDB0 9
IDB1 10
IDB2 11
IDB3 13
IDB4 14
IDB5 15
IDB6 16
IDB7 17

SHT 1

NOTE.
ALL ROM SOCKETS WIRED TYPICAL TO SOCKET 8.

A16 ROM SKT 9
A17 ROM SKT 10
A18 ROM SKT 11
A19 ROM SKT 12
A20 ROM SKT 13
A21 ROM SKT 14
A22 ROM SKT 15
20

A11 7603
$\overline{B0}$ 1
$\overline{B1}$ 2
$\overline{B2}$ 3
$\overline{B3}$ 4
$\overline{B4}$ 5
B5 6
$\overline{B6}$ 7
$\overline{B7}$ 9
A4 14
A5 13
A6 12
A7 11
A8 10
CS 15

IAB15
IAB14
IAB13
IAB12
IAB11

SHT 6

SHT 8 CONT B

A3 RES - PACK 1K
14 15 12 11 10 15 1 9

A4 LS133 9 SEL B SHT 1
3 4 5 6 7 2 1 10 11 12 13 14 15

R19 1K
+5V

A5 74LS367
A4 74LS367
A3 74LS367

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1° FRACTIONS ± 1/64 1 PLACE DEC ± 010 2 PLC DEC ± 02	SIGNATURE AND DATE DRAWN Randy Fox 4/77 CHK APVD
APPLICATION		MATL	FINISH

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

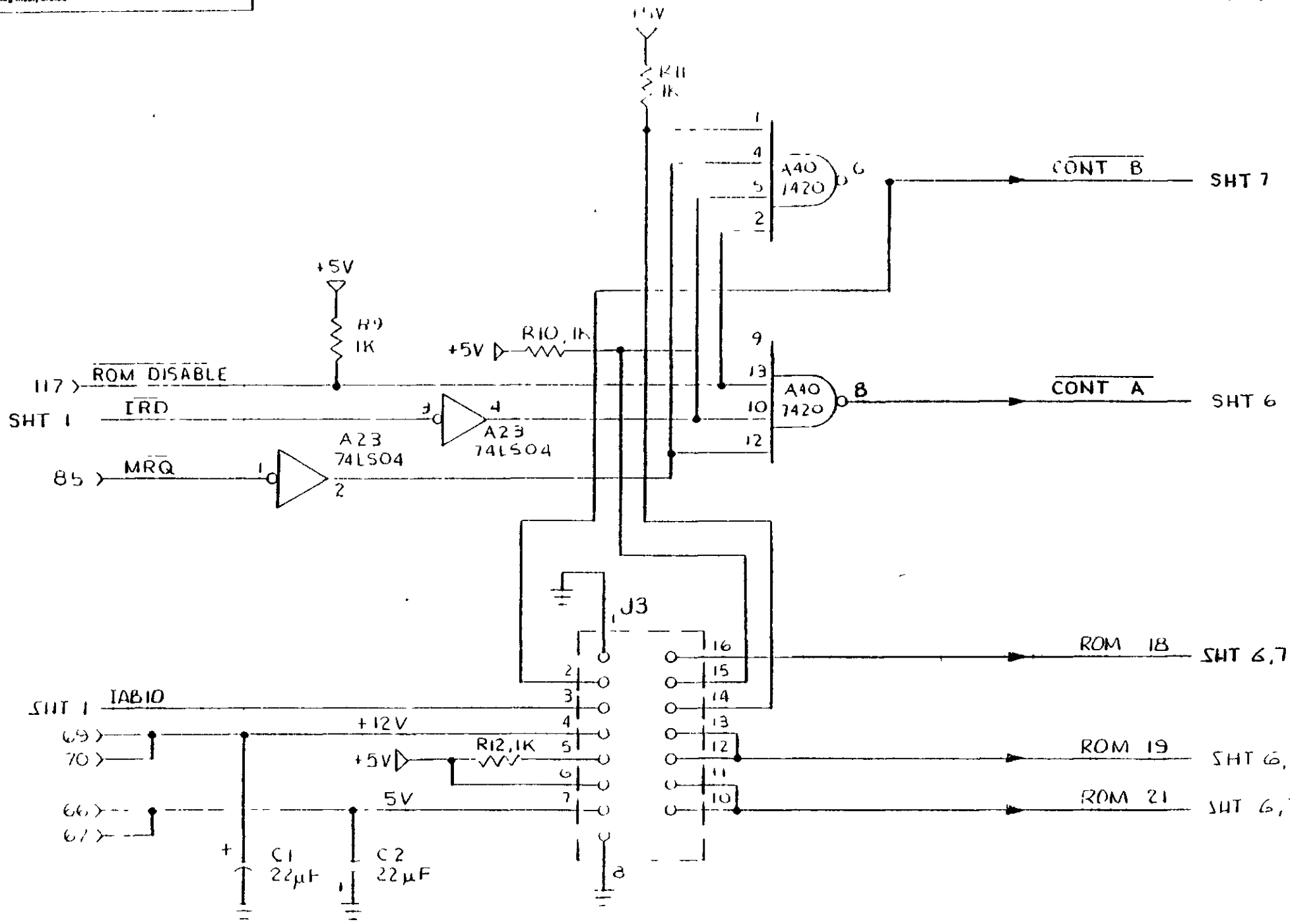
TITLE LOGIC DIAGRAM Z 80 PROM MEMORY BD

SIZE C | DRAWING NO 02 0041 01 | ISSUE B

SCALE NONE | SHEET 7 OF 8

REVISIONS

LTR	DESCRIPTION		APPROVED



JUMPER TABLE 1

ROM	J3	TYPES
2716	1 TO 16 3 TO 13 6 TO 11	2048x8 EPROM TRI-STATE
2708	4 TO 15 7 TO 10 1 TO 16 5 TO 14 2 TO 15	1024x8 EPROM TRI-STATE
6381	4 TO 15 7 TO 12 8 TO 10 6 TO 11 5 TO 14	1K x 8 PROM TRI-STATE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLC DEC ± .02

SIGNATURE AND DATE
DRWN
DES'G CHK
APVD

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM
Z 80 PROM MEMORY BD

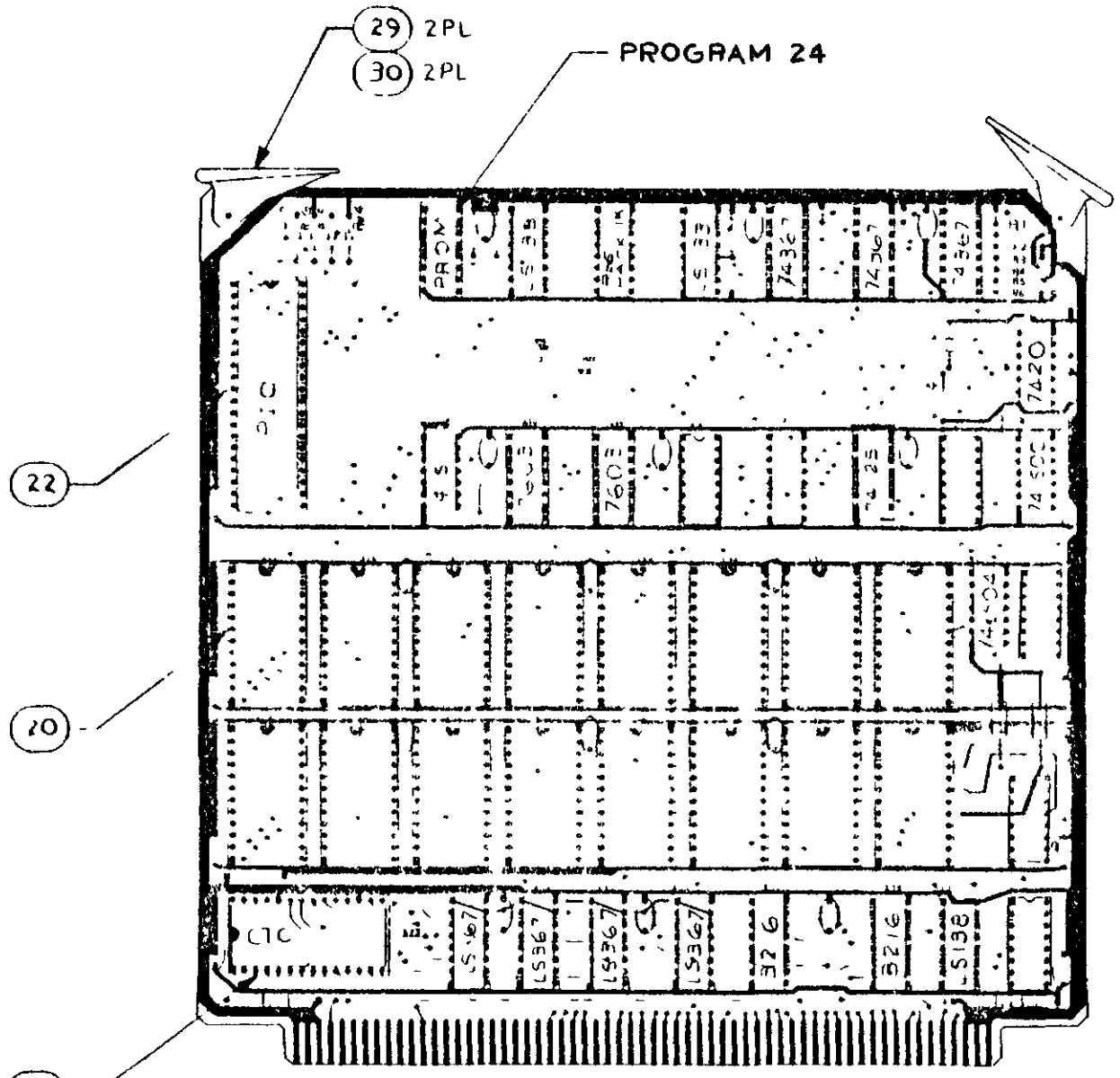
SIZE C | DRAWING NO 02 0011 01 | ISSUE B

SCALE NONE | SHEET 8 OF 8

NEXT ASSY | USED ON | APPLICATION | MATL | FINISH

CONFIDENTIAL

B	ECN 00184 (RELEASE)	3/78	P.N.
D1	ECN 00276 (CREATE -00)	5 23 78	A



NOTES

1 ASSEMBLE PER ZILOG MANUFACTURING SPECS

2 RUBBER STAMP SERIAL NO AND LATEST REV LETTER

3 REFER TO PARTS LIST FOR COMPLETE IDENTIFICATION OF REFERENCE DESIGNATIONS

4 ALL UNDESIGNATED CAPS ARE 0.1UF

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ANGLES ± 1 FRACTIONS ± 1/64 2 PLACE DEC ± 01 3 PLC DEC ± 002	SIGNATURE AND DATE DRWN P MILES 12 27 77 CHKD 1/78 APVD D Brown 1/1/78
APPLICATION		MATL	FINISH

ZILOG INC.
[illegible] CUPERTINO CALIFORNIA 95014

TITLE PRINTED WIRING ASS'Y, Z 80 PMB

SIZE C | DRAWING NO 09-0041-00/61 | REV B

SCALE 1:1 | SHEET 1 OF 1

6.5 PMB Specification

MEMORY SIZE:
Sixteen 24-pin sockets for up to 32 KBYTES of PROM/EPROM

MEMORY TYPE:
2708, 2716, 6381

INTERFACE:
TTL interface, with MCZ series data, address, and control signals.

ADDRESS SELECTION:
PROM programmable for unique addressing of each PROM socket.

PARALLEL I/O:
16 programmable bidirectional I/O lines.

COUNTER/TIMER:
4 programmable counter/timer channels.

ELECTRICAL SPECIFICATIONS:
DC POWER

	WITHOUT MEMORY	WITH 2708		WITH 2716		WITH 6381	
		TYP	MAX	TYP	MAX	TYP	MAX
+5V	0.60A	0.70A	0.84A	1.59A	2.28A	2.84A	3.40A
-5V	---	0.48A	0.96A	---	---	---	---
+12V	---	0.80A	1.28A	---	---	---	---

CONNECTOR:

122-pin edge (100 mil spacing) available from:

VENDOR	PART NO.
GARRY MFG. CO.	4000-2
AUGAT	14005-19P1

PHYSICAL CHARACTERISTICS:

LENGTH: 7.7 in/19.6cm
DEPTH: 7.5 in/19.1cm
THICKNESS: .062 in/0.16 cm
SPACING BETWEEN CARDS: 0.5 in/1.27cm centers
MAX COMPONENT HEIGHT: 0.4 in/1.02cm
ETCH LAYERS: TWO

ENVIRONMENT:

0 to 50 degrees centigrade

BURN IN REQUIREMENTS:

Prior to final test, the PMB shall burn in for 96 hours at 45 degrees C, and VCC at 5.3V +/- 2%. (5.2V to 5.4V) If any component is replaced after burn in, either component or the entire board must undergo an additional 48 hours at temperature and voltage.

6.6 PMB Parts List

1	PCB,BLANK,REV.B	10-0041-01	1	
2	I.C.,PROM	33-0053-24	1	A1
3	I.C.,74LS133	33-0170-01	2	A2,4
4	I.C.,74367	33-0008-01	3	A5,6,7
5	I.C.,PIO	33-0057-01	1	A8
6	I.C.,74LS11	33-0061-01	1	A9
7	I.C.,7603	33-0164-00	2	A10,11
8	I.C.,74125	33-0035-01	1	A13
9	I.C.,74LS00	33-0058-01	1	A14
10	I.C.,74LS04	33-0059-01	1	A23
11	I.C.,CTC	33-0078-01	1	A32
12	I.C.,74LS367	33-0055-01	4	A33,34,35,36
13	I.C.,3216	33-0089-01	2	A37,38
14	I.C.,74LS138	33-0068-01	1	A39
15	I.C.,7420	33-0026-01	1	A40
16	RES.NET.1K	47-0000-01	1	A3
17	RES.NET,220/330	47-0000-02	0	A12 (NOT SUPPLIED)
18	SOCKET,I.C.,14-PIN	21-1000-06	1	A13
19	SOCKET,I.C.,16-PIN	21-1000-02	12	A1,5,6,7,10,11,12, J1,J2,J3,K1,K2
20	SOCKET,I.C.,24-PIN	21-1000-03	16	A15-22,A24-31
21	SOCKET,I.C.,28-PIN	21-1000-04	1	A32
22	SOCKET,I.C.,40-PIN	21-1000-01	1	A8
23	RES,1/4W,5%,1K	47-1000-63	7	R9,10,11,12,13,18,19
24	RES,1/4W,5%,220	47-1000-47	0	R2,3,5,7,14,16 (NOT SUPPLIED)
25	RES,1/4W,5%,330	47-1000-51	0	R1,2,6,8,15,17 (NOT SUPPLIED)
26	CAP,22UF,15V	15-0003-25	4	C1,2,3,4
27	CAP,0.1UF,50V	15-0000-50	25	C5-C29
28	DIODE,1N4001	48-1000-01	1	CR1
29	EJECTOR,BLANK	24-0001-01	2	
30	PIN,EJECTOR	91-3000-01	2	
31	COMPONENT CARRIER	33-0173-17	1	J1:PIO&CTC PORT SELECT
32	COMPONENT CARRIER	33-0173-18	1	J2:I/O PORT RANGE SELECT

6.7 Pinout for PROM Memory Board

PIN #	SIGNAL NAME
001	+5V
002	+5V
003	+5V
004	IORQ-
005	DB5
006	.
007	IEI.PMB.PIO
008	DB3
009	PIO.0.A0
010	PIO.0.A1
011	PIO.0.A2
012	DB6
013	DB0
014	PIO.0.A3
015	PIO.0.A4
016	PIO.0.A5
017	PIO.0.A6
018	PIO.0.A7
019	PIO.0.A.RDY
020	PIO.0.A.STRB-
021	PIO.0.B.RDY
022	PIO.0.B.STRB-
023	.
024	PIO.0.B0
025	PIO.0.B1
026	AB7
027	AB8
028	PIO.0.B2
029	AB5
030	AB6
031	PIO.0.B3
032	AB15
033	PIO.0.B4
034	PIO.0.B5
035	.
036	AB13
037	AB11
038	PIO.0.B6
039	PIO.0.B7
040	.
041	.
042	.

PIN #	SIGNAL NAME
043	.
044	.
045	.
046	.
047	.
048	.
049	.
050	IEO.PMB.PIO
051	.
052	.
053	.
054	.
055	.
056	.
057	.
058	IEO.PMB.CTC
059	+5V
060	+5V
061	+5V
062	GND
063	GND
064	GND
065	.
066	-5V
067	-5V
068	DB4
069	+12V
070	+12V
071	DB2
072	.
073	DB7
074	.
075	DB1
076	.
077	.
078	.
079	INT-
080	.
081	.
082	.
083	.
084	.
085	MRQ-
086	.
087	.
088	.
089	AB9
090	.

PIN #	SIGNAL NAME
091	AB10
092	.
093	.
094	AB14
095	.
096	.
097	AB12
098	AB4
099	PHI-.(SYSTEM CLOCK-)
100	AB3
101	AB2
102	AB1
103	AB0
104	.
105	.
106	.
107	.
108	.
109	.
110	CK/T0
111	CK/T1
112	CK/T2
113	CK/T3
114	ZC/TO0
115	M1-
116	RD-
117	ROM.DISABLE-.(IN)
118	ZC/TO2
119	ZC/TC1
120	GND
121	GND
122	GND

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