Zilog

ZDS 1/25 HARDWARE USER MANUAL

PRELIMINARY

Zilog

03-3003-02, Revision 1

31 October 1978

ZDS 1/25 HARDWARE USER MANUAL

PRELIMINARY

TABLE OF CONTENTS

APPENDICES

1.0 INTRODUCTION

1.1 General Information

This manual describes the installation and hardware operation of the ZDS-1/25 Development Systems. It is divided into sections to enable the user to quickly locate information pertinent to the product's installation, operation and use. The sections and their contents are shown below.

SECTION I - INTRODUCTION	Describes the organization of the manual, related documents and functional description.
SECTION II - INSTALLATION	Describes the hardware installation and checkout of the system.
SECTION III - MAJOR UNITS	Describes the functional purpose and operation of the varous sub asssemblies in the unit.
SECTION IV - PRINCIPLES OF OPERATION	Describes the detailed operation of the unit as a system.

1.2 Related Documents

The following list of documents will provide detailed information to supplement this manual.

- RIO Operating System-User's Manual
- RIO Text Editor-User's Manual
- RIO Assembler and Linker-User's Manual
- ZDS-1/25, ZDS-1/40 PROM User's Manual
- Z80-CIB Hardware User's Manual
- Z80-ZDSP Hardware User's Manual
- Z80-PPB Hardware User's Manual
- Z80-PPB/16 Hardware User's Manual

1.3 General Description

The ZDS-1/25 Development System is a microcomputer system designed to support all hardware and softwre development activities for the Z80-CPU. The system includes a single cabinet which contains dual single-density hard-sectored floppy disk units, emulation interface, real-time storage module, breakpoint module, memory module, console interface module, monitor module, DC power supplies, internal cabling and single card slot for option expansion.

Specific features of the ZDS-1/25 Development System include:

- Z80-CPU with 4k bytes dedicated static RAM/ROM.
- RS-232 or current loop interface supporting transmission rates from 50-9600 baud.
- 60k bytes of dynamic RAM.
- Programmable hardware breakpoint module.
- Programable real-time event storage module.
- In-circuit emulation interface to user's prototype system.
- Memory mapping in blocks of 256 bytes.
- Dual single-density hard-sectored floppy disk drives and controller.
- Full operating system software:

  -ROM-based debug software

  -Relocatable Macro Assenbler and Linker

  -Text Editor

  -Disc File Management System
- Optional interfaces:

  -Auxiliary Serial/Parallel Input/Output Board

  -Printer Interface/Prom Programmer Interface

  -EPROM/Bipolar PROM Programmers

  -Parallel Interface Board

- Optional Peripherals

  -1920 character CRT terminal with upper/lower case keyboard

  -120 character/second Matrix Printer, bidirectional with forms length selector.

- Optional Software:

  -Basic Interpreter, including both binary and BCD math.

  -FORTRAN IV based on ANSI 1966 standard.

  -PLZ programming lanquages (Complier, Interpreter and high level assembler)

1.4 OPERATING MODES

Because the Z80-CPU is shared by both the system and the user's prototype during emulation, two distinct modes of operation are provided for the user. These modes of operation are clearly indicated by the MONITOR and USER switch/indicators on the front of the system.

MONITOR MODE:

This is the nórmal operating mode of the system when not using the emulation logic. In this mode all system resources are allocated to the development system and the emulation logic is disabled. While running in this mode the breakpoint module is disabled, and loading of the breakpoint module and the real-time storage parameters is enabled. The user memory in the prototype system may be accessed by the development system in part or as a whole depending on the memory mapper configuration.

USER MODE:

This mode is used when running in-circuit emulation and may be established in one to two fashions: (1) by pressing the USER button, or (2) by executing a Go command from the Debug environment. In this mode the Z80-CPU is dedicated to the emulation logic and is used to execute user's program in a real time mode. In order to accomplish this, certain system functions and emulation functions must occur. These functions are listed below:

- Breakpoint logic is enabled to compare address, data and control busses for equivalence.
- Breakpoint parameters may not be loaded.
- Real Time Storage Module is allowed to trace bus events.
- Real Time Storage Module parameter loading is disabled.
- Enable data strobe for Real Time Storage Modules.
- Enables Z80-CPU to see interrupt, non-maskable interrupt, wait, bus request and reset inputs from the user's system.
- Allows user's system to utilize blocks of or the entire development system memory, save F000H-FFFFH.
- Write protects the 1K static RAM scratch pad.

2.0 INSTALLATION

2.1 Unpacking

Each ZDS-1/25 Development System is shipped in a padded shipping container for protection. Upon receiving the system, place container in upright position, open container, remove top section of packing material, and visually inspect the unit for damage.

WARNING

The approximate weight of the unit is 65 lbs; exercise caution when removing unit from shipping container.

Remove the unit from the bottom of the shipping container. Insure power cable and emulation cable w/terminator are included in the container.

Remove foam pads from floppy disk units, and inspect openings for foreign objects.

Remove the two top cover retaining screws (reference Fig 2-3) from the rear of the unit, and remove the top-cover by moving it towards the rear and upward.

Inspect the inside of the unit for foreign objects, loose mechanical components, and to insure all DC power supply connections are secure.

Check all pluggable components to be sure that they are securely seated on the PC boards.

Check all PC boards to be sure that they are installed in their correct slots (reference Figure 2-1 for locations).

Check all I/O cable connections to be sure that they are secure on the motherboard and the rear of the unit (reference Figure 2-2).

Replace top-cover and secure with two screws, previously removed.

2.2 PRE-POWER CHECKS

The performance of the system can be affected by noise and/or transients entering the system on the primary power input. Therefore, one of the following noise isolation techniques should be used.

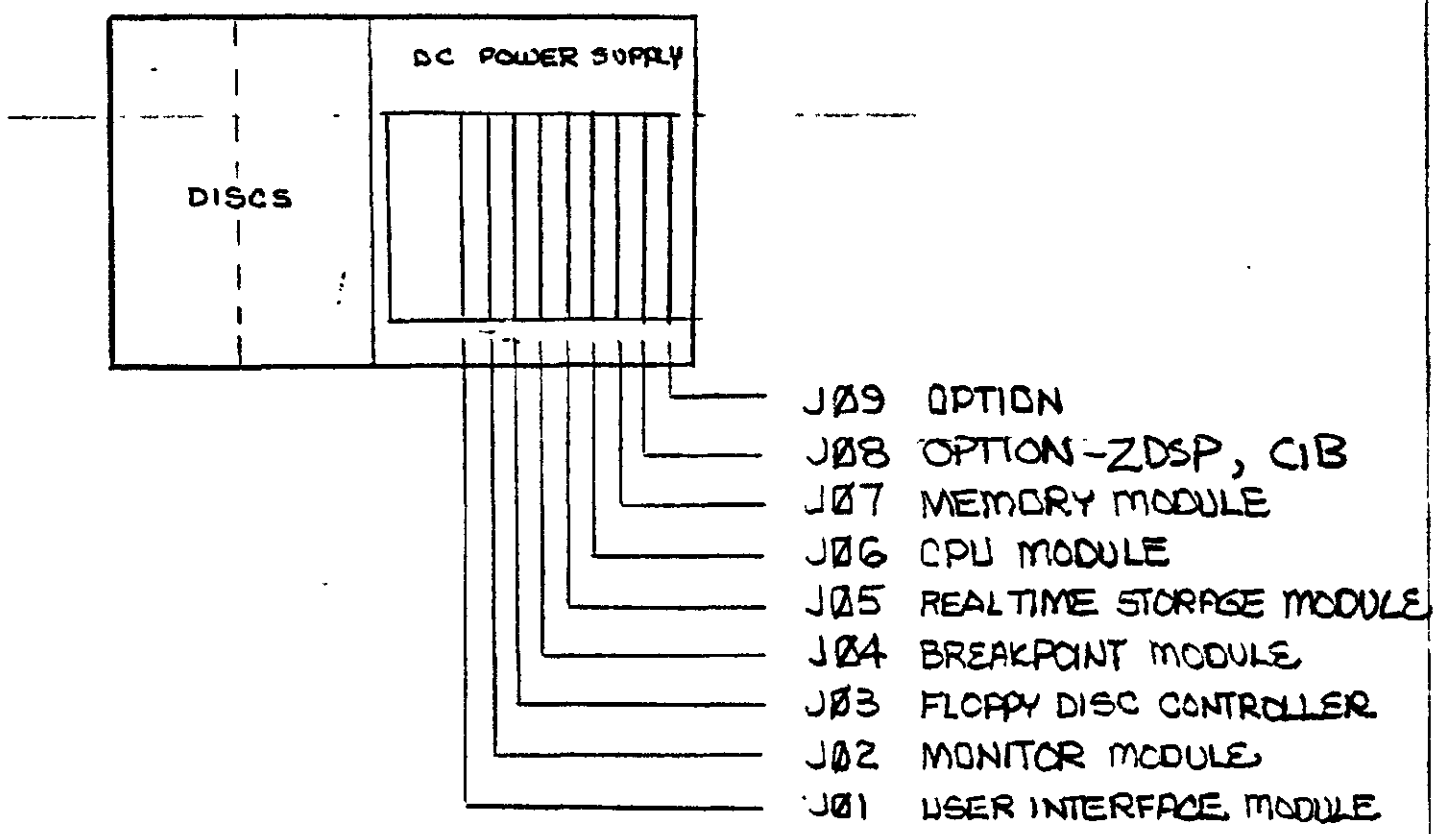


FIGURE 2-1 PC BOARD LOCATIONS

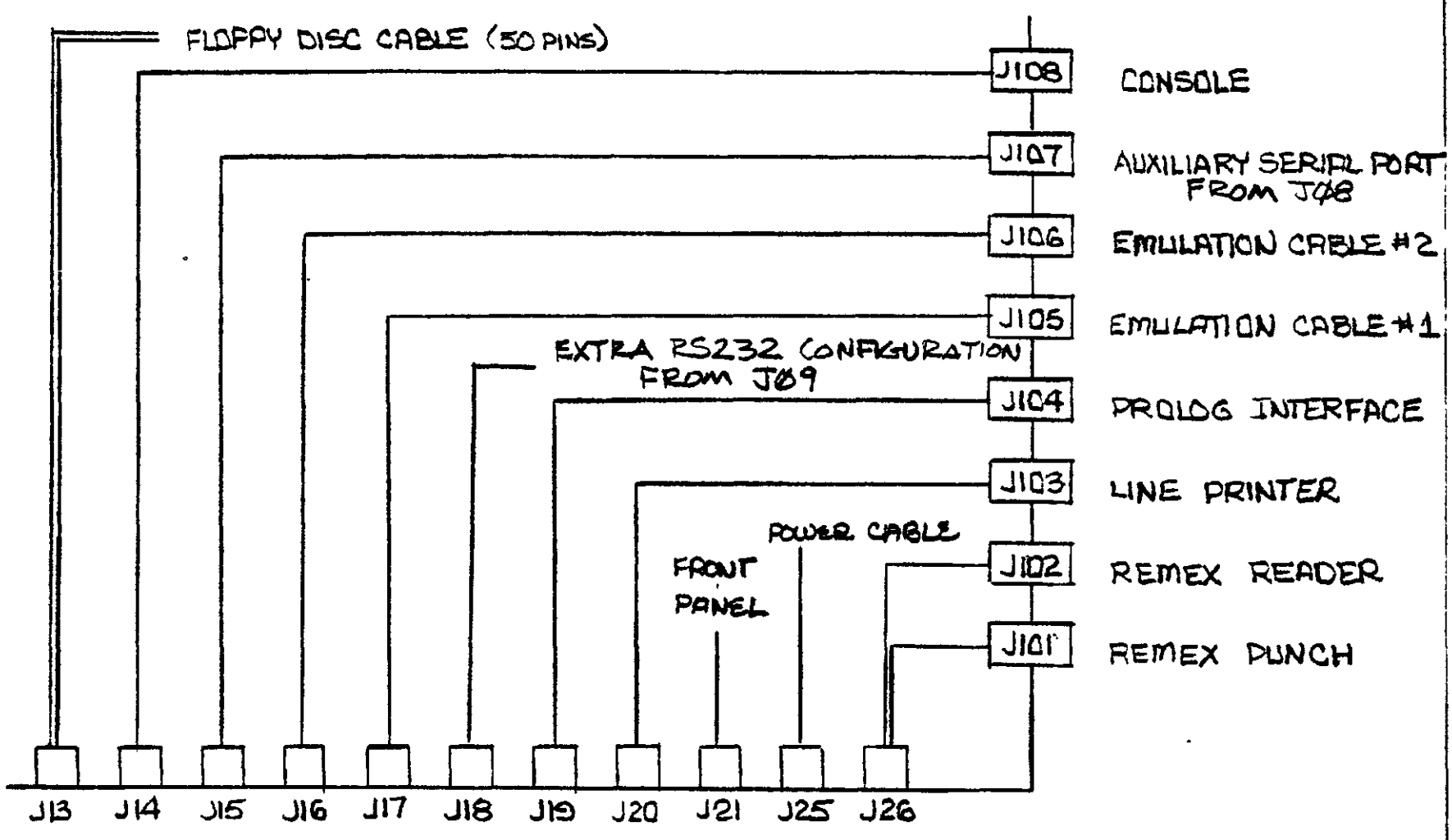


FIGURE 2-2 I/O CONNECTIONS

a. Power-line shielding may be utilized, enclosing the input power lines in rigid conduit or metallic shielding, which is connected to earth ground.

b. Line filters may be utilized to reduce the amplitude of transients on the line.

GROUNDING

The proper grounding of the system is extremely important, especially when connecting the emulation cable to the user's prototype system. Inadequate grounding often causes intermittent problems which may be difficult to isolate. Also, inadequate grounding between the prototye and the development system may result in damage to the emulation interface and/or user's prototype.

All Zilog machine power cords contain an insulated equipment ground wire (green, or green with yellow stripe), which is indentical in size and insulation to the grounded and ungrounded supply conductors. This conductor connects the machine frame ground to a protective ground on the input power plug.

WARNING

An insulated grounding conductor identical in size and insulation to the grounded and ungrounded branch-circuit supply conductors, except that it is green or green with one or more yellow stripes, is to be installed as part of the branch-circuit that supplies the unit. This conductor must be connected at the service equipment. Conduit must not be used as the only grounding medium.

PRIMARY INPUT POWER

Prior to connecting the power cable between the input power source and the system, the source must be checked for proper polarity, voltage and grounding.

Cycles (+/- 1%:)	60HZ	50HZ
Phase:	Single	Single
Voltage (+/- 10%)	110VAC	100/230 VAC
Current:		
Kilovolt Amperes:		

2.3 CONSOLE CONNECTION

A single 25-pin female connector is provided at the rear of the unit for connecting a console driver (reference Figure 2-3). The console device may be any keyboard printer or CRT display device employing an RS-232 or 20 ma. current loop interface. Baud rates for the console may be from 50-9600.

CAUTION

The terminal connector on the rear of the system is shipped with pins 5,6 and 8 wired high. According to standard RS-232 specifications, these pins are designated:

Pin 5-Clear to Send
Pin 6-Data Set Ready
Pin 8-Carrier Detect

These pins serve as TTY.RETURN lines which are pulled up to +12v through 200 ohms.

The only pins used by the RS-232 interface are:

Pin 2-RS232 Data In
Pin 3-RS232 Data Out
Pin 7-RS232 Return

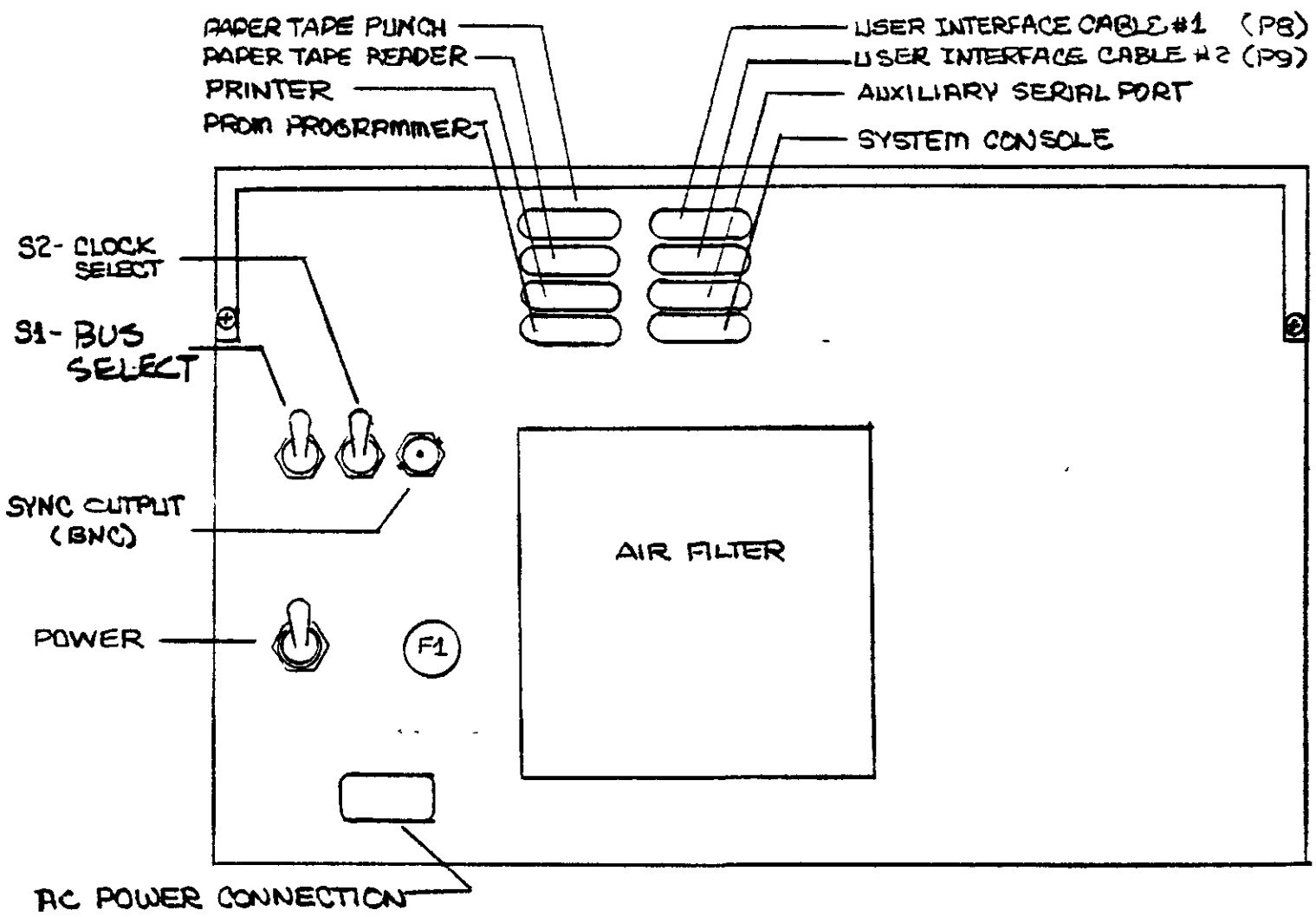
Pins used by the current loops (teletype) interface are:

Pin 10-TTY Data In
Pin 16-TTY Data Out
Pins 5,6,7,24-TTY IN Return
Pin 17-TTY Out Return

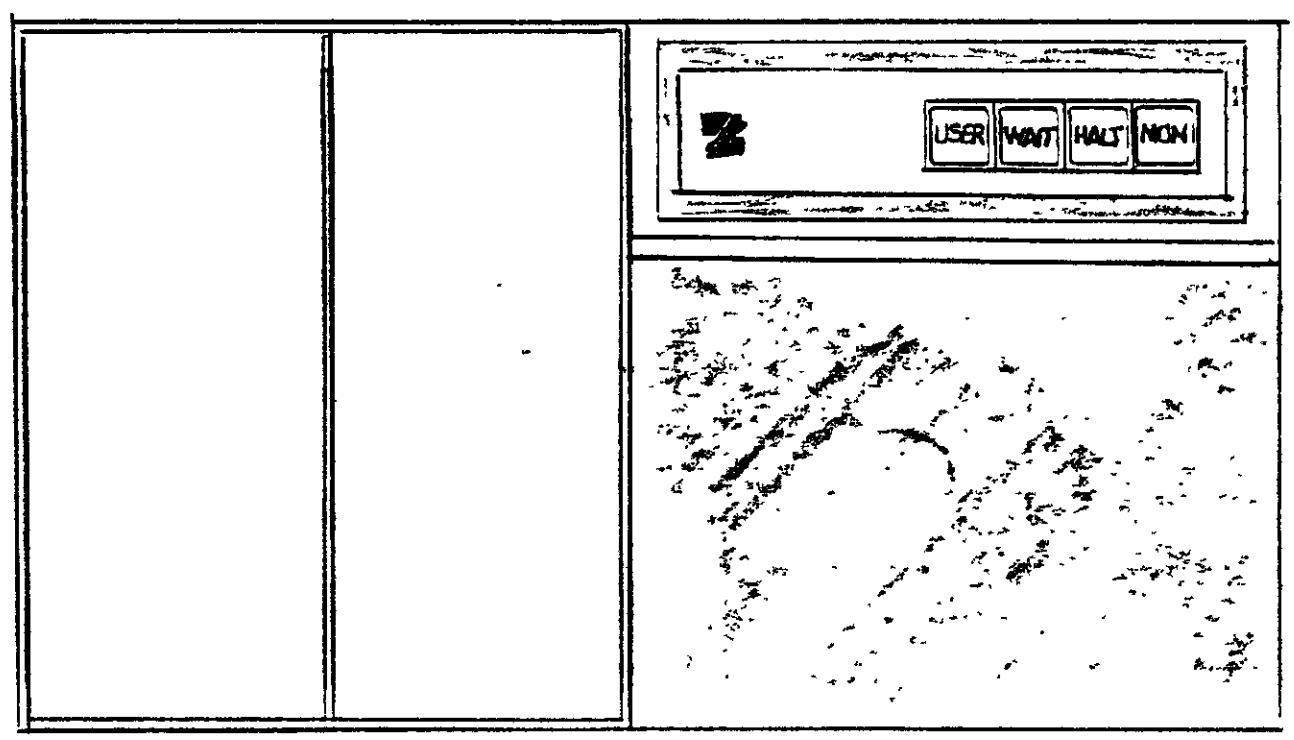
After insuring that correct pin connections exist in the cable from the terminal, the cable may be connected to the terminal connector on the rear of the unit.

2.4 POWER UP SEQUENCE

Apply power to terminal console device and apply power to the ZDS-1/25 by activating the switch on the rear of the unit. The MON indicator should be illuminated and the fan should energize.



REAR VIEW



FRONT VIEW

Figure 2-3 ZDS-1/25 DEVELOPMENT SYSTEM

3.0 MAJOR UNITS

3.1 General Information

The ZDS-1/25 contains the basic hardware of a microcomputer system, plus an emulation subsystem used for real-time hardware and software debugging (reference Figure 3-1). The various modules that comprise the system will be described functionally, concentrating on their inter-relationship and the role they perform in the overall system. For detailed operation of each module, reference Section 4.0 Principles of Operation.

3.2 Microcomputer System

The modules that compose the microcomputer system are the Central Processor Module, Dynamic Memory Module, Floppy Disk Controller Module, and the Optional I/O Modules(s). These are described in the following text with the exception of the I/O Modules which are described in seperate manuals (reference Section 1 for manual title and number).

3.2.1 Central Processor Module (CPU)

The Central Processor Module provides the major control for the system using the Z80-CPU. Resident on the CPU module is the 3K Monitor PROMs which serve to control all debug and emulation activity along with simple I/O drivers for the console and floppy disk interface. A 1K byte static RAM memory is provided to be used as a "scratch pad" for the 3K monitor. All Z80-CPU signals are buffered on the board providing interface to the internal address, data and control busses. Decoding of address signals provides page and card selecct signals used by on board PROM/RAM and the off-board Dynamic Memory Module. The page and card selection forces the 3K Monitor and 1K static RAM to appear at address F000-FFFFH while the system is in MONITOR mode. This feature allows the user to create and debug programs which are located at any address from 0000-EFFFH.

The CPU Card also provides the system with a USART to enable asynchronous interface with the system console device. Baud rate synchronization with the console device is automatic and rates from 50-9600 Baud are supported. Like the Floppy Disk Controller Module, the actual intelligence for this module resides in the 3K PROM Monitor. Also provided is a four-channel counter-timer circuit, Z80-CTC, which is used partially by the system and may be also controlled by the user.

3.2.2 Dynamic Memory Module (DMM)

A single Dymanic Memory Module is provided in the system; it contains a maximum of 60K bytes of storage when 16Kx1 Dynamic RAM components are employed. All refresh timing signals are generated on board and are triggered by the refresh signal from the CPU module. Jumpers on the board allow use of either 16K or 4K memory components by controlling selected address lines received from the CPU module.

3.2.3 Floppy Disk Controller Module (FDC)

The Floppy Disk Controller Module provides an interface between the system and two single-density, single-sided, hard-sectored floppy disk units. Actual intelligence, which is required by the controller, is contained in the 3K Monitor PROM's located on the CPU module. The controller serves as a temporary data buffer, interface to the disks, data modulator, data separator and CRC generator and checker.

3.2.4 Optional I/O Modules

Optional card slots (J8 and J9) are provided for I/O expansion. Any one of the ZDS-1 Series option boards may be installed in one of these slots without modifications to the motherboard wiring. For details regarding these options reference the appropriate manual listed in Section 1.2.

3.3 EMULATION SUBSYSTEM

A group of modules comprise a specialized subsystem within the ZDS-1/25. Its purpose is to monitor and control the interface between the ZDS-1/25 and the user's prototype while performing in-circuit emulation. This subsystem is composed of the following modules described in subsequent subparagraphs below.

- Breakpoint Module
- Real Time Storage Module
- User Interface Module
- Monitor Module

3.3.1 Breakpoint Module (BKPT)

The Breakpoint Module provides the user with a means to terminate execution of a program when specified conditions of the address, data or control bus occur. This feature is

most useful when debugging programs or hardware that run in real-time. The breakpoint allows real-time execution of a program until the selected event occurs, at which time one of two events may occur: first, the user may wish to stop program execution or break on the event so that CPU registers, memory or the real-time storage module may be examined; second, the user may wish to generate a sync pulse on the occurrance of the event to trigger external test equipment to monitor the event in his own hardware. Either of these can be accomplished easily by entering the desired parameter from the system console.

The Breakpoint Module is loaded (with the parameters entered via the system console) by the 3K Monitor PROM. These parameters, called "arguments," may be any one or a combination of the following:

- CONTROL ARGUMENTS:
  - M1 Op Code Fetch
  - MR Memory Read
  - MW Memory Write
  - PR Port (I/O) Read
  - PW Port (I/O) Write

- ADDRESS ARGUMENTS
  - A Memory Address
  - P Port (I/O) Address

- DATA ARGUMENT
  - D Data Byte
  - M Data Mask

3.3.2 Real Time Storage Module (RTSM)

The Real Time Storage Module provides a means for the system to store selected bus transactions while executing a program. This feature allows the system to trace address, data and control bus lines in real time execution of the user's program to provide a history of the most current 256 selected events. The user may display the contents of the history on the system console to analyze the execution of the program under test.

Control of the RTSM is provided by the emulation subsystem, (while executing the user's program) to enable real-time storage of bus activity. Parameter loading and display of the history is controlled by the 3K PROM Monitor on the CPU module. The user may select any one or a combination of the trace parameters to trace:

- Memory Reads
- Memory Writes
- Port (I/O) Reads
- Port (I/O) Writes
- All Read Operations
- All Write Operations
- All Port Operations
- All Memory Operations
- All Operations

3.3.3 User Interface Module (UIM or Mapper/ICE)

The User Interface Module provides the electrical interface between the emulation subsystem and the user's prototype system so that in-circuit emulation may occur. Connection between the ZDS-1/25 and the user's prototype is achieved by a three-foot cable and termination block. The M/ICE contains receivers, drivers and interface controls, as well as a memory mapper.

Memory mapping allows the user's prototype system to borrow blocks of development system memory, each block being composed of 256 bytes. Typically, this feature is used when the user is developing software that will eventually reside in PROM on the prototype. By means of the mapper, the user may borrow blocks of memory from the development system memory as though it were resident in his prototype without any degradation in system speed.

The mapper is loaded to the configuration desired by the user by executing a disk resident program called "MAPPER." Once the map is loaded, the user may enable the map or disable the map using one of the methods shown below. Control of bus access is provided by Switch One (S1) on the rear of the unit.

TO ENABLE MAPPER LOGIC:

- Place MEM select switch (S1) to map EXT (sw down) and issue a port write to EEH with data bit D1 low.

TO DISABLE MAPPER LOGIC (use one of the following):

- Place MEM select switch (S1) to internal MEM (sw up)
- Execution of Port Write to I/O Port EEH with data bit D1 high
- Operator depresses the WAIT button (System Reset)

Also provided on the M/ICE is clock selection logic, which selects the clock source for the Z80-CPU while running emulations, i.e., internal (2.5 MHZ) or external (variable). Clock selection is controlled by S2 on the rear of the unit; UP for internal, driving clock, DOWN for external clock.

3.3.4 Monitor Module (MON.25)

Although the monitor module provides several diskrete functions for the system, its primary purpose is to provide various strobes and controls used by the emulation subsystem. The diskrete functions provided by the monitor are as follows:

- Console Electrical Interface - provides receiver and driver circuits which allow use of standard RS-232 or current loop device as the system console. The method of interface determines which receivers and drivers are employed.

- Operator Panel Interface - provides debounce circuitry for the MON, USER, WAIT, S1 and S2 switches; provides lamp drivers for MON, WAIT, HALT and USER indicators; provides switch synchronization logic between modes and system logic functions to prevent undesirable disruption of system timing.

- System I/O Port Decode - provides decoding logic for Z80-CPU address bits A0-A7 to select system address ports of F0-FFH and to prevent user's prototype from addressing the system I/O ports E0-FFH.

The remainder of the logic on the monitor is used to generate control signals used by the emulation subsystem to sample data, address and control busses, or to provide control of the interface to the user's prototype and synchronize the emulation subsystem to the user supplied clock if external clock is selected.

4.0 PRINCIPLES OF OPERATION

4.1 GENERAL INFORMATION

The following discussion describes the detailed operation of each p.c. board used in the ZDS-1/25 Development System. A block diagram of each board is provided, showing the various functional units on the board, which are then related to a specific logic Sheet number for further circuit clarification.

4.2 CENTRAL PROCESSOR MODULE

The processor card contains a Z80-CPU, Z80 CTC and USART for console interface, plus 3K of PROM and 1K of static RAM for controlling the debug environment. System PHI is derived from a 19.6608 MHZ oscillator is provided to the floppy disk controller for synchronous data separation.

The CPU bus is fully buffered to support stand alone system operation with full memory and I/O compliments.

The relationship of these elements is represented in Figure -----.

4.2.1 Z80 Microprocessor (Sheet 1)

The Z80-CPU serves as the control for the system. It is shared by both the system (MONITOR MODE) and the emulation subsystem (USER MODE). The Z80-CPU does not differientiate between executing programs in USER or MONITOR MODES as a consequence the surrounding logic of the microcomputer system and emulation subsystem must make the distinction. The processor operates in a normal fashion fetching and executing instructions from storage either PROM or RAM as described in the Z80-CPU Technical Manual.

4.2.2 Reset Logic (Sheet 1)

The Z80-CPU may be reset by one of several conditions. This reset operation will result in the following:

- Program Counter will be reset (0000H)
- Interrupt Enable flip-flop will be reset, disabling all maskable interrupts.
- Interrupt Page Address Register (I) will be cleared.
- Memory Refresh Register (R) will be cleared.
- Interrupt Mode 0 will be established.
- Address and data bus go to a high impedance state while RESET is active (logic 0). Also, all control output signals go to their inactive state.

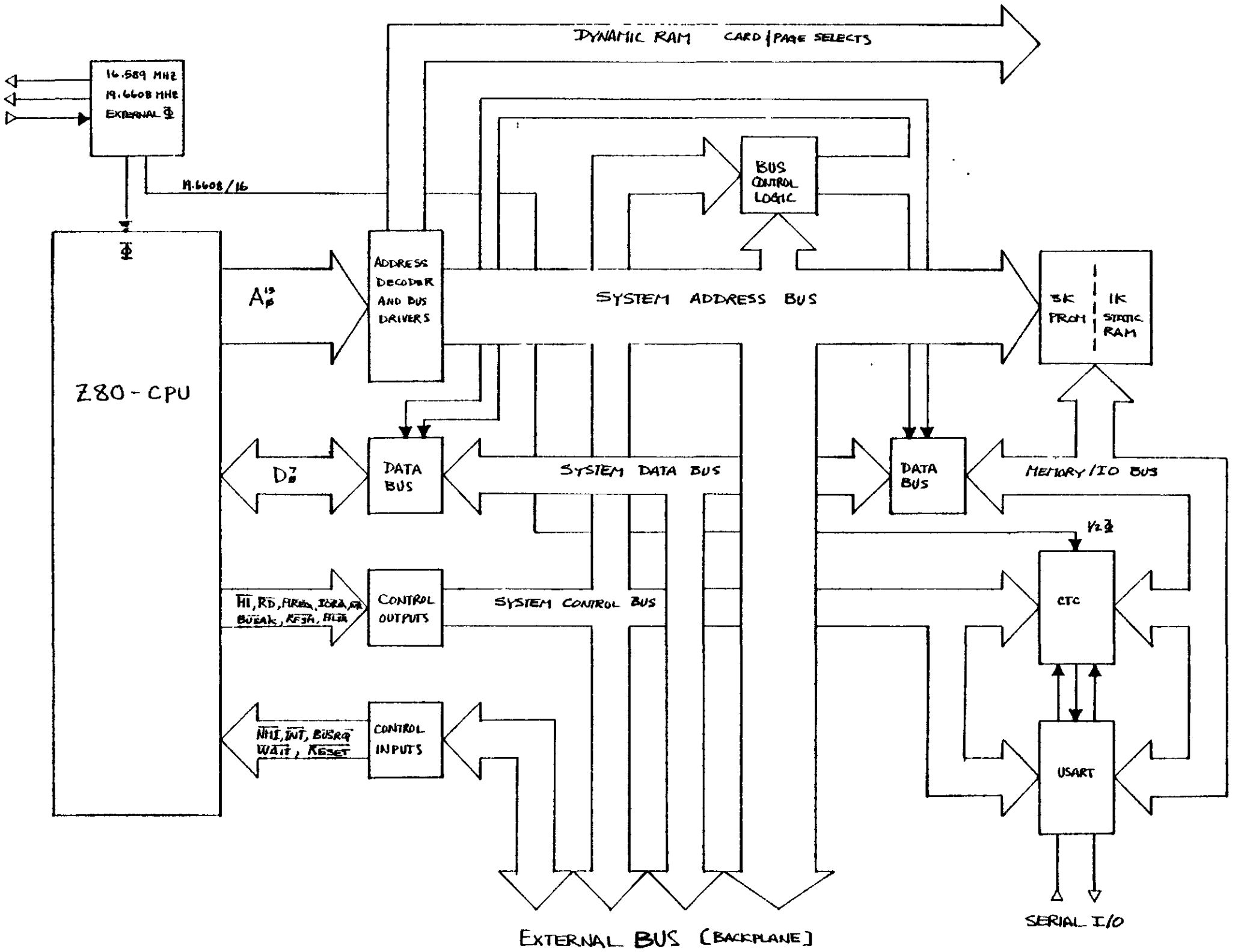


FIGURE 4-1. CPU-2 BLOCK DIAGRAM

Reset logic circuitry is triggered by one of the following events:

- RESET SW (Reset Switch) occurs when the operator depresses the momentary switch (WAIT) on the front panel of the unit. Debounce circuitry is provided (logic Sheet 1) via C3 and R2 on the CPU board.
- RESTART is generated from the mode change logic on the moniter module and is the result of one of the following events:

  - BREAK signal from the Breakpoint Module, indicating a comparison between the argument registers and the bus activity.

  - Switching between MONITOR and USER modes, either by operator pressing MON or USER buttons, or a software generated mode change from the 3K PROM Debug firmware.

- SYS RESET does not directly reset the Z80-CPU, but instead generates the RESTART signal previously described. The SYS RESET signal may be generated by (1) power-on clear signal, (2) software reset commands, or (3) mode change from MONITOR to USER or visa versa.

Two outputs are generated by the reset logic; one is applied directly to the Z80-CPU as a reset while the second output, POWER ON CLR, is applied to the User Interface Module, Monitor Module and the Option card slot as a reset.

4.2.3 CLOCK GENERATOR (Sheet 1)

The Z80 CPU bus buffers are shown on Sheet One of the schematics. System PHI is generated by hybrid oscillator A29. Counter A22 produces the 2.46 MHz system clock as well as half PHI for baud rate timing. The discrete circuit oscillator is controlled by a 16.589 MHz crystal and is used by the floppy controller's synchronous data separator.

Data bus buffer A31 interfaces the CPU to the system bus (backplane) and drives toward the CPU during M1 or Read cycles. Buffers A26 and A23 drive the system address bus. A32 drives outbound control signals such as M1, IORQ, RD, etc., while A27 receives user provided inputs, e.g., INT, NMI, RESET, etc.

In actuality, system PHI is provided by the User Interface Module, which determines the appropriate development system clock. Zilog clock driver A25 provides a MOS compatible clock source for the LSI devices.

4.2.4 CONTROL BUFFER (Sheet 2)

Sheet 2 of the schematics detail the PROM/RAM implementation and the bus control logic for both A31 and A16 bus buffers.

Chip selects for A17-A19 and A13, A14 occur when PROM addresses are decoded by Sheet 3 logic. These decoded addresses, along with I/O and interrupt requests from peripherals A20 and A21 (Sheet 4) cause bus driver A16 to drive the system data bus toward the CPU.

Automatic baud rate timing is acquired through tristate driver A28 and data bit D0, through Port FFH.

The Development System 3K Monitor is intended to provide the basic debugging commands, basic Input/Output driver firmware and bootstrap portion of a floppy disk-based operating system. The operation of this firmware is described in the ZDS-1/25, 1/40 PROM MANUAL.

4.2.5 DATA BUFFER (Sheet 3)

Sheet 3 depicts the address decoding assignments for the following:

PROM Firmware	F000-FFFF HEX
Dynamic Memory	0-EFFF HEX
System Ports	F0-FF HEX

Adder A34 translates monitor mode addresses from 00 to F000 placing memory select decoder A33 in the user address space (RAM at zero). Gates A7 and A11 generate the page 15 address enable which allows monitor mode PROM accesses. System I/O ports are decoded by the logic of A2 and A3.

4.2.6 ADDRESS BUFFER AND DECODER (Sheets 1, 2, and 4)

Sheet 4 contains the peripherals found on the CPU2 card. The console interface is implemented by way of USART A21, and CTC provides interrupt capability for the floppy disk interface and the USART status lines. Jumper E1 and E2 allow receiver interrupts from the USART. Flop flop A8 provides a square-wave baud-rate clock source to the USART.

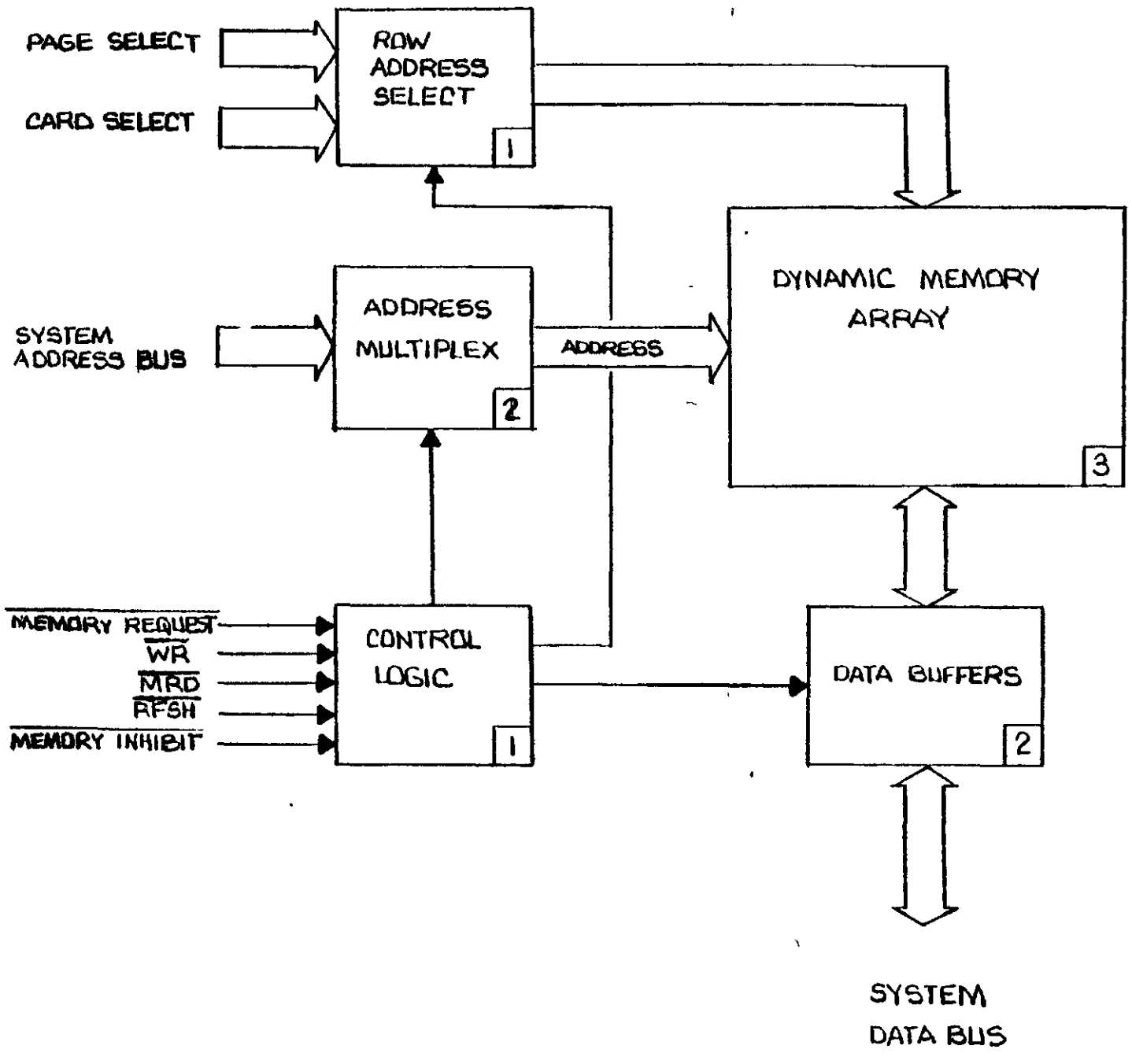


Figure 4-2 DYNAMIC MEMORY MODULE

4.2.7 Z80-CTC (Counter Timer Circuit)

4.2.7.1 CTC Pin Description

D0-D7

Z80-CPU Data Bus (bi-directional, tri-state).

This bus is used to transfer all data and command words between the Z80-CPU and the Z80-CTC. There are 8 bits on this bus, of which D0 is the least significant.

CS1-CS0

Channel Select (input, active high)

These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O write or read. (See truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

CE-

Chip Enable (input, active low)

A low level on this pin enables the CTC to accept control words, interrupt vectors, or time constant data words from the Z80 data bus during an I/O write cycle, or to transmit the contents of the down counter to the CPU during an I/O ready cycle. In most applications, this signal is decoded from the 8 least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four counter/timer channels.

Clock (phi)

System Clock (input)

This single-phase clock is used by the CTC to synchronize certain signals internally.

M1-

Machine Cycle One Signal from CPU (input, active low)

When M1- is active and the RD- signal is active, the CPU is fetching an instruction from memory. When M1- is active and the IORQ- signal is active, the CPU is acknowledging an interrupt, alerting the CTC to place an interrupt vector on the Z80 data bus if it has daisy chain priority and one of its channels has requested an interrupt.

IORQ-

Input/Output Request from CPU (input, active low)

The IORQ- signal is used in conjunction with the CE- and RD- signals to transfer data and channel control words between the Z80-CPU and the CTC. During a CTC write cycle, IORQ- and CE- must be true and RD- false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid RD- signal. In a CTC read cycle, IORQ-, CE-, and RD- must be active to place the contents of the down counter on the Z80 data bus. If IORQ- and M1- are both true, the CPU is acknowledging an interrupt request, and the highest-priority interrupting channel will place its interrupt vector on the Z80 data bus.

RD-

Read Cycle Status from the CPU (input, active low)

The RD- signal is used in conjunction with the IORQ- and CE- signals to transfer data and channel control words between the Z80-CPU and the CTC. During a CTC write cycle, IORQ- and CE- must be true and RD- false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid RD- signal. In a CTC read cycle, IORQ-, CE-, and RD- must be active to place the contents of the down counter on the Z80 data bus.

IEI

Interrupt Enable In (input, active high)

This signal is used to help form a system-wide interrupt daisy chain which establishes priorities when more than one peripheral device in the system has interrupting capability. A high level on this pin indicates that no other interrupting devices of higher priority in the daisy chain are being

serviced by the Z80-CPU.

IEO

Interrupt Enable Out (output, active high)

The IEO signal, in conjunction with IEI, is used to form a system-wide interrupt priority daisy chain. IEO is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. Thus, this signal blocks lower priority devices from interrupting while a higher priority interrupting device is being serviced by the CPU.

INT-

Interrupt Request (output, open drain, active low)

This signal goes true when any CTC channel which has been programmed to enable interrupts has a zero-count condition in its down counter.

RESET-

Reset (input, active low)

This signal stops all channels from counting and resets channel interrupt enable bits in all control registers, thereby disabling CTC-generated interrupts. The ZC/TO and INT- outputs go to their inactive states, IEO reflects IEI, and the CTC's data bus output drivers go to the high impedance state.

CLK/TRG3-CLK/TRG0

External Clock/Timer Trigger (input, user-selectable active high or low)

There are four CLK/TRG pins, corresponding to the four independent CTC channels. In the counter mode, every active edge on this pin decrements the down counter. In the timer mode, an active edge on this pin initiates the timing function. The user may select the active edge to be either rising or falling.

ZC/TO2-C/TO0

Zero Count/Timeout (output, active high)

There are three ZC/TO pins, corresponding to CTC channels 2

through 0. (Due to package pin limitations, channel 3 has no ZC/TO pin.) In either counter mode or timer mode, when the down counter decrements to zero, an active high going pulse appears at this pin.

4.2.7.2 CTC Programming

Before a Z80-CTC channel can begin counting or timing operations, a channel control word and a time constant data word must be written to it by the CPU. These words will be stored in the channel control register and the time constant register of that channel. In addition, if any of the four channels have been programmed with bit 7 of their channel control words to enable interrupts, an interrupt vector must be written to the appropriate register in the CTC. Due to automatic features in the interrupt control logic, one pre-programmed interrupt vector suffices for all four channels.

Loading the Channel Control Register

To load a channel control word, the CPU performs a normal I/O write sequence to the port address corresponding to the CTC channel. Two CTC input pins, namely CS0 and CS1, are used to form a 2-bit binary address to select one of four channels within the device. In many system architectures, these two input pins are connected to address bus lines A0 and A1, respectively, so that the four channels in a CTC device will occupy contiguous I/O port addresses. A word written to a CTC channel will be interpreted as a channel control word, and loaded into the channel control register, with bit 0 being a logic 1. The other seven bits of this word select operating modes and conditions as indicated in the diagram below. Following the diagram, the meaning of each bit will be discussed in detail.

D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Enable	Mode	Range*	Slope	Trigger*	Load Time Constant	Reset	1

* Used in timer mode only

Bit 7=1

The channel is enabled to generate an interrupt request sequence every time the down counter reaches a zero-count

condition. To set this bit to 1 in any of the four channel control registers necessitates that an interrupt vector also be written to the CTC before operation begins. Channel interrupts may be programmed in either counter mode or timer mode. If an updated channel control word is written to a channel already in operation with bit 7 set, the interrupt enable selection will not be retroactive to a preceding zero-count condition.

Bit 7=0

Channel interrupts disabled.

Bit 6=1

Counter mode selected. The down counter is decremented by each triggering edge of the external clock (CLK/TRG) input. The prescaler is not used.

Bit 6=0

Timer mode selected. The prescaler is clocked by the system clock , and the output of the prescaler in turn, clocks the down counter. The output of the down counter (the channel's ZC/TO output) is a uniform pulse train of periods given by the product

$$t * P * TC$$

where t is the period of system clock , P is the prescaler factor of 16 or 256, and TC is the time constant data word.

Bit 5=1

(Defined for timer mode only.) Prescaler factor is 256.

Bit 5=0

(Defined for timer mode only.) Prescaler factor is 16.

Bit 4=1

Timer mode - positive edge trigger starts timer operation.
Counter mode - positive edge decrements the down counter.

Bit 4=0

Timer mode - negative edge trigger starts timer operation.
Counter mode - negative edge decrements the down counter.

Bit 3=1

Timer mode only - external trigger is valid for starting timer operation after rising edge of T of the machine cycle following the one that loads the time constant. The prescaler is decremented two clock cycles later if the setup time is met, otherwise, three clock cycles.

Bit 3=0

Timer mode only - timer begins operation on the rising edge of T of the machine cycle following the one that loads the time constant.

Bit 2=1

The time constant data word for the time constant register will be the next word written to this channel. If an updated channel control word and time constant data word are written to a channel while it is already in operation, the down counter will continue decrementing to zero before the new time constant is loaded into it.

Bit 2=0

No time constant data word for the time constant register should be expected to follow. To program bit 2 to this state implies that this channel control word is intended to update the status of a channel already in operation, since a channel will not operate without a correctly programmed data word in the time constant register, and a set bit 2 in this channel control word provides the only way of writing to the time constant register.

Bit 1=1

Reset channel. Channel stops counting or timing. This is not a stored condition. Upon writing into this bit, a reset pulse discontinues current channel operation, however, none of the bits in the channel control register are changed. If both bit 2=1 and bit 1=1, the channel will resume operation upon loading a time constant.

Bit 1=0

Channel continues current operation.

A channel may not begin operation in either timer mode or counter mode unless a time constant data word is written into

the time constant register by the CPU. This data word will be expected on the next I/O write to this channel following the I/O write of the channel control word, provided bit 2 of the channel control word is set. The time constant data word may be any integer value in the range 1-256. If all eight bits in this word are zero, it is interpreted as 256. If a time constant data word is loaded to a channel already in operation, the down counter will continue decrementing to zero before the new time constant is loaded from the time constant register to the down counter.

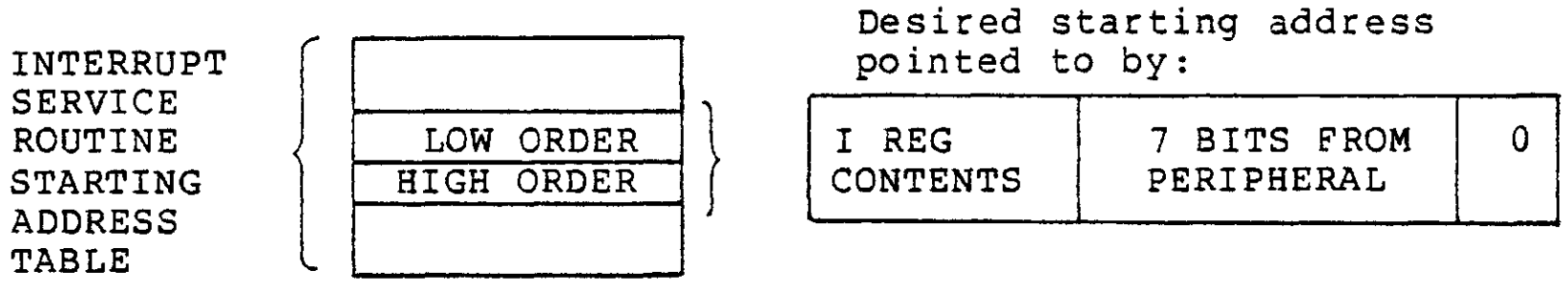
Time Constant Register

D7	D6	D5	D4	D3	D2	D1	D0
TC7	TC6	TC5	TC4	TC3	TC2	TC2	TC0

MSB LSB

The Z80-CTC has been designed to operate with the Z80-CPU programmed for mode 2 interrupt response. Under the requirements of this mode, when a CTC channel requests an interrupt and is acknowledged, a 16-bit pointer must be formed to obtain a corresponding interrupt service routine starting address from a table in memory. The upper 8 bits of this pointer are provided by the CPU's I register, and the lower 8 bits of the pointer are provided by the CTC in the form of an interrupt vector unique to the particular channel that requested the interrupt.

MODE 2 INTERRUPT OPERATION



The high order 5 bits of this interrupt vector must be written to the CTC in advance as part of the initial programming sequence. To do so, the CPU must write to the I/O port addresses corresponding to the CTC channel 0, just as it would if a channel control word were being written to that channel, except that bit 0 of the word being written must contain a 0. (As explained above in Section 3.1, if bit 0 of a word written to a channel were set to 2, the word would be interpreted as a channel control word, so a 0 in bit

0 signals the CTC to load the incoming word into the interrupt vector register.) Bits 1 and 2, however, are not used when loading this vector. At the time when the interrupting channel must place the interrupt vector on the Z80 data bus, the interrupt control logic of the CTC automatically supplies a binary code in bits 1 and 2 identifying which of the four CTC channels is to be serviced.

Channel 2 - Baud Rate Generation

This channel may be operated in either counter or timer mode and is triggered or clocked by the output of A4-pin 9. Once the counter decrements to zero, the ZC2 output goes active (high) to clock the second stage of A4 whose output provides the transmit and receive clocks to the USART.

Channel 3 - USART Transmit Interrupt Generator

This channel allows the USART to have interrupt capability with the system. This channel will generate an interrupt upon receiving a TxRDY signal from the USART.

4.2.8 USART Operation

4.2.8.1 USART Signal Description

Data Bus (D0-D7)

This tree-state, 8-bit bus is used for information exchange between the USART and the host processor. Data, controk , andd stat6us bytes are exchanged upon execution of input and output instructions from the Z80.

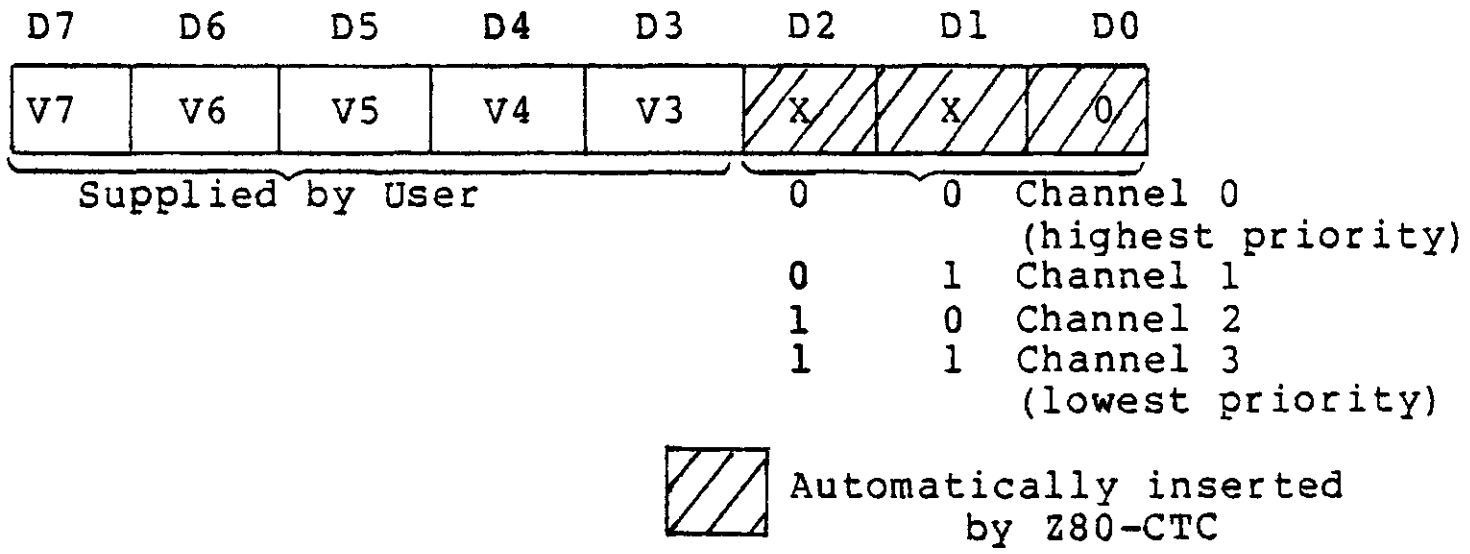
Reset (RST)

The USART will assume an idle sstate when a high level is applied to the reset input. When the reset is returned low, the USART will remain in the idle state until it receives a new mode control instruction.

Clock (CLK)

This input is used for internal timing within the USART. It does not control the transmit or rec3eive rate. However, it should be at least 30 times the reeceive or transmit rate in the synchronous mode and 4.5 times the receive or trasnmit rates in the asynchronous mode. The CLK frequency is also restricted by both an upper and a lower bound.

INTERRUPT VECTOR REGISTER



4.2.8.2 CTC Utilization

All four channels of the Z80-CTC are used by the system for various timing functions. The channels used and their purpose are shown below:

Channel 0 - Sector Counter

This channel is operated in counter mode and is used as a Sector Counter for the Floppy Disk Controller. Interrupts are used with this channel to flag software as to when the appropriate number of sector pulses have been received from the disk so that the heads may be loaded. This counter is incremented by the signal, INDX, from the Flopppy Disk Controller Module.

Channel 1 - Bit Measurement

This channel is operated in timer mode and is triggered by the RCUR OUT signal from the Serial Latches on the CPU module. The output of the channel (ZC1) becomes RCV CLK which is routed to the CPU module to clock the RCVR OUT signal into the Serial Latches.

Control/Data (C/D)

During a read operation, if this input is at a high level, the status byte will be read, and if it is at a low level, the receive data will be read by the processor. When a write operation is being performed, this input will indicate to the USART that the bus information being written is a command if

C/D is high and data if C/D is low.

C/D-	RD-	WR-	CS-	
0	0	1	0	USART DATA-->DATA BUS
0	1	0	0	DATA BUS-->USART DATA
1	0	1	0	USART STATUS-->DATA BUS
1	1	0	0	DATA BUS-->USART COMMAND
X	X	X	1	DATA BUS-->3-STATE

Read (RD-)

This active low input enables data or status to be transferred from the USART to the Z80.

Write (WR-)

This active low input enables data or control to be transferred to the USART from the Z80.

Chip Select (CS-)

This active low input enables the processor to access the USART for an I/O operation. When CS- is high, the data bus output is in the high impedance state.

Data Set Ready (DSR-)

This is a general-purpose input signal and forms part of the status byte that may be read by the processor. DSR- is generally used as a response to DTR by the modem to indicate that it is ready. The signal acts only as a flag and does not control any internal logic.

Data Terminal Ready (DTR-)

This output signal reflects the condition of bit 1 in the command byte from the Z80. The DTR signal is commonly used for data terminal ready or rate select in modem control.

Clear to Send (CTS-)

This is a general-purpose input signal used to enable the USART to transmit data if the TxEN bit in the command byte is a one. CTS- is generally used as a response to RTS- by a modem to indicate that transmission may begin. Designers not using CTS- in their systems should remember to tie it low so that USART data transmission will not be disabled.

Request to Send (RTS-)

This output signal reflects the condition of bit 5 in the command byte from the Z80. The RTS- signal is commonly used to initiate a data transmission by requesting the modem to prepare to send.

Transmit Data (TxD)

Data from the data bus is converted to a serial format with appropriate sync, start/stop, and parity information inserted into the data stream. This bit stream is then transmitted to the TxD output.

Transmitter Ready (TR)

The TR output signal goes high when data in the transmit data buffer has been shifted into the transmitter section allowing the transmit data buffer to accept the next byte from the processor. TR will be reset when information is written into the transmit data buffer. Loading the command register also resets TR. TR will be available on this output pin only when the USART is enabled to transmit (CTS-=0, TxEN=1). However, the TxRDY bit in the status buffer will always be set when the transmit data buffer is empty regardless of the state of TxEN and CTS-.

TR can be tested by checking bit 0 of the status register for polling operation or the TR signal can be used to generate an interrupt. On the SCON, CTC2 is used to receive the active high TR signal from the USART to decrement a counter from 1 to 0, and consequently, provide a Z80 mode 2 interrupt vector.

Transmitter Clock (TxC-)

The transmitter clock controls the serial character transmission rate. In the asynchronous mode, the TxC- frequency is a multiple of the actual baud rate. Bits 0 and 1 of the mode instruction select the multiple to be 1x, 16x, or 64x the baud rate. In the synchronous mode, the TxC- frequency is automatically selected to equal the actual baud rate.

Note that for both synchronous and asynchronous modes, serial data is shifted out of the USART by the falling edge of TxC-.

Receive Data (RxD)

Composite serial data is received at this input and converted

to a parallel format; sync, start/stop, and parity are checked, and then the assembled byte is prepared for buffering to the Z80. For communications requiring less than 8 bits per character, the extra bits are set to logical "zero".

Receiver Ready (RR)

The RR output signal indicates to the processor that data has been shifted into the receiver buffer from the receiver section and may be read. The signal is active high and will be reset when the buffer is read by the processor. RR can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver may be running. If the processor does not read the receiver buffer before the next character is shifted from the receiver section, then an overrun error will be indicated in the status buffer.

RR can be tested by checking bit 1 of the status register for polling operation or the RR signal can be used to generate an interrupt. On the SCON, CT1 may be used to receive the active high RR signal from the USART to decrement a counter from 1 to 0, and consequently, provide a Z80 mode 2 interrupt vector.

Receiver Clock (RxC-)

The receiver clock is the rate at which the incoming character is received. In the asynchronous mode, the RxC frequency may be 1, 16, or 64 times the actual baud rate, but in the synchronous mode, the RxC- frequency must equal the baud rate. Bits 0 and 1 in the mode instruction select asynchronous at 1x, 16x, or 64x or synchronous operation at 1x the baud rate.

Unlike TxC-, data is sampled by the USART on the rising edge of RxC-. Since the USART will frequently be handling both the reception and transmission for a given link, the receive and transmit baud rates will be the same. RxC- and TxC- then require the same frequency and may be tied together and connected to a single clock source or baud rate generator.

Sync Detect (SYNC)

This signal is used only in the synchronous mode. It can be an input or output depending on the USART mode instruction, programming the operation for external or internal synchronization, respectively. In the internal sync mode, the SYNC "output" will go to a logical one when the USART has

identified the sync character in the receiver data stream. If the USART is programmed for "bi-sync" operation, the sync output will not go to a logical one until the second consecutive sync character has been identified. In both cases, the sync output transition from low to high will occur in the middle of the last bit of the respective sync character. Sync and bit 6 (sync) in the status register are reset when the status buffer is read or when a device RST occurs.

In the external sync mode, a positive edge on the sync "input" will cause the USART to start assembling a data byte on the next falling edge of RxC-. The sync signal should remain high for at least one RxC- period.

4.2.8.3 USART Operation

A set of control words must be sent to the USART to define the desired mode and communications format. The control words will specify the baud rate factor (1x, 16x, 64x), character length (5 to 8), number of stop bits (1, 3/2, 2), asynchronous or synchronous mode, syndet (internal or external), parity, etc.

After receiving the control words, the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the USART may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

NOTE: The 8251 and 9551 USARTs may provide faulty data from the receiver buffer for the first read after power-on. A dummy read is recommended.

The USART cannot transmit until the TxEN (Transmitter Enable) bit has been set by a command instruction and until the CTS- (Clear to Send) input is a "zero".

4.2.8.4 USART Programming

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the

communications interface. If an external reset is not available, three successive zeros followed by a reset command instruction can be used to initialize the USART. TxD is held in the "marking" state after reset, waiting for a new command instruction.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This control word specifies the general characteristics of the interface regarding the synchronous or asynchronous mode, baud rate factor, character length, parity, and number of stop bits. Once the mode instruction has been received, sync characters or command instructions may be inserted depending on the mode instruction content.

Command Instruction

This control word directs the actual operation of the format selected in the mode instruction. Functional control of transmit and receive, error reset, reset, and modem signals are accommodated in the command instruction.

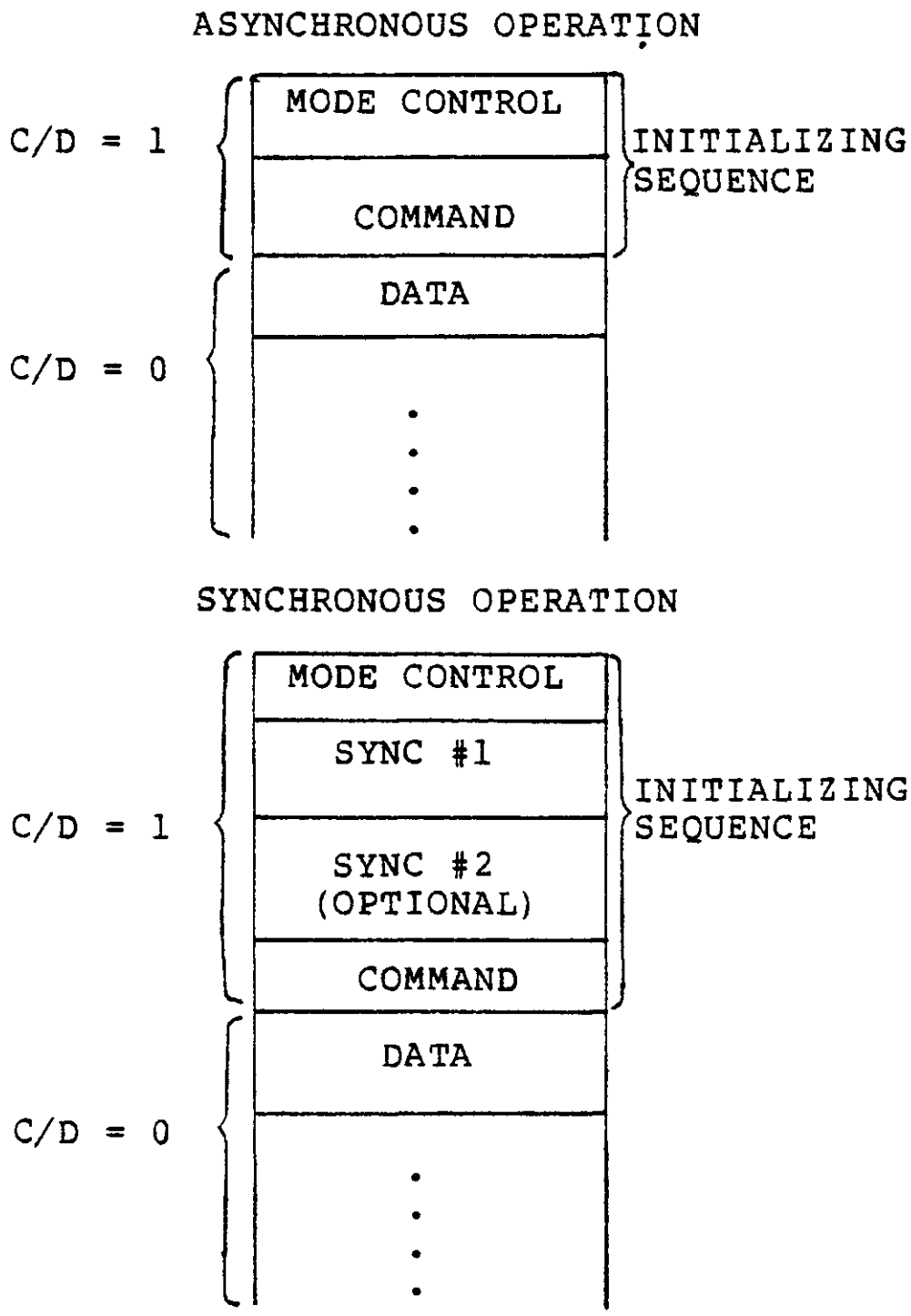


FIGURE 4-13: Control Word Sequence for Initialization

Only a single address is set aside for mode control bytes, command bytes, and sync character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as sync characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following an external reset signal or following an internal reset command.

Mode Control Codes

The USART interprets mode control codes as illustrated in Figures 4-14 and 4-15.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between the data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus, in synchronous mode, a character will consist of five, six, seven, or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven, or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1 1/2, or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1 1/2 stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When syndet is an output, internal synchronization is specified; one or two sync characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

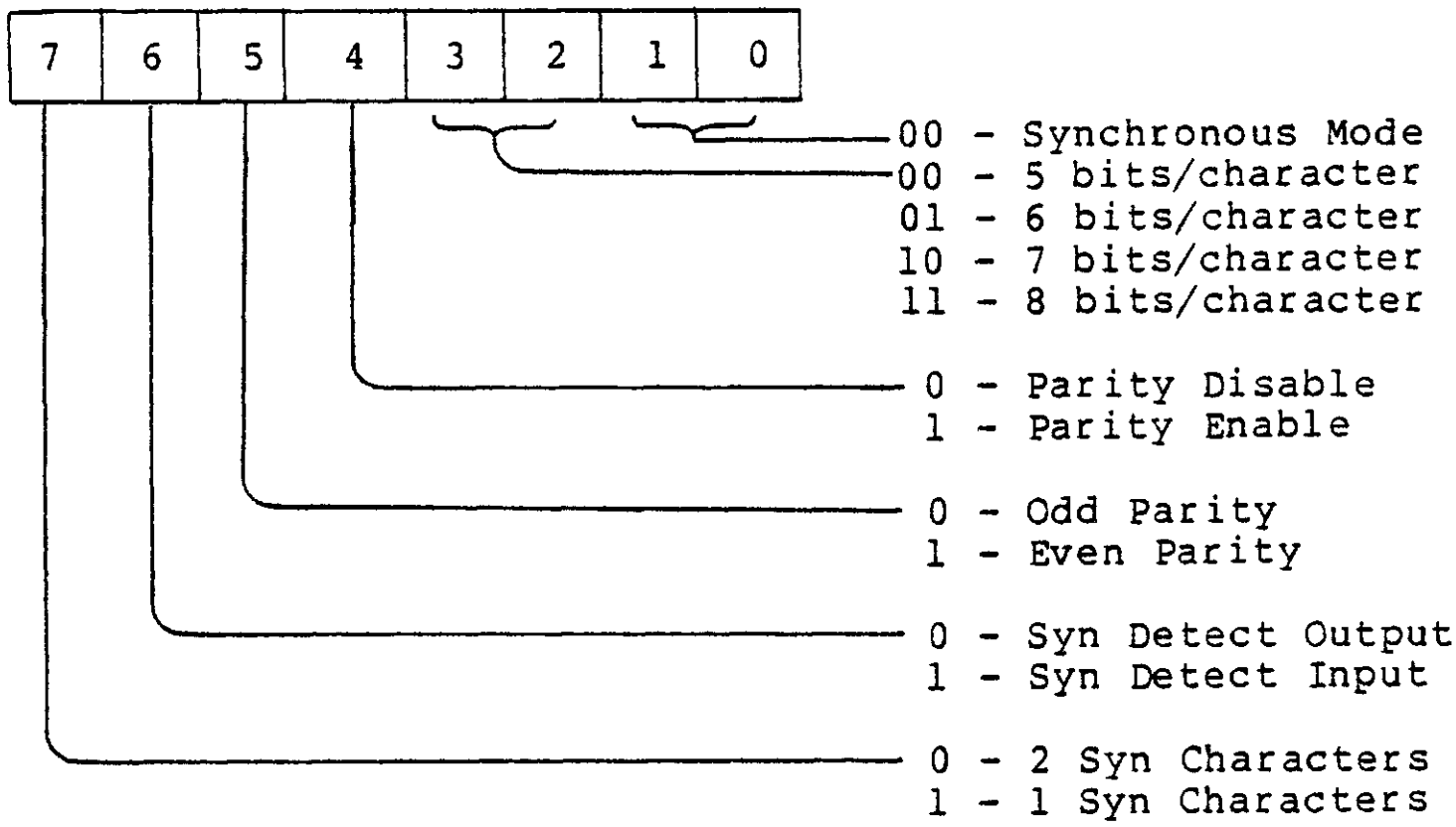


Figure 4-14. Synchronous Mode Control Codes

Mode Instruction Definition

The USART can operate in either asynchronous or synchronous communication modes. Understanding how the mode instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

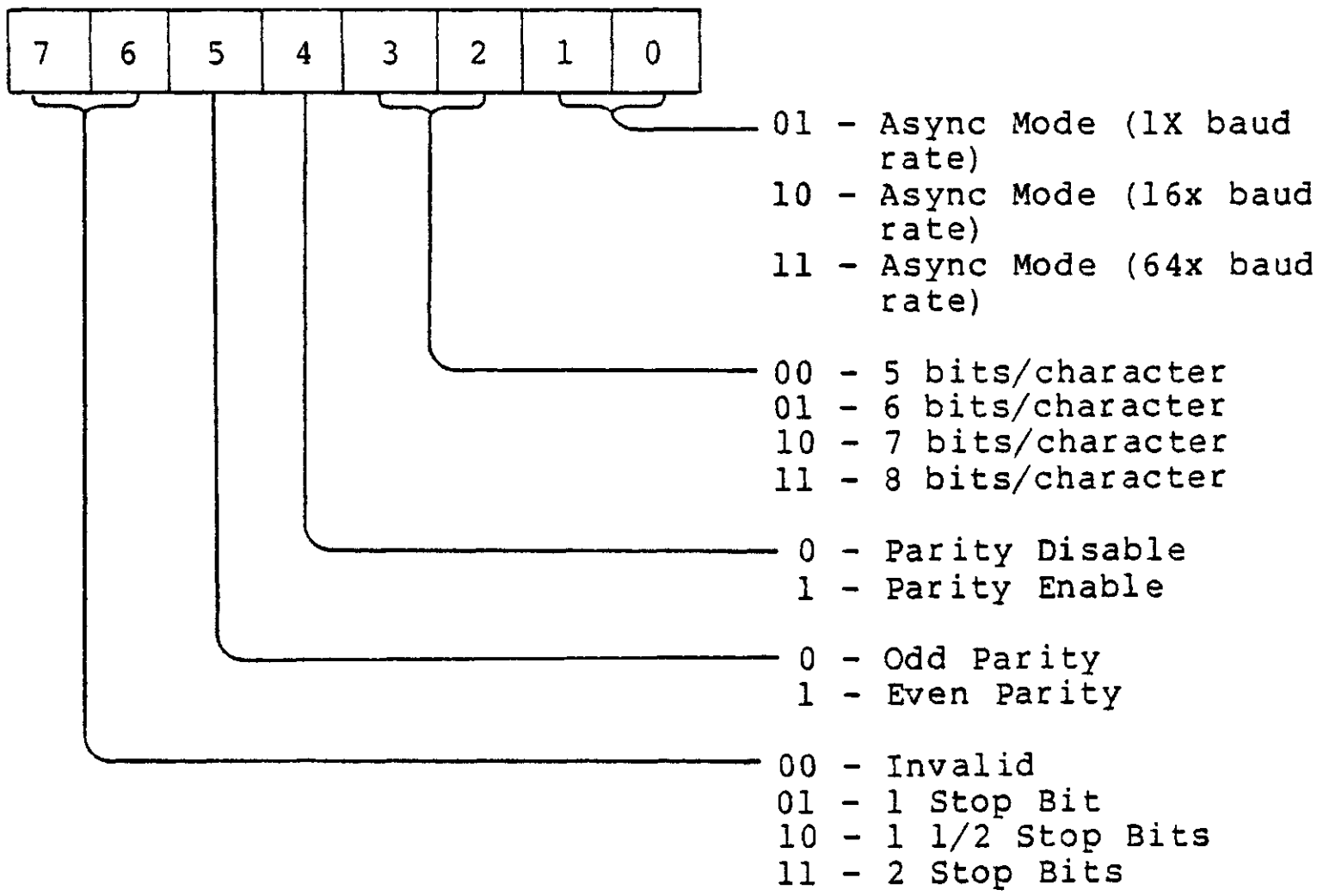


Figure 4-15. Asynchronous Mode Control Code

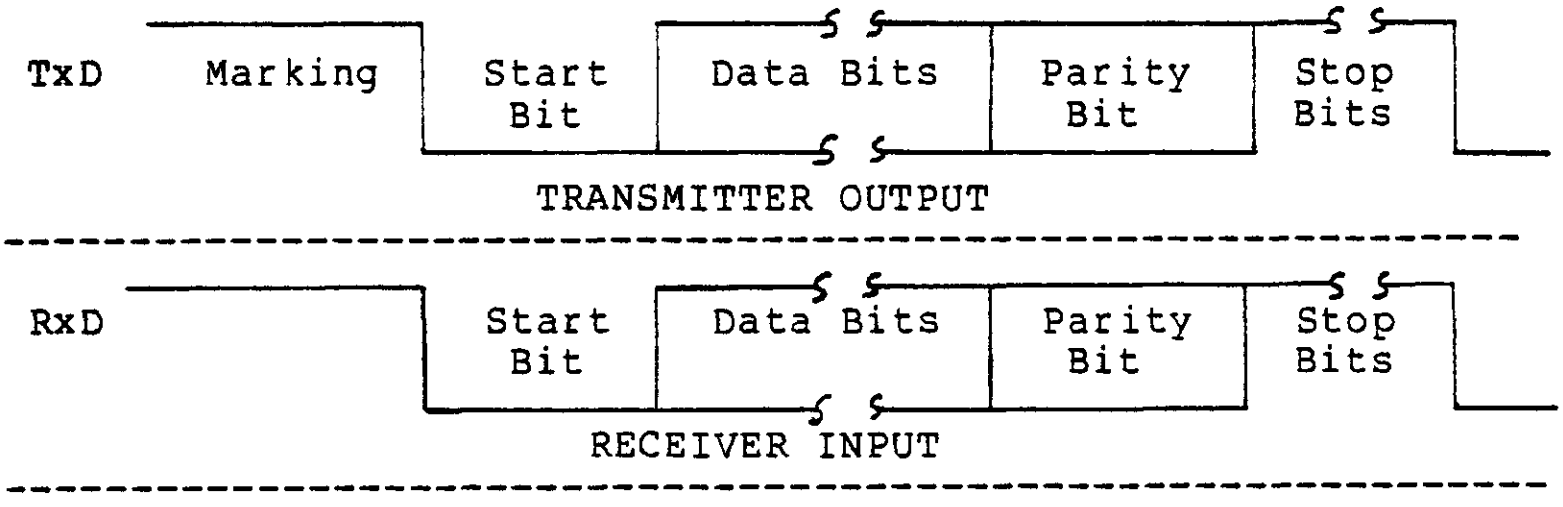
Asynchronous Mode

When a data character is written into the USART, it automatically adds a start bit (low level or "space") and the number of stop bits (high level or "mark") specified by the mode instruction. If parity has been enabled, an odd or even parity bit is inserted just before the stop bit(s), as specified by the mode instruction. Then, if CTS- and TxEN are active, the character is transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of TxC- at TxC-, TxC/16- or TxC-/64, as defined by the mode instruction.

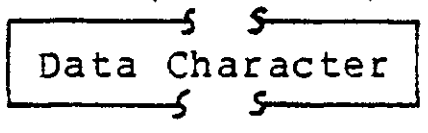
If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the start bit of the next character provided by the processor. TxD may be forced to send a break (continuously low) by setting the correct bit in the command instruction.

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a start bit and a new character. The start bit is checked by testing for a "low" at its nominal center and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and stop bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of RxC-. If a high is not detected for the stop bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid stop bit, the input character is loaded into the parallel data bus buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the command instruction. Error flag conditions will not stop subsequent USART operation.

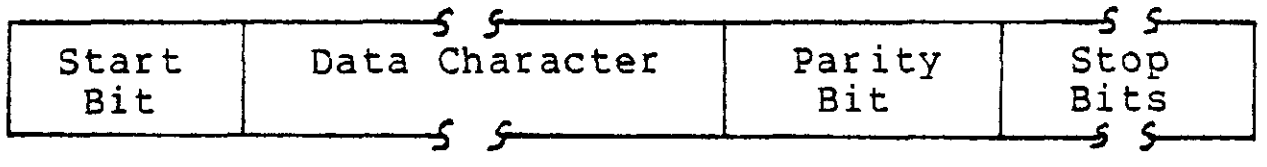
TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



CPU BYTE (5-8 Bits/Char)

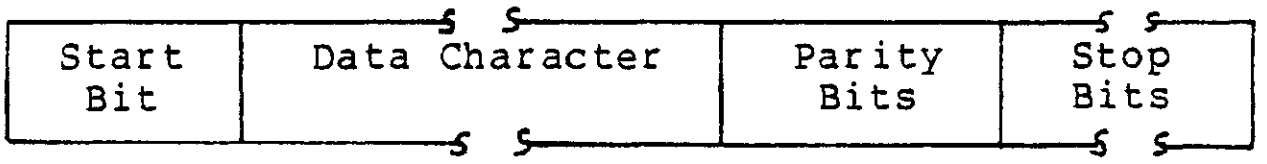


ASSEMBLED SERIAL DATA OUTPUT (TxD)

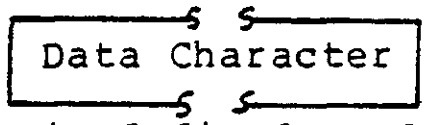


TRANSMISSION FORMAT

SERIAL DATA INPUT (RxD)



CPU BYTE (5-8 bits/char)*



* If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero"

RECEIVE FORMAT

Synchronous Transmission

As in asynchronous transmission, the TxD output remains "high" (marking) until the uPD8251 receives the first character from the processor which is usually a sync character. After a command instruction has set TxEN and after clear to send (CTS-) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of TxC- and the same rate as TxC-.

Once transmission has started, synchonronus mode format requires that the serial data stream at TxD continue at the TxC- rate or sync will be lost. If a data character is not provided by the processor before the uPD8251 transmitter buffer becomes empty, the sync character(s) loaded directly following the mode instruction will be automatically inserted in the TxD data stream. The sync character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the USART becomes empty, and must send the sync character(s), the TxEMPTY output is raised to signal the processor that the transmitter buffer is empty and sync characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

Synchronous Receive

In synchronous receive, character synchronization can be either external or internal. If the internal sync mode has been selected, and the enable hunt (EH) bit has been set by a command instruction, the receiver goes into the hunt mode.

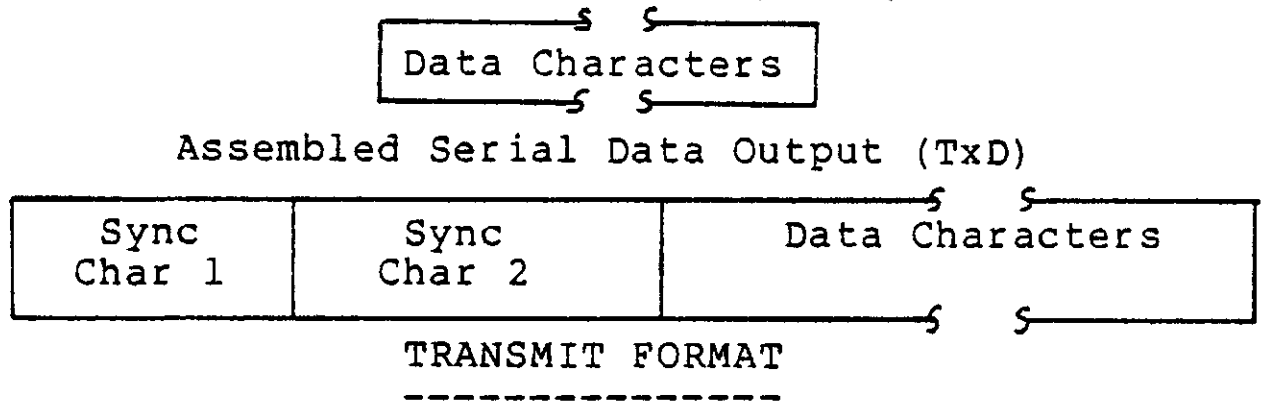
Incoming data on the RxD input is sampled on the rising edge of RxC-, and the receiver buffer is compared with the first sync character after each bit has been loaded until a match is found. If two sync characters have been programmed, the next received character is also compared. When the sync character(s) programmed have been detected, the USART leaves the hunt mode and is in character synchronization. At this time, the syndet (output) is set high. Syndet is automatically reset by a status read.

If external sync has been specified in the mode instruction, a "one" applied to the syndet (input) for at least one RxC- cycle will synchronize the USART.

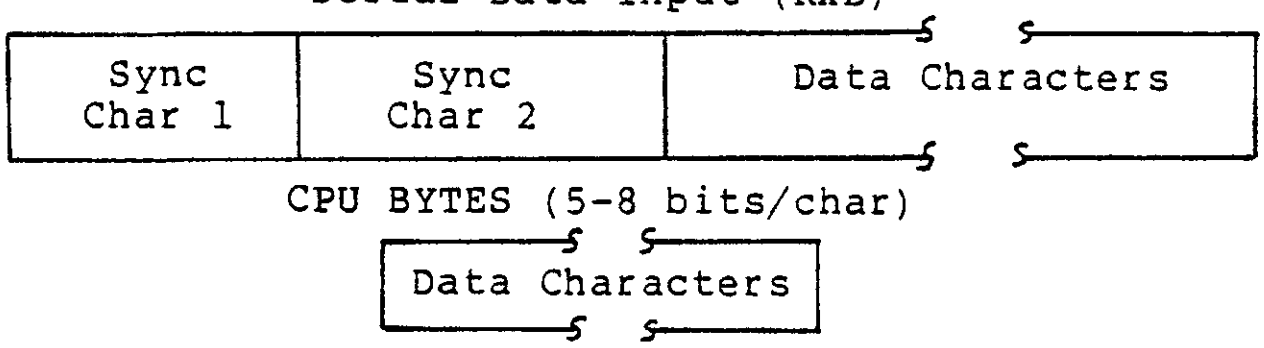
Parity and overrun errors are treated the same in the synchronous as in the asynchronous mode. Framing errors do not apply in the synchronous format.

The processor may command the receiver to enter the hunt mode with a command instruction which sets enable hunt (EH) if synchronization is lost.

TRANSMIT/RECEIVER FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Command Words

Command words are used to initiate specific functions within the USART, such as, "reset all error flags" or "start searching for sync". Consequently, command words may be issued by the microprocessor to the USART at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

A reset operation (internal via CMD IR or external via the reset input) will cause the USART to interpret the next "control write", which must immediately follow the reset, as a mode instruction. Following the mode instruction, a command word, of the format shown in Figure 4-16, is issued

to the USART.

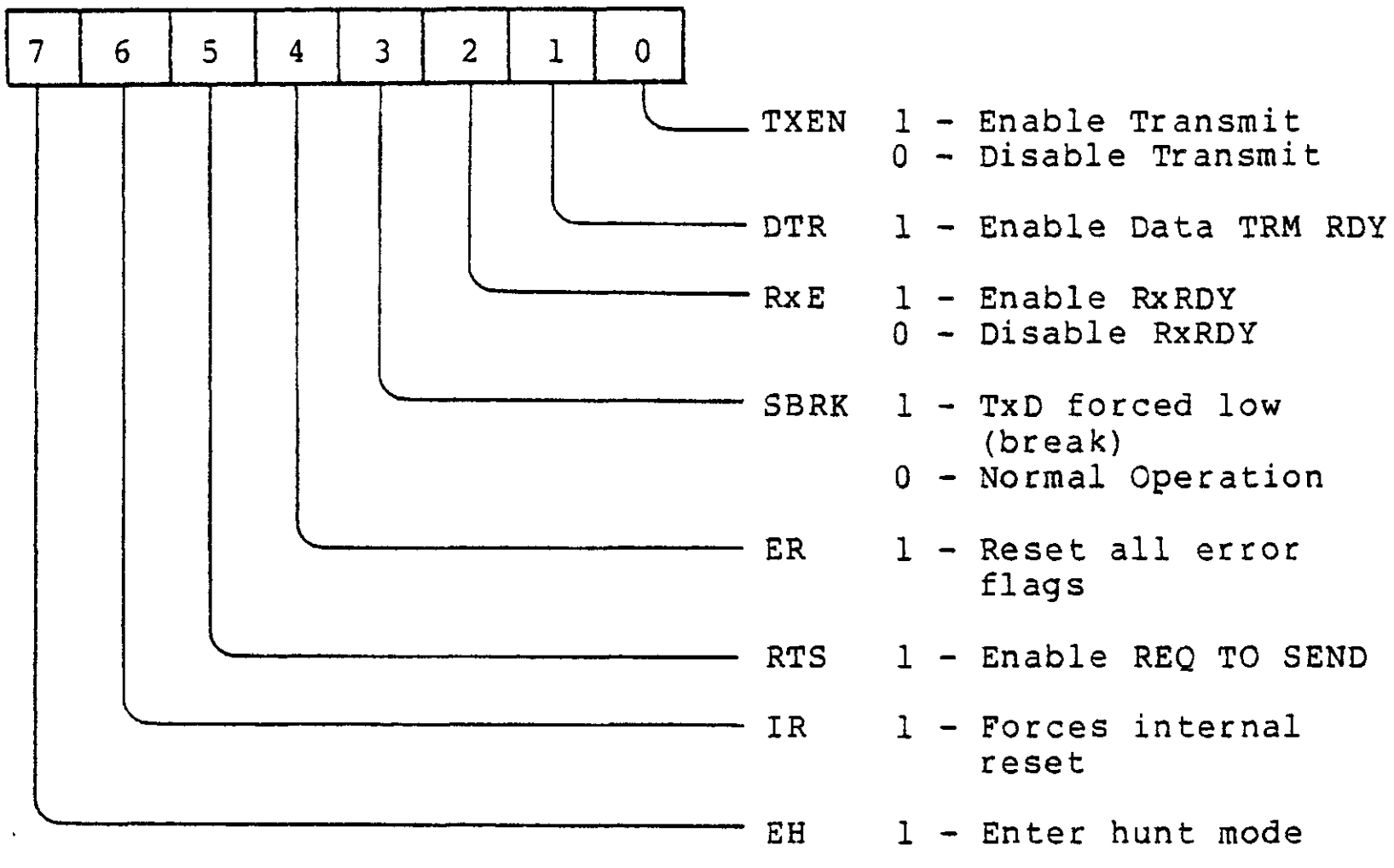


Figure 4-16. USART Control Command

Bit 0 of the command word is the transmit enable bit (TxEN). Data transmission from the USART cannot take place unless TxEN is set in the command register. Figure 5 defines the way in which TxEN, TxE, and TxRDY combine to control transmitter operations.

Bit 1 is the data terminal ready (DTR) bit. When the DTR command bit is set, the DTR- output connection is active (low). DTR is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the receiver enable command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the receive character buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and

transferred to the receiver character buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

Table 4-2. Transmitter Section Operation

TxEN	TxE	TxRDY	
1	1	1	Transmit output register and transmit character buffer empty. TxD continues to mark if USART is in the asynchronous mode. TxD will send sync pattern if USART is in the synchronous mode. Data can be entered into buffer.
1	0	1	Transmit output register is shifting a character. Transmit character buffer is available to receive a new byte from the processor.
1	1	0	Transmit register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit register is currently sending and an additional character is stored in the transmit character buffer for transmission.
0	X	X	Transmitter is disabled.

Bit 3 is the send break command bit (SBRK). When SBRK is set, the transmitter ouput (TxD) is interrupted and a continuous binary "0" level (spacing), is applied to the TxD output signal. The break will continue until a subsequent command word is sent to the USART to remove SBRK.

Bit 4 is the error reset bit (ER). When a command word is

transmitted with the ER bit set, all three error flags in the status register are reset. Error reset occurs when the command word is loaded into the USART. No latch is provided in the command register to save the ER command bit.

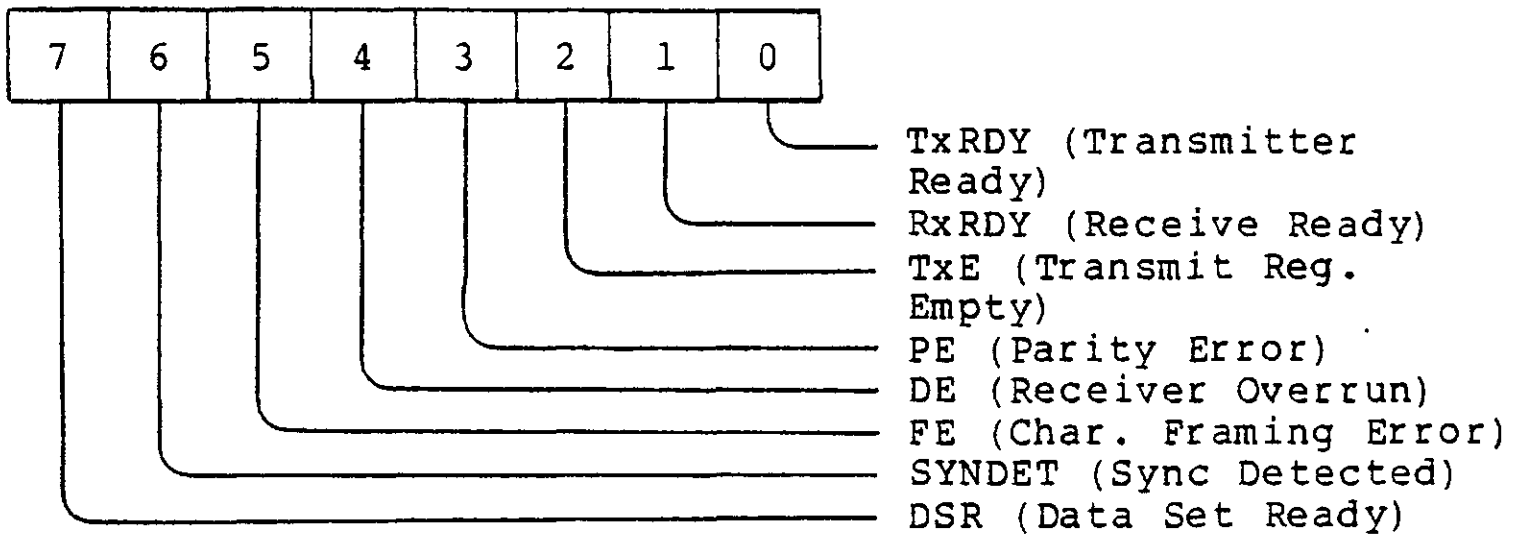
Bit 5, the request to send command bit (RTS), sets a latch to reflect the RTS signal level. The output of this latch is created independently of other signals in the USART. As a result, data transfers may be made by the microprocessor to the transmit register, and data may be actively transmitted to the communication line through TxD regardless of the status of RTS.

Bit 6, the internal reset (IR), causes the USART to return to the idle mode. All functions within the USART cease, and no new operation can be resumed until the circuit is reinitiallized. If the operating mode is to be altered during the execution of a microprocessor program, the USART must first be reset. Either the external reset connection can be activated, or the internal reset command can be sent to the USART. Internal reset is a momentary function performed only when the command is used.

Bit 7 is the enter hunt command bit (EH). The enter hunt mode command is only effective for the USART when it is operating in the synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "enter hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent command word is sent, when the IR command is sent to the USART, or when sync characters are recognized.

Status Read Format

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The USART has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the C/D- input "high" to obtain device status information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both polled and interrupt driven environments.



TxRDY signals the processor that the transmit character buffer is empty and that the USART can accept a new character for transmission.

RxRDY signals the processor that a completed character is holding in the receive character buffer register for transfer to the processor.

TxE signals the processor that the transmit register is empty.

PE is the parity error signal indicating to the CPU that the character stored in the receive character buffer was received with an incorrect number of binary "1" bits. The PE flag is cleared by setting the ER bit in a subsequent command instruction. PE being set does not inhibit USART operation.

OE is the receiver overrun error. OE is set whenever a byte stored in the receiver character register is overwritten with a new byte before being transferred to the processor. The OE flag is cleared by setting the ER bit in a subsequent command instruction. OE being set does not inhibit USART operation.

FE is the character framing error which indicates that the asynchronous mode byte stored in the receiver character buffer was received with an incorrect character bit format (stop bit), as specified by the current mode. The FE flag is cleared by setting the ER bit in a subsequent command instruction. FE being set does not inhibit USART operation.

4.3 DYNAMIC MEMORY MODULE

A Dynamic Memory Module is provided for the Development System for storage of user programs and the operating system. The module utilizes 16K Dynamic RAM components to provide a maximum storage capacity of 60K bytes. Memory addressing is controlled by a combination of the Address Bus (A0-A15) bits and Page and Card Select signals from the Central Processor Module, previously described. The relationships are illustrated in Figure 4-2.

4.3.1 Control Logic (Sheet 1)

The Control Logic receives Memory Request (MRQ), Memory Read (MRD), Write (WR), Memory Inhibit and Refresh (RFSH) signals from the Central Processor Module and converts them to timing sequences for memory access.

Memory access is triggered by MRQ (active low). Once an access is initiated the following events must occur:

- For refresh cycles MRQ (low) and RFSH (low) force all Row Address Selects (RAS0-RAS3) to their active low state and generates CONTROL (low) and ICAS (low) for the refresh cycle. The data buffers are switched to prevent gating of any data onto the system data bus.
- For memory read or write cycles MRQ (active low) triggers the access and enables the RAS address to be gated to the memory array (CONTROL going low) followed by the delayed RAS signal ICAS (active low), which enables gating of the CAS address to the memory array.

The MEMORY INHIBIT signal is provided by the Central Processor Module when accessing the on-board 3K PROM or 1K static RAM to disable the data buffers of the Dynamic Memory Module from placing data onto the system data bus.

4.3.2 Data Buffers (Sheet 2)

A pair of 4-bit bidirectional bus drivers (A3 and A6) serve to interface the Dynamic RAM Array to the system data bus. These are always enabled (pin 1 grounded) and are solely controlled by OUTPUT ENABLE (active low). The OUTPUT ENABLE signal originates from the control logic (Sheet 1) and selects whether data is to be received from or placed onto the system data bus. For memory write (MRQ and WR low) operations, the buffers receive data from the system data bus, this is also true for refresh operations (MRQ and MRD low) and data from the selected address is gated onto the system data bus.

4.3.3 Row Address Select (Sheet 1)

The Row Address Select logic is composed of a muliplexer (A11) and two additional stages of gating to differentiate between normal memory access and refresh accesses. During refresh operations (MRQ and RFSH low) all RAS signals (RAS0-RAS3) are forced to their active low state. Normal memory accesses involve generation of selected RAS signals by gating the outputs of multiplexer A11 with Memory Request (MRQ) active low. The jumpers for RAS address selection are shown below.

FOR 16K COMPONENTS (60K): L-M, N-O

4.3.4 Address Multiplex (Sheet 2)

The Address Multiplex function (A7 and A8) provides control of the Z80-CPU addresses, which are gated to the Dynamic Memory Array during the RAS and CAS cycles of each memory access. Enables to the multiplexers are grounded, thereby constantly providing an enable for either the A or B inputs to be gated to the memory array. When in the idle state (CONTROL signal high), the B-inputs A0-A4, A12 and A13 are gated to the array. During a RAS cycle (Control active low), the A-inputs are gated as long as it is not a refresh (RFSH low) cycle. The jumpering for the proper address selection is shown below.

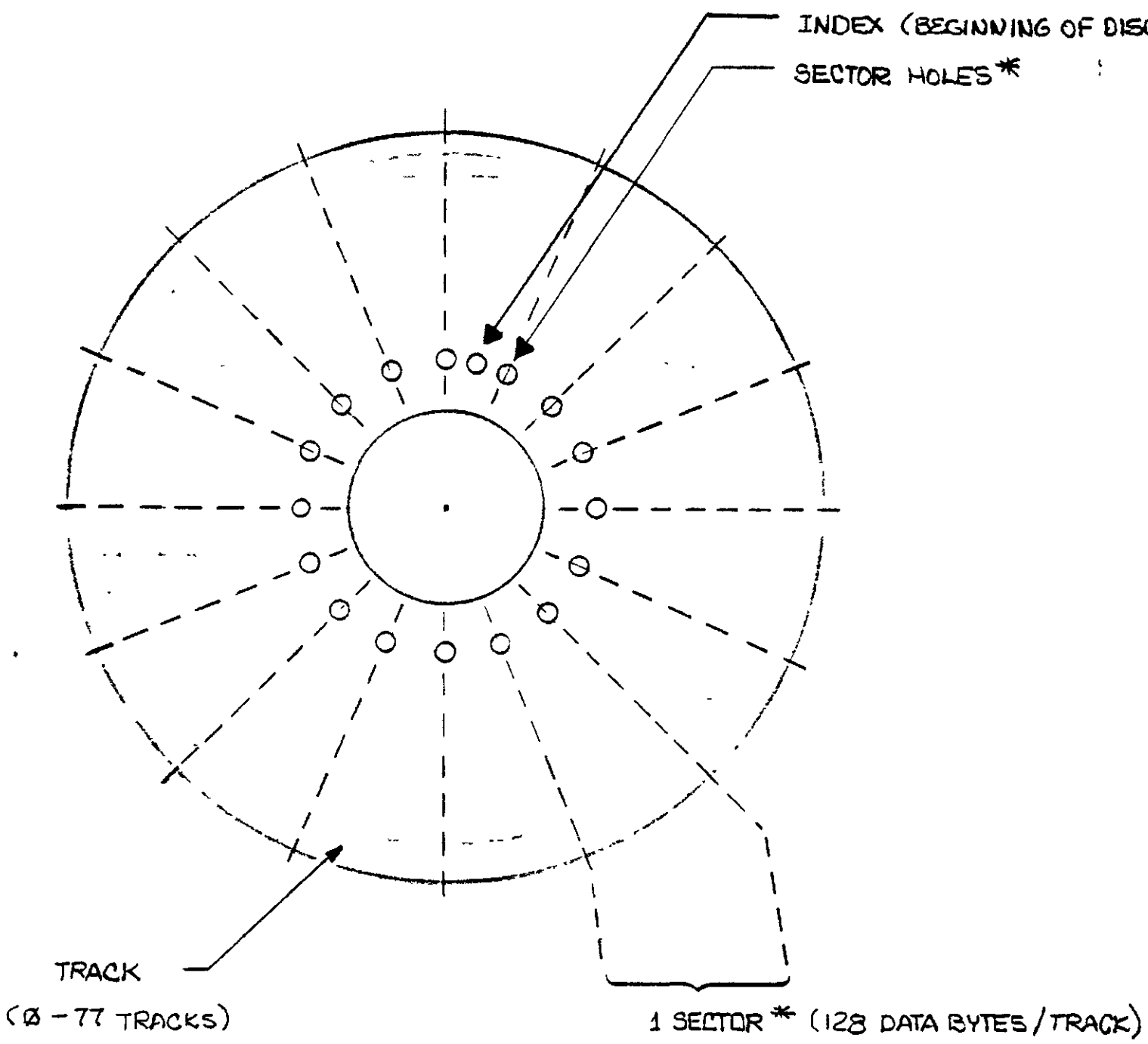
FOR 16K COMPONENTS (60K): B-C, E-F, H-I

4.3.5 Dynamic Memory Array (Sheet 4)

The Dynamic Memory Array is composed of 32, 16K X 1 bit Dynamic Random Access Memory components. These are arranged in four rows, each containing 16,384 bytes of storage. This scheme allows a basic configuration of 60K.

4.4 FLOPPY DISC CONTROLLER MODULE

The Floppy Disc Controller Module provides an interface between the Development System and two single-density, single-sided, hard-sectored floppy disk drives, e.g., Shugart Model 801 Disc Drive. Interface and timing functions are provided by the controller, but the intelligence for the controller is imbedded in the 3K PROM Debug firmware. A block diagram of the controller is provided in Figure 4-9, which may be used as a reference.



* ONLY 16 SECTORS ARE SHOWN FOR CLARITY, THE ACTUAL DISKETTE USED CONTAINS 32 SECTORS.

Figure 4-3 DISC RECORDING FORMAT

4.4.1 Diskette Format

In order to understand the operations of disk units, the reader should know how data is stored on the surface of the diskettes. Each hard sectored diskette contains 32 holes or sector marks which identify the beginning of each sector on the diskette. The beginning of the diskette itself contains a single hole called an "index mark," which serves as a reference point for all succeeding sector marks, (see Figure 4-3).

The index and sector marks serve to synchronize the controller rotational movement of the diskette, but a means must be provided to locate data stored at various parts on the surface of the diskette from the center to the outer limits. Data is stored in concentric locations called "tracks" beginning from the outer-most edge (Track 00) to the inner-most edge (Track 76). Movement from one track to the next is controlled by a stepper motor within the disk drive which controls the read/write head positioning. A pulse applied to the drive causes the head to be moved one track position. The direction of movement (inware/outward) must also be provided to the drive by the controller.

4.4.2 Data Format

The format of the data written on a selected track between a sector mark and the next sector mark is controlled by the driver program contained in the 3K PROM Debug firmware. The basic format for the data written in each sector is illustrated below.

▨ - SHADED AREAS ARE ESTABLISHED BY THE FIRMWARE AND CONTROLLER

- PREAMBLE - 16 bytes of all zeroes; used to synchronize the controller for the following data fields.

- SECTOR ADDRESS - single byte having the most significent bit equal to a "1" for a start bit, followed by two zeroes The last five bits contain the sector address.

  100 xxxxx

  SECTOR ADDRESS (0-1FH)

- TRACK ADDRESS - single byte containing the track address in the least significant seven bits AD-A6.

  0 xxxxxxx

  TRACK ADDRESS (0-7FH)

- DATA BLOCK - 128 bytes of data stored by the user; may be in binary or ASCII form.

- LINKAGE - provides two pointers, each composed of two bytes, which point to the preceding and succeeding sector of data in the file. The pointers are composed of the sector and track addresses previously described.

- CRC - the Cyclic Redundancy Check word (2 bytes) is the output of the CRC generator contained in the controller. It is a check sum for the sector and track addresses, data block and linkage words.

- POSTAMBLE - is composed of a series of zeroes written after the CRC word to provide a protection gap after the valid data fields of the sector.

4.4.3 RECORDING FORMAT

The format of the data recorded on the diskette is a total function of the System resident firmware. Data is recorded on the diskette using frequency modulation as the recording mode; i.e., each data bit recorded on the diskette has an associated clock bit recorded with it. This is referred to as FM. Data written on and read back from the diskette takes the form as shown in Figure 4-4. The binary data pattern shown represents a 101.

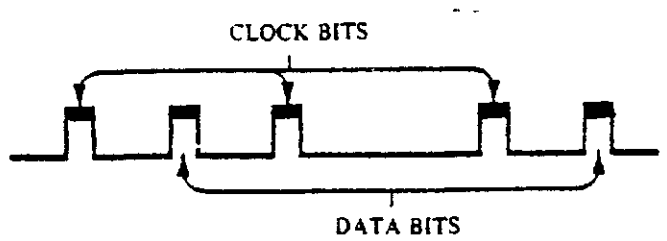


Figure 4-4
DATA PATTERN

a. BIT CELL - As shown in Figure 4-5, the clock bits and data bits (if present) are interleaved. By definition, a bit cell is the period between the leading edge of one clock bit and the leading edge of the next clock bit.

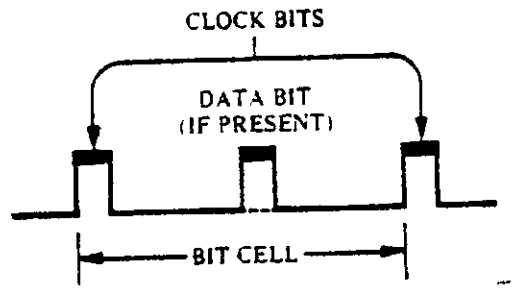


Figure 4-5
DATA PATTERN

b. BYTE - A Byte, when referring to serial data (being written onto or read from the disk drive) is defined as 8 consecutive bit cells. The most significant bit cell is defined as bit cell 0, and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disk drive first and bit cell 7 is being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first, and the least significant byte is transferred last.

When data is read back from the drive, bit cell 0 of each byte will be transferred first and bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

Figure 4-6 illustrates the relationship of the bits within a byte, and Figure 4-7 illustrates the relationship of the bytes for read and write data.

4.4.4 Floppy Disk Controller Interfaces

As previously described the Floppy Disk Controller serves to interface the Development System to dual floppy disk drives. This operation is represented in block form by Figure 4-8. The controller must provide two interfaces: (1) for interface to the Development System, and (2) for the disk units. Each of these interfaces will be briefly described in the following text.

DEVELOPMENT SYSTEM INTERFACE:

Interface to the Development System is fairly simple. The three system busses (address, data and control) are employed by the controller in a simplified form.

Data Bus - interfaces are eight bits (D0-D7) of the system data bus to the controller for command, status, and data exchange.

Address Bus - does not directly interface to the controller. Because the controller is an I/O device and does not posses DMA (direct memory access) capabilities, it may be selected by decoding the lower Address Bus lines (A0-A7) of the Z80-CPU during I/O Request operations. This decoding is performed by the MONITOR Module and results in the following select signals which are applied to the controller.

- DISK CONT A (Port F9H) used for loading command information into the controller.

- DISK CONT B (Port FAH) also used for loading command information into the controller and retrieving status.

- DISK DATA (Port F8) is used to transfer data to or from the on-board data buffer.

Control Bus - a minimal number of control signals are required because the controller only utilizes the I/O controls of the Z80-CPU. The IORQ signal along with RD for I/O read operations

Figure 4-6 illustrates the relationship of the bits within a byte, and Figure 4-7 illustrates the relationship of the bytes for read and write data.

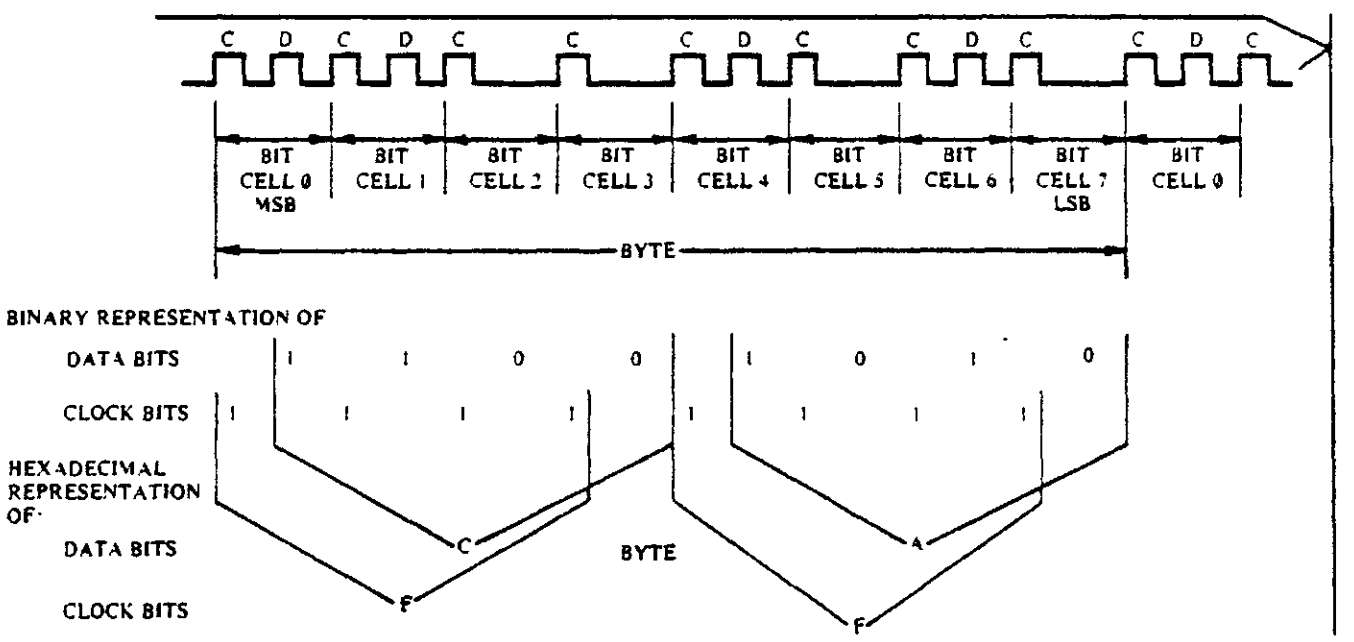


Figure 4-6
BITS WITHIN A BYTE

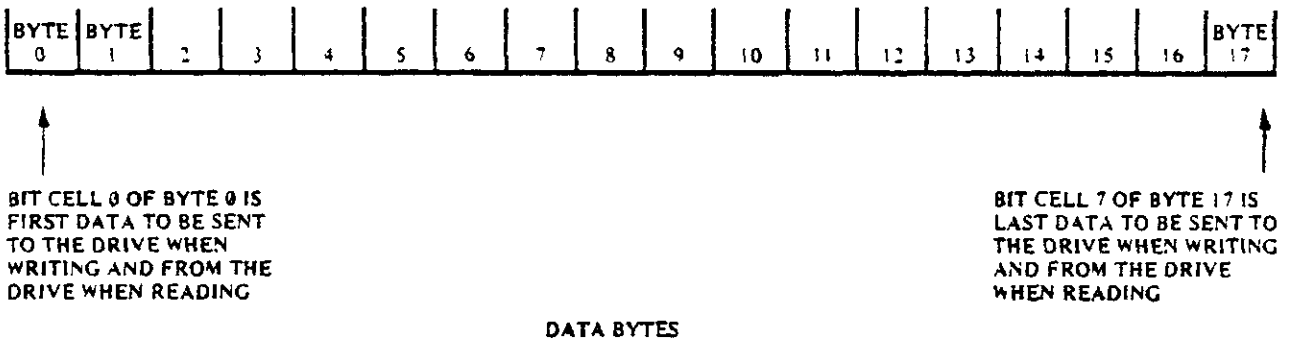


Figure 4-7
DATA BYTE RELATIONSHIPS

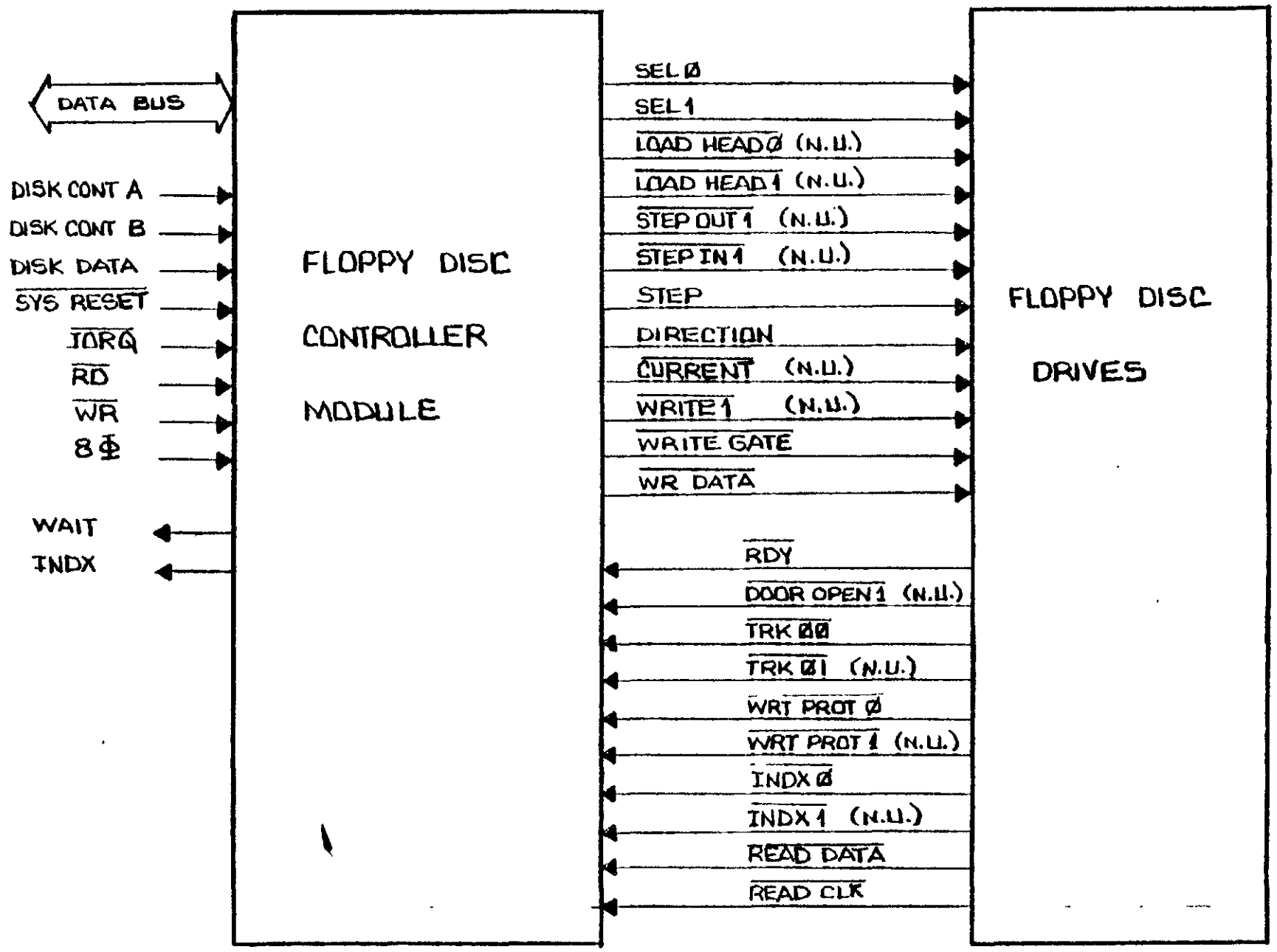


Figure 4-8 DISC INTERFACE DIAGRAM

or WR for I/O write operations is used to control data movement between the system data bus and the controller. The PHI clock from the Central Processor Module is used by the controller for all timing. Also provided is the SYS RESET signal from the CPM. Two outputs are provided from the controller to the system: (1) WAIT is used to synchronize data transfer from the controller to the Z80-CPU; (2) INDX provides index and sector mark recognition which is used to clock the CTC located on the SCON Module.

FLOPPY DISC DRIVE INTERFACE:

Many signals are provided for the floppy disk interface in order to faciliate the interface of many types of floppy disk drives. However, when utilizing the Shugart SA801 Disc Drives a minimum number of signals may be employed due to the flexability of the disk units.

SEL0/SEL1 (SELECT) - signals are used by the drive(s) to determine when it has been selected for an operation by the controller. Under normal operation, the Drive Select line will load the R/W head, apply power to the stepper motor, enable the input lines, activate the output lines, and light the ACTIVITY LED on the front of the drive.

LOAD HEAD 0/1 - signals are not used by the interface, but are optionally provided to enable the controller to control the loading of the R/W heads in the drive(s).

STEP OUT/STEP IN - signals are also not used by the interface, but are provided as independent controls to allow two signals for stepper motor control. The drives presently employ the use of the STEP signal and DIRECTION signal for this function.

STEP - signal (active high) in conjunction with the DIRECTION signal being high causes the head to move one track away from the center of the disk.

DIRECTION - signal (when high) selects movement away from the center of the disk; conversely, when low, selects movement toward the center of the disk.

CURRENT - provides an independent signal for applying DC power to the Stepper Motor of the disk drive(s). This is not used by the SA801 Disc Drives.

WRITE GATE - provides a common control to the disk drives to write data onto the disk surface. When disabled (logic high) the heads are enabled for read operations.

WRITE 1 - provides an optional signal which may be used to generate the WRITE GATE function for drive 1 while WRITE GATE itself would perform the function for drive 0.

WR DATA - this interface line provides the data to be written on the disk and is enabled by the WRITE GATE line being active (low). Each transition from a logical one level to a logical zero level will cause the current through the Read/Write head to be reversed, thereby writing a data bit.

RDY (Ready) - this signal indicates that a disk has been inserted, the door closed, and the two index holes sensed.

DOOR OPEN 1 - provides an optional status bit to indicate that the drive has gone from a READY state to a non-ready state (door open).

TRK 00/01 - provides a signal from the drive(s) which indicates that the drive's R/W head is positioned at track zero (outermost track) and the access circuitry is driving current through phase one of the stepper motor. Only TRK00 is required by both SA801 Disc Drives and the controller, due to the drive selection technique employed.

WRT PROT 0/1 - provides a status indicating the diskette inserted into the drive has a write-protection tab installed. Only a single line is required, and is shared by both SA801 Disc Drives.

INDX0/1 - this signal provides an indication of the beginning of the track once every revolution of the diskette (166.67 ms). Only INDX0 is used, and it is shared by both drives.

READ DATA - this line provides raw read data (data and clock) as it is read by the R/W head. Optionally, it can contain only the read data if the drive contains data/clock separation logic.

READ CLK - provides the read clocks after they have been internally separated from the data/clock stream by the drive's internal data separation logic.

4.4.5 Floppy Controller - Detailed Operation

The detailed operation of the Floppy Disc Controller Module will be provided using Figure 4-9 as a reference. This illustration functionally illustrates the controller and provides specific references to logic Sheet numbers for the Floppy Disc Controller.

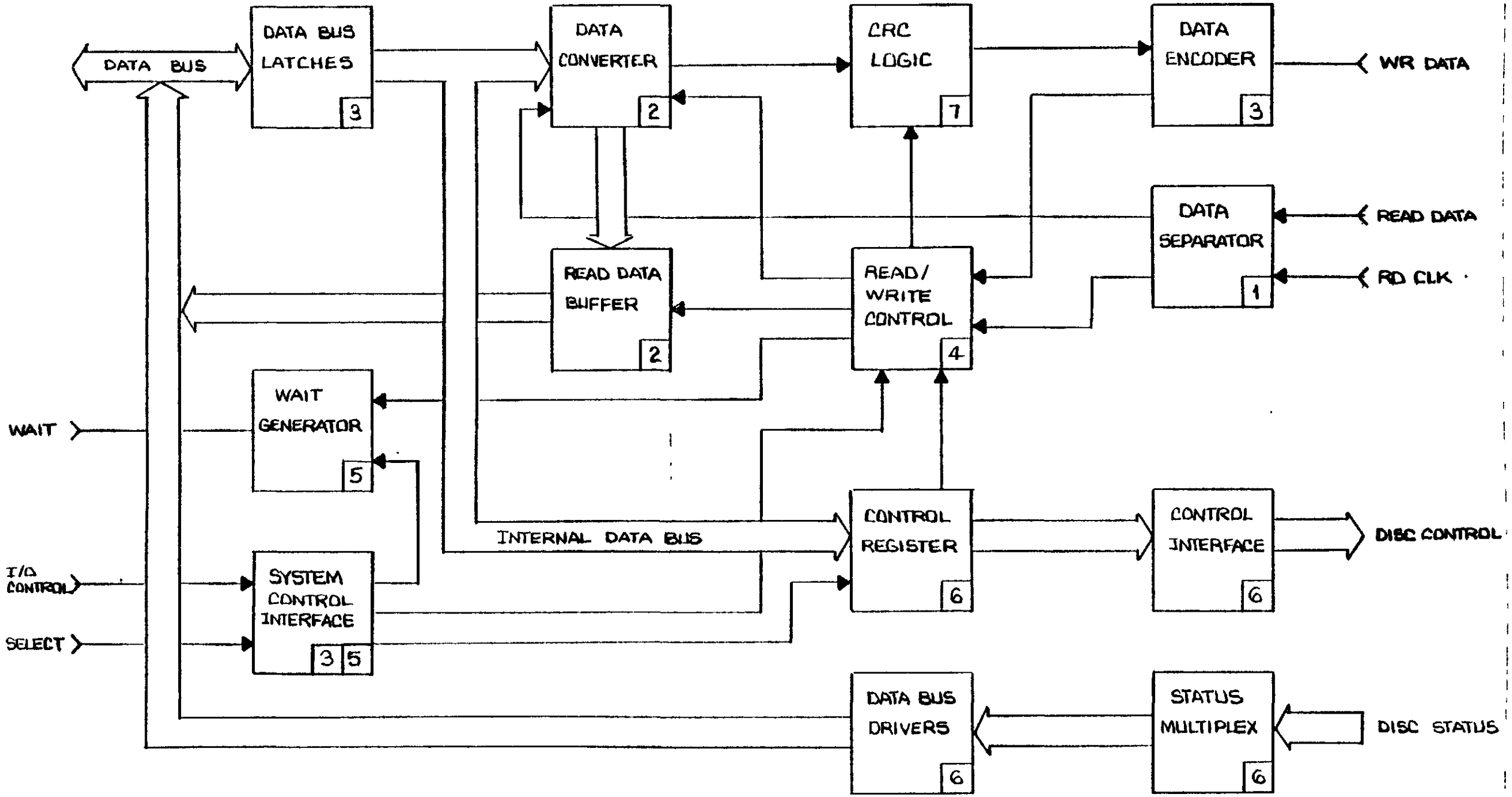


Figure 4-9 FLOPPY DISC CONTROLLER - BLOCK DIAGRAM

4.4.5.1 Data Bus Latches (Sheet 3)

All data is destined for the controller (I/O Ports F8, F9 or FA) must pass through the Data Bus Latches (A30 and A33). When any of the three I/O Port Addresses assigned to the controller are selected during an I/O (Port) Write operation (IOWR active low), the contents of the system data bus is latched by the Data Bus Latches. The outputs of the latches are routed to the Data Converter (A23 and A24) on Sheet 2, as well as to the Control Registers (A22, A25 and A26) on Sheet 6.

4.4.5.2 Data Converter (Sheet 2)

The Data Converter (A23 and A24) provides both parallel-to-serial data conversion during write operations, and serial-to-parallel data conversion during read operations.

During Write operations the converter is parallel loaded with the contents of the Data Bus Latches (Sheet 3) as a result of TX LOAD (active high) and the leading edge of the SHIFT CLK (active low). When the TX LOAD signal goes false (logic 0) the converter functions as a shift register, performing a shift right operation with each occurrance of the SHIFT CLK. The serial data output (TxK), most significant bit of the converter is routed to the CRC Logic for exposure to the CRC generator.

During Read operations the output of the Data Separator (Sheet 1) RxDATA is applied to the serial data input of the Data Converter. The occurrance of each SHIFT CLK will serially shift the RxData into the converter. Once eight bits have been loaded into the converter the contents of the converter are quickly transferred to the Read Data Buffer (Sheet 2) so that the next eight bits may be clocked in without disruption of the serial data stream.

4.4.5.3 Read Data Buffer (Sheet 2)

The Read Data Buffer (A31 and A32) provides a temporary storage for data during read operations from the disk. This temporary storage is required to prevent disruption of the serial data stream being shifted into the Data Converter. Once eight bits have been assembled by the converter they are transferred in parallel to the Read Data Buffer by the RxBUFF LOAD signal (active low) so that the serial data timing into the converter is not disrupted.

The 3K PROM firmware will transfer the data from the Read Data Buffer by executing an I/O Port Read from Port F8H which

results in the generation of READ CHAR (active low). This action enables the outputs of the Read Data Buffer to go active, transferring the contents to the system data bus (D0-D7).

4.4.5.4 CRC Logic (Sheet 7)

The CRC Logic provides the CRC Generation and Check function for data being serially written or read from the disk. It also performs a data multiplex function in determining what type of data is to be gated to the Data Encoder during write operations.

An F9401 CRC Generator/Checker (AZ) provides the generation and checking of the serial data stream. During write operations, indicated by WRITE ENABLE (high) and WR MODE+ (high), the output of the Data Converter (TxD) is gated to the generator via A15 and is clocked into the CRC Generator/Checker by the SHIFT CLK (low). The generator performs a division on the incoming data stream using a CRC-16 polynomial. When data is being entered, the CRC Enable flip-flop A10 (Sheet 7) is reset causing the CWE (check Word Enable) input to the generator to be disabled. Once the data has been completely transferred (128 bytes) the 3K PROM firmware will set the CRC Enable flip-flop activating the CWE input to the generator. This condition will enable the 16-bit cyclic redundency check character to be appended to the data stream to the disk.

During read operations, the RCV DATA signal from the Data Converter (Sheet 2) is gated to the generator by RX MODE+ (high). The data is once again shifted into the generator by the SHIFT CLK (low) signal, but the generator only functions as a monitor to sample the data stream. Once the last bit of the incoming data stream has been received, this would logically be the last bit of the 16-bit CRC received, the CRC ERR (active low) may be sampled to see if an error has occurred. This signal will remain in a fixed state until another SHIFT CLK is applied or until the generator is reset by RX MODE + or WR MODE + going false (low).

4.4.5.5 Data Encoder (Sheet 3)

The Write Data Encoder (A4, A18, A19, A12, A20 and A27) serves to integrate the write clock with the data being transferred to the disk drive, to maintain the double frequency recording format (reference Figure 4-4). The 8O clock from the Central Processor module is divided by eight to yield A (2.047 MHZ) which is applied to the Data Encoder which performs a divide by 2, 4 and 8 conversion. The divide by eight output (TX CLK) occurs at a 256KHZ rate and is applied to the Read/ Write Control logic (Sheet 4) to control data movement within the controller. The output WR DATA interfaces directly to the disk drive(s) as a composite clock and data signal.

4.4.5.6 Data Separator (Sheet 1)

The Data Separator shown on logic Sheet 1 serves to interface the READ DATA and RD CLK signals from the disk drive(s) to the controller. This board is designed to accomodate interface to drives which have no internal data separation logic or to those which do. For the Model SA801 Disc Drives the latter is the case so the READ DATA and RD CLK signals are present from the disk interface.

Four jumpers are provided on the board (A-D) to select internal or external data separation. The position of each jumper for internal or external data separation is shown below.

	A	B	C	D
INTERNAL	1-2	1-2	1-2	1-2
EXTERNAL	1-3	1-3	1-3	1-3

The logic is enabled to function only in read operations, RX MODE + (active high) and results in the generation of RX DATA which goes to the Data Converter (Sheet 2) and the Read/Write Control (Sheet 4). Also generated is RX CLK (active high) which is routed to the Read/Write Control logic to control data movement during read operations.

4.4.5.7 Read/Write Control (Sheet 4)

The logic shown on Sheet 4 serves to control the data transfer between the controller and the drive, the data movement within the controller and to synchronize the whole process with data transfers to or from the system data bus.

WRITE OPERATIONS:

The write operation is initiated by setting the WRITE latch in the Control Register (Sheet 6). This results in two signals: WR MODE (active low) and WR MODE + (active high), which are applied to the Read/Write Control logic on Sheet 4. The WR MODE + removes the reset from the Write Enable

generator (A6) and the WR MODE (low) prevents read clocks (RX CLK) from triggering the Shift Clock generator (A5 and A9). The WR MODE + enables the Shift Clock generator to function with each occurrance of the TX CLK. The WR MODE (active low) removes the set input from the Start Bit Detection logic (A10 and A11) and allows the bit counter (A11) to increment with each TX CLK. Once eight bits have been written the TX BUFF UNLOAD (active low) signal is inverted by A8 to provide TX LOAD (high) to enable the parallel loading of the Data Bus Latch outputs (Sheet 3) into the Data Converter (Sheet 2) so that the next character may be serially shifted to the disk.

READ OPERATIONS:

The read operation is initiated when WR MODE (active low) signal is false (high) enabling the RX CLK to trigger SHIFT CLK. The SHIFT CLK cannot increment the Bit Counter (A11) until the Start Bit Detect Flip-flop is set, signifying the first bit received of the sector address. By implementing this feature, only the actual data fields of the record being read will be transferred to the Z80-CPU and CRC Checking will not commence until the actual data is present. Once the data begins, the Bit Counter advances until eight bits have been serially shifted into the Data Converter (Sheet 2) as indicated by RX BUFF LOAD (active low). The RX BUFF LOAD (low) enables the outputs of the Data Converter (Sheet 2) where it may be transferred to the Z80-CPU by executing a Port Read to Port F8H. Data must be removed from the buffer prior to the reception of the next data character or it will be over written.

4.4.5.8 System Control Interface (Sheet 3)

The interface between the system and the controller is shown on logic Sheet 3 and Sheet 5. The Z80-CPU I/O Control signals, IORQ, RD and WR are decoded on Sheet 5 to form IORD and IOWR which are used on Sheet 3. The disk controller is assigned three I/O Port Addresses (F8, F9 and FA) each of which has a special purpose. A decode port address results in the generation of the following gating signals used to control data movement to or from the system data bus.

WR CONT 1	- Write to port FA - enables loading of Control Register B
WR CHAR	- Write to port F8 - enables loading of Data Bus Latches
READ CHAR	- Read to port FA - enables reading of Read Data Buffer
READ STATUS	- Read to port FA - enables reading of the Status Multiplex
WR CONT 2	- Write to port F9 - enables loading of Control Register A

4.4.5.9 Wait Generator (Sheet 5)

The Wait Generator is provided to help synchronize the data transfer between the system data bus and the controller. During Write operations it functions using TX BUFF UNLOAD and WR CHAR signals to prevent the Z80-CPU from transferring a character into the Data Bus Latches (Sheet 3) until the existing data being held in the latches is transferred to the Data Converter (Sheet 2).

During Read operations it functions using RX BUFF LOAD and READ CHAR signals to prevent the transfer of data from the Read Buffer (Sheet 2) until it has been loaded from the outputs of the Data Converter (Sheet 2).

4.4.5.10 Control Register (Sheet 6)

The Control Register is actually composed of three 4-bit registers (A22, A25 and A26) which are configured to form an eight bit register (A22 and A25) and a four bit register (A26). The intent is to provide an eight bit register to control those signals which are accessed or changed most frequently and a 4-bit register which is seldom accessed. These registers shall be referenced as Control Register A (8-bits) and Control Register B (4-bits). The various bits of the registers and their respective I/O Port Addresses are shown in Figure 4-10.

4.4.5.11 Control Interface (Sheet 6)

The Control signal interface to the disk drives is shown on logic Sheet 6. The interface circuitry (A27, A34 and A35) decodes the outputs of the Control Registers and inverts the signals to drive the disk drive interface. Many signals are presented to the interface which are not used by the Model SA801 Disc Drive, reference paragraph 4.4.4.

4.4.5.12 Status Multiplex (Sheet 6)

The Status Multiplex consists of a 2-input 4-bit multiplexer (A37) and a bus driver (A28). Eight signals are provided into the multiplexer of which four may be sampled at any one time. The selection of which four bits are examined is determined by the SEL 1 (bit 6) signal from Control Register B. The outputs of the multiplexer are routed to A28 along with CRC ERR (active low) from the CRC Checker (Sheet 7). Gating of the status onto the system data bus is controlled by the READ STATUS (low) signal from the System Control Interface (Sheet 5). The status bits are shown in Figure 4-11. Like the Control Interface signals there are many status signals some of which are not used, reference paragraph 4.4.4.

STATUS FROM PORT FAH

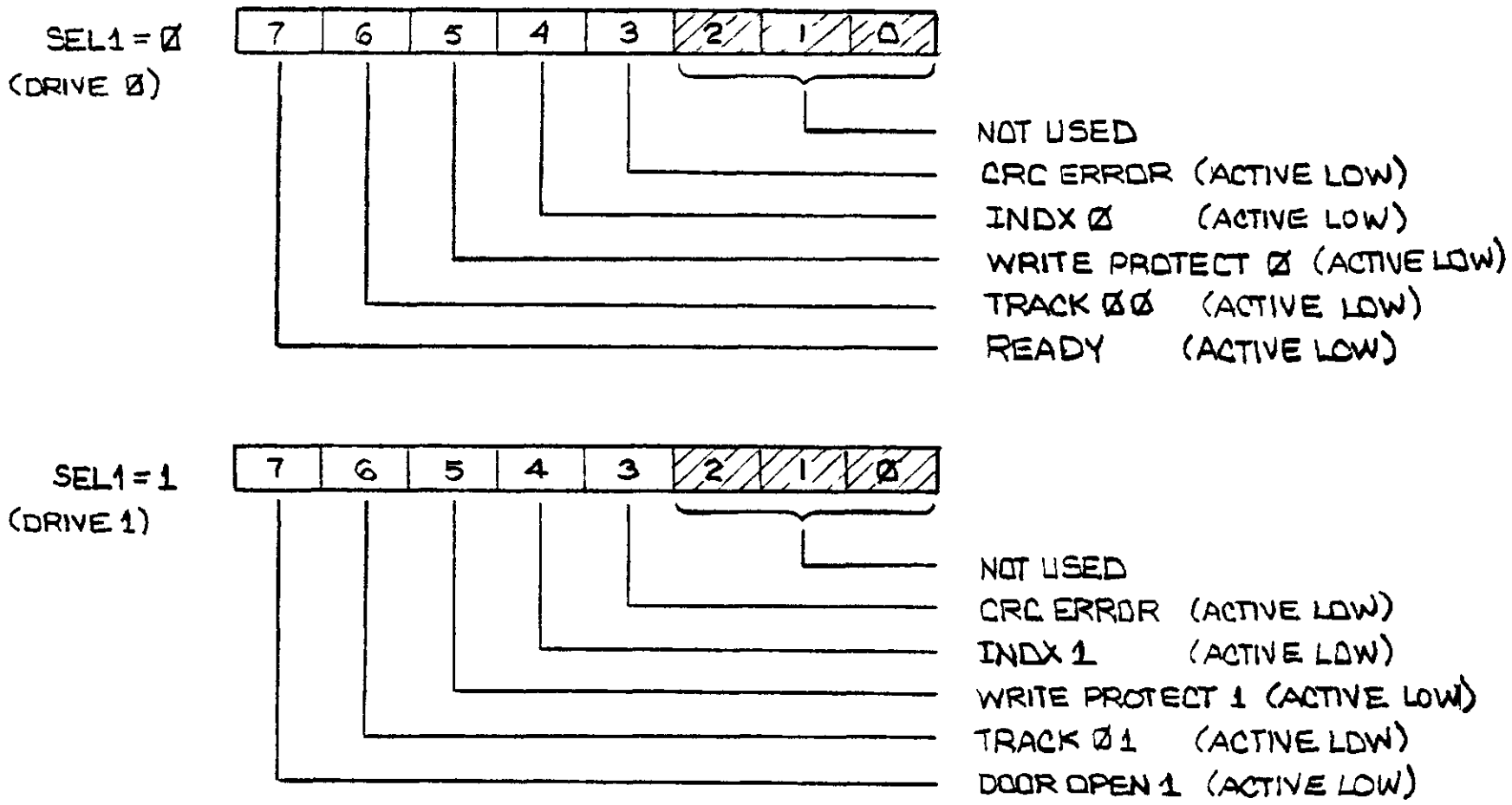
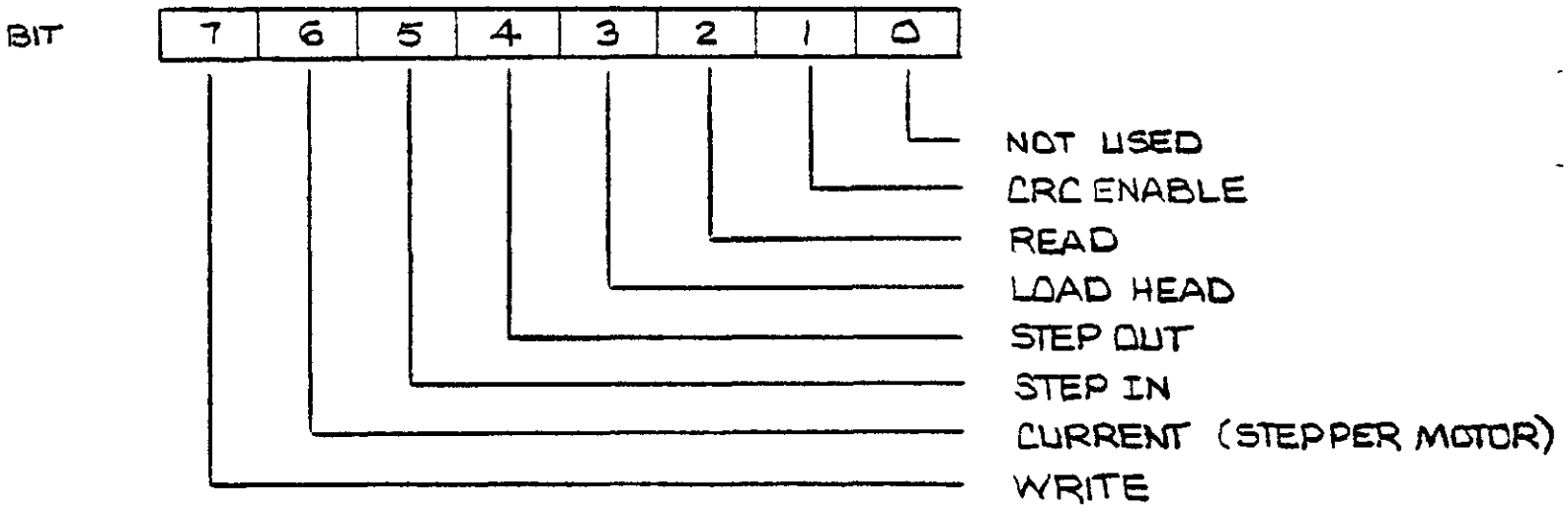


Figure 4-11 Disc Drive Status

CONTROL REGISTER A (PORT F9H)



CONTROL REGISTER B (PORT FAH)

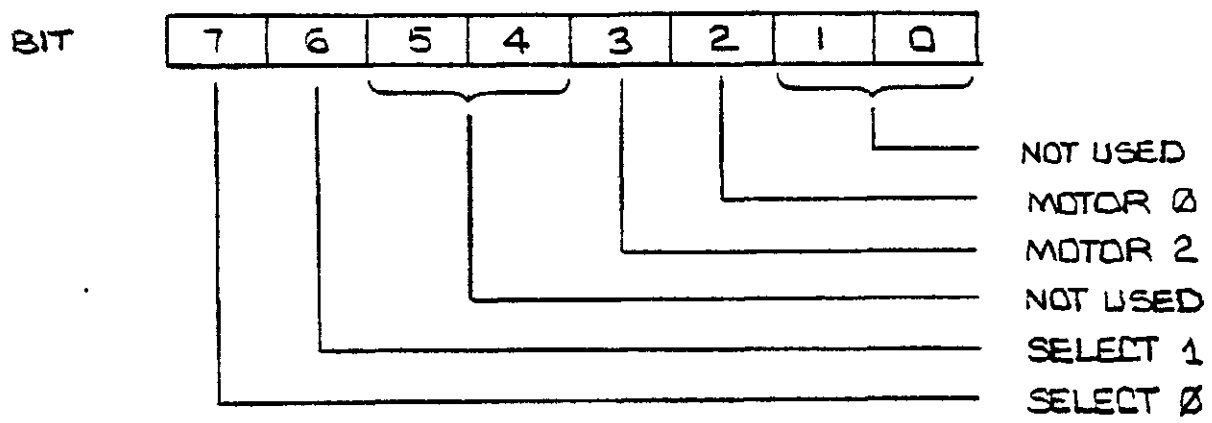


Figure 4-10 DISC CONTROL REGISTERS

4.5 Breakpoint Module

This module functions as a part of the Emulation Subsystem and provides the user with the capability to suspend the real-time execution of a program when selected address, data and control bus events occur. A block diagram, Figure 4-18, is provided as a reference containing specific references to logic Sheet numbers.

4.5.1 Control Logic

The control logic, although not shown on the block diagram, performs an important part in the Breakpoint Module. A majority of the control logic is shown on Sheet 4. This logic is responsible for controlling the loading of address, data, data mask and control bus arguments into the respective registers. Loading of the various arguments must be performed in strict sequence by issuing I/O (Port) write commands to Port FBH. The sequence may be terminated early by issuing an I/O (Port) read to Port FBH which will reset the Sequence Control Register (A7).

The Sequence Control Register (A7) and associated decoder (A14) serve to generate data strobe signals for loading of the selected argument registers. These strobes are active for the duration of the IOWRB pulse generated on logic Sheet 3.

1st Write - LOAD MODE (Control Argument)
2nd Write - LOAD DATA (Data Argument)
3rd Write - LOAD ADDR LOWER (Lower Half of Address Argument)
4th Write - LOAD ADDR UPPER (Upper Half of Address Argument)
5th Write - LOAD DATA MASK (Data Mask Argument)

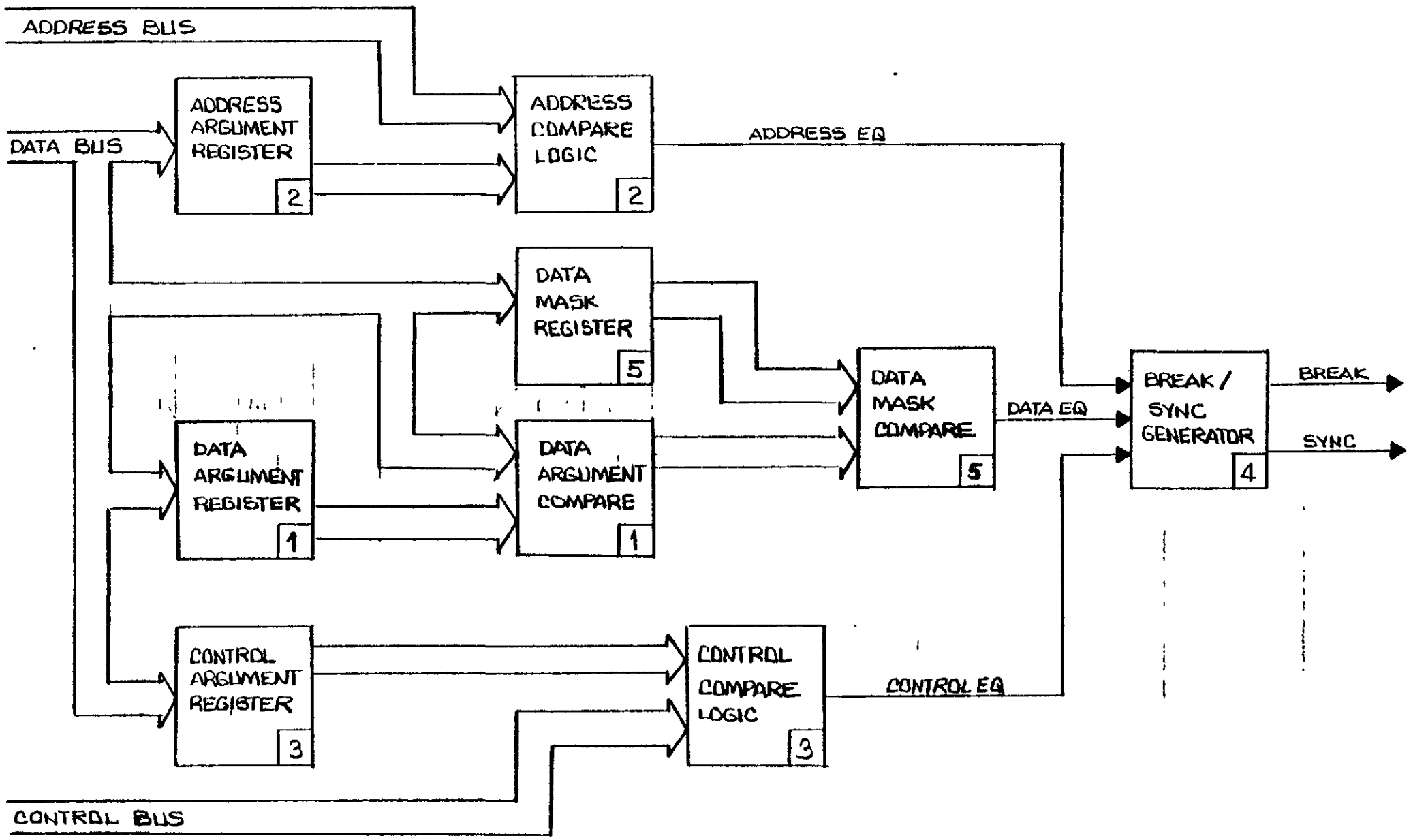
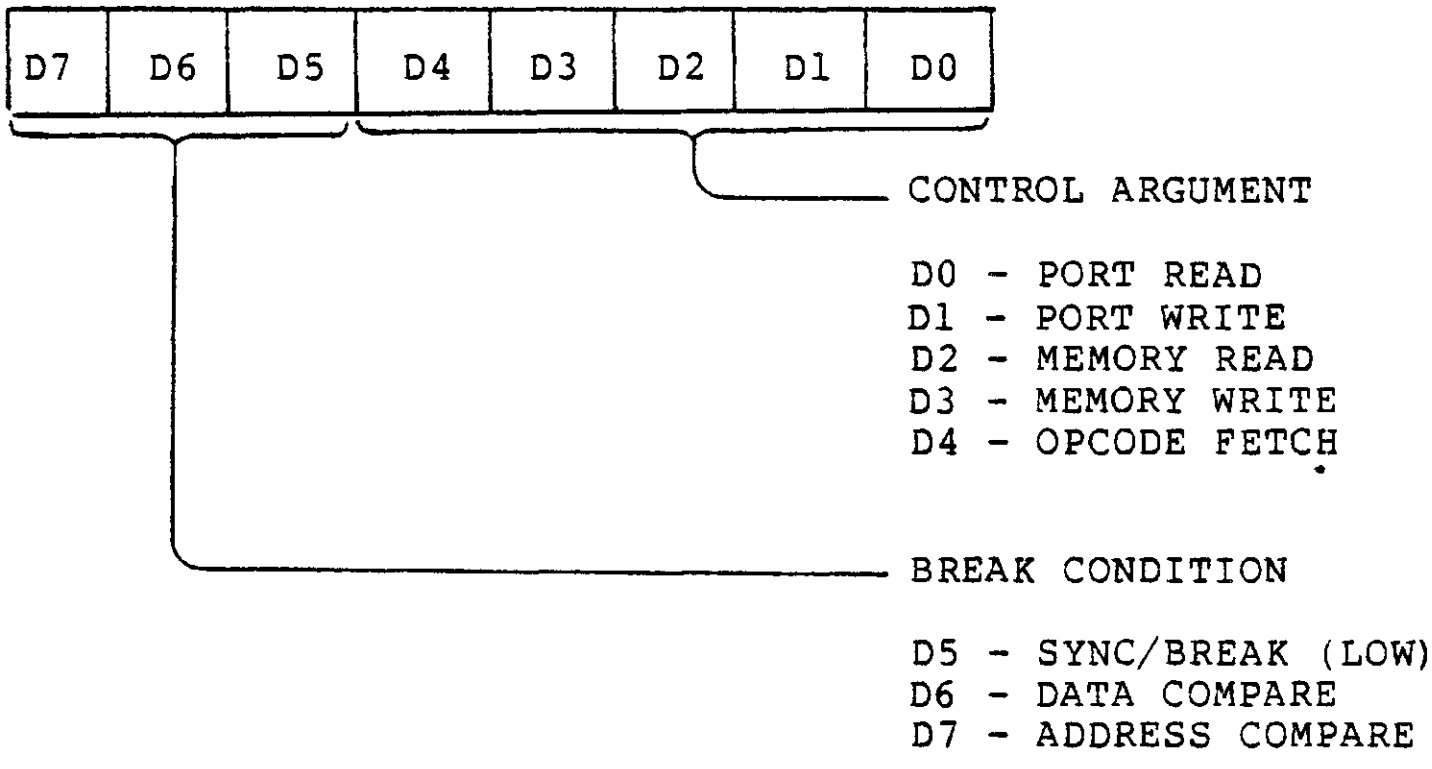


Figure 4-18 BREAKPOINT MODULE - BLOCK DIAGRAM

Generation of the first write (LOAD MODE active low) causes the control bus argument to be loaded (Sheet 3) and also loads the Break Condition Register (A12) on Sheet 4. The bit configuration of the data bus, for loading these registers is shown below.



4.5.2 Address Argument Register (Sheet 2)

The address Argument Register is composed of four quadruple D-type flip-flops configured to form two eight bit registers having separate clock inputs. Elements A19 and A20 comprise the lower Address Argument Register and A17 and A18 form the Upper Address Argument Register.

Data bus information is transferred into the lower Address Argument Register when the third Port Write is issued to Port FBH while the Upper Address Argument Register is loaded with the fourth Port Write. The outputs of the argument registers feed the B-inputs of the Address Comparators also shown on the Sheet 2.

4.5.3 Address Comparators (Sheet 2)

Address comparison is achieved using four 4-bit magnitude comparators which continuously compare the contents of the Upper and Lower Address Argument Registers with the Z80-CPU's Address Bus (A0-A15). When an equivalence occurs the A=B output of the comparator will be an active high and depending on the state of EN ADDR LSB, the output of A25 or A27 will be gated to flip-flop A3 (ADDR EQ). If the selected Control Bus Argument is true (CONTROL EQ active high) flip-flop A3 will set indicating that an address comparison has occurred. This signal is routed to the Break Condition Selection logic (Sheet 4).

4.5.4 Data Argument Register (Sheet 1)

The data argument is loaded into A22 and A23 during the second I/O (Port) Write to PORT FBH by the clock signal LOAD DATA being active low. Outputs of the Data Argument Register are routed to the Data Comparison logic shown on logic Sheet 1. Once data is loaded into the Data Argument Register it cannot be cleared, instead another write operation must be performed with the data bus set to zero in order to affect a register clear.

4.5.5 Data Argument Compare Logic (Sheet 1)

Contents of the Data Argument Register are compared with the Z80-CPU data bus (D0-D7) using two quad-input exclusive-OR gates (A15 and A16). Equivalence of selected data bits result in D0 EQU - D7 EQU being generated. These signals are routed to the Data Mask Compare logic for another comparison with the

mask, if any, before the DATA EQ flip-flop (A10) may be set. The setting of the DATA EQ flip-flop is contingent on two events, (1) the gating of the DATA BITS EQ signal from the Data Mask Compare logic and (2) the generation of the DATA STROBE signal from the Monitor Module. This is to insure the Real Time Storage Module captures data bus activity before the break actually occurs. The CONTROL EQ signal into the second stage of A10 insures the proper control argument accompanies the condition when the data bus is equivalent to the Data Argument Register.

4.5.6 Data Mask Register (Sheet 5)

The Data Mask Register provides the user with a means to monitor the data bus for a selected bit or group of bits. Components A1 and A2 from the 8-bit Data Mask Register which is loaded by the execution of the fifth Port Write to Port FBH. Like the Data Argument Register the Data Mask Register cannot be reset. It must be reset by writing an all zeroes data byte into it.

4.5.7 Data Mask Compare Logic (Sheet 5)

Data mask comparison is implemented using two quad 2-input positive NAND-buffers (A8 and A9) whose outputs are wire-or'ed to form DATA BITS EQ (active low). The mask function works as follows:

Example: User wants to test for bit 7 being active high from a specific port address.

Function	7	6	5	4	3	2	1	0	
Data Argument Register:	0	0	0	0	0	0	0	0	
Data Bus:	1	0	1	1	0	0	0	1	XOR
Result:	1	0	1	1	0	0	0	1	
Data Mask Register:	1	0	0	0	0	0	0	0	NAND
Result:	0	1	1	1	1	1	1	1	

Any Low Output = Data Bits EQ

4.5.8 Control Argument Register (Sheet 3)

Control bus arguments are loaded into A21 (Sheet 3) and A12 (Sheet 4) upon issuance of the first Port Write to Port FBH by the clock signal LOAD MODE being active low. As mentioned previously in subparagraph 4.5.1 both the control arguments and break condition are loaded simultaneously. Control bus conditions are:

- IORD (D0) Port Read
- IOWR (D1) Port Write
- MRD (D2) Memory Read
- MWR (D3) Memory Write
- M1 (Dr) Opcode Fetch

4.5.9 Control Compare Logic (Sheet 3)

The control bus argument bits are compared with the actual Z80-CPU control bus by A28 and A5, the latter being used for M1 or Opcode Fetch. Only one of the above five conditions may be loaded into the argument register at any one time. Detection of equivalence between the bus and argument register results in CONTROL EQ active low and active high being generated.

4.5.10 Break/Sync Generator (Sheet 4)

The logic provided by the Break/Sync Generator controls when a SYNC pulse and/or BREAK is to be generated. Whenever there is an equivalence between the argument registers and the bus activity a SYNC is generated, a Break may or may not be generated. The QA output of A12 (Break Condition Register) determines if only a SYNC or a SYNC and a BREAK will occur. Whenever a SYNC occurs, the signal forces the BREAK STATUS latch (A6) set. The BREAK STATUS (active high) signal may be examined by executing a Port Read to Port FEH. This latch may be reset by POWER ON CLR (low) or a Port Read to Port FBH.

If a BREAK occurs the signal (active low) is gated via A30-pin 13 to the Monitor Module where it is used to trigger the Mode Change Logic thereby causing a transition from User Mode to Monitor Mode terminating the execution of the user's program.

4.6 Real Time Storage Module

The Real Time Storage Module provides the function of a programmable storage device which monitors the Z80-CPU address, data and control buses while running in USER or Monitor Mode. Figure 4-X provides a block diagram which will be used as a reference from the following text.

4.6.1 Storage Array (Sheets 1 and 2)

Data storage for the selected bus events by eight 256 x 4 bit static RAMs. These RAMs serve to store 16 address bits (A0-A15), 8 data bits (D0-D7), seven bits of control information and a first event stored marker bit to indicate the beginning of the most current trace activity. The Storage Control logic provides an address to all eight static RAMs simultaneously so that it functions as a 256 x 32 bit memory.

Although data is stored into the memory array in quantities of 32 bits (WR signal active low) it is read from the array in eight bit fields. This is accomplished by holding the address lines (RA0-RA7) in a fixed state and executing four Port Read operations from Port Address FCH, reference subparagraph 4.6.6.

4.6.2 Address Latches (Sheet 1)

Three quad D-type latches (A11, A12 and A13) are provided to latch the Address Bus (A0-A15) of the Z80-CPU during either USER or MONITOR modes of operation. The latches are clocked by DATA STB B (active high) which originates from the Monitor Module. The latches provide a temporary storage for the Address Bus information prior to writing it into the Storage Array components A3, A4, A5 and A6.

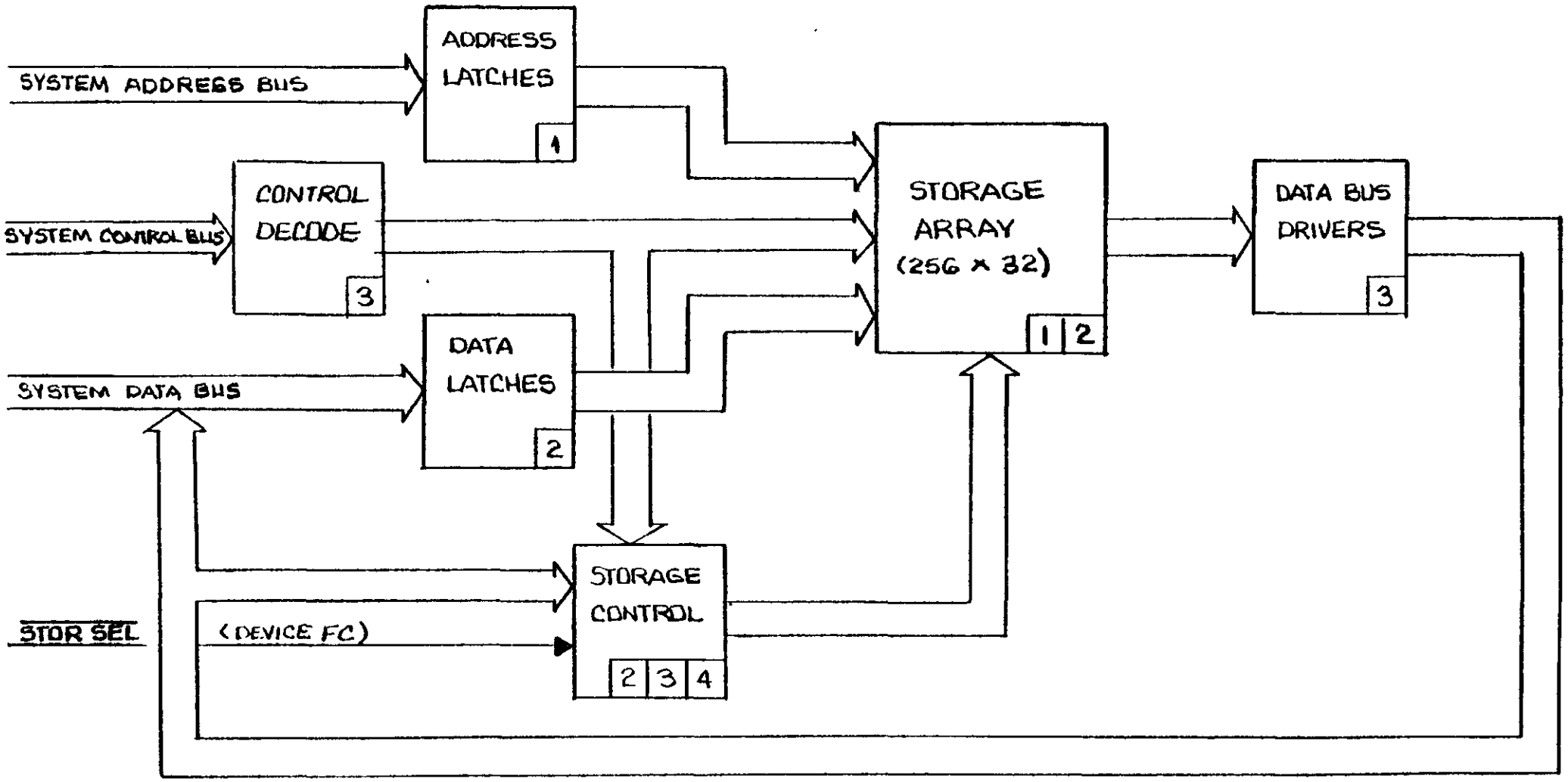


Figure 4-19 Real Time Storage Module - Block Diagram

4.6.3 Data Latches (Sheet 2)

Two quad D-type latches (A18 and A23) are provided to latch the Data Bus (D0-D7) of the Z80-CPU during USER or MONITOR modes of operation. Like the address latches they are clocked by DATA STB B (active high) from the Monitor Module. Outputs of the latches are routed to memory components A1 and A8 of the Storage Array.

4.6.4 Control Decode (Sheet 3)

The Control Decode logic provides a method of compacting various Z80-CPU control bus signals before storing them in the Storage Array. Logic is provided by A25 and A27 to AND selected control signals to result in a value which better describes the bus event in progress. The source signals and resultant signals, which are stored, are shown below.

SOURCE	RESULT	
MRQ, RD	MRD	MEMORY READ
MRQ, WR	MWR	MEMORY WRITE
IORQ, RD	IORD	I/O READ
IORQ, WR	IOWR	I/O WRITE
IORQ, M1	INT ACK	Interrupt Acknowledge

In addition to the aforementioned signals two others are also stored which are BUSAK (A24-pin 3) and HALTA (logic Sheet 2). The state of the aforementioned five signals are latched by a single quad D-type latch (A26) which is clocked by DATA STB B. The BUSAK and HALTA signals are not latched because these are signals which have a long duration when active and are thus not time critical.

4.6.5 Data Bus Drivers (Sheet 3)

Two bus driver elements (A16 and part of A17) interface the output data lines from the static RAM storage Array to the system data bus. These drivers are only enabled in Monitor Mode when an I/O Read is issued to Port FCH (STOR SEL active low).

4.6.6 Storage Control Logic (Sheets 2, 3 and 4)

The Storage Control Logic provides two functions: 1) controls loading of the Storage Array, and 2) unloading of the Storage Array for software.

In order to determine what types of transactions are to be stored in the Storage Array the user loads the qualifier into the Real Time Storage Module by executing a Port Write to Port FCH while in Monitor Mode. Data bits D0-D3 contain the qualifier which is strobed into a quad D-type latch (A19) on logic Sheet 3. The outputs of this latch are ANDed with the decoded signals MRD, MWR, IORD and IOWR by A20 to generate a write strobe WR DATA (active low) to the Storage Array when running in USER mode (emulation). Latched address, data and control bus information will then be written into the Storage Array. Concurrently, the contents of the Address Generator (A9 and A10 on Sheet 4) for the Storage Array will be incremented pointing to the next sequential location in the array.

To read the contents of the Storage Array the system must be in MONITOR Mode and Port Reads to I/O Port FCH must be executed. Since 32 bits represent one bus event, four consecutive Port Reads must be executed, each transferring 8 bits to the system data bus. The selection of which 8-bit field is to be transferred is determined by a counter (A22) and associated decoder (A15) as shown below.

Port Read	Count	8-Bit Field Transferred
1	0	LSB. STORED ADDRESS BUS (A0-A7)
2	1	MSB. STORED ADDRESS BUS (A8-A15)
3	2	STORED DATA BUS (D0-D7)
4	3	STORED CONTROL BUS

Once four consecutive Port Reads have been executed the counter reaches a full count, decoded as RD CONTROL (active low) which generates the READ signal (Sheet 3) on the next Port Read to decrement the Address Generator (A9 and A10) on logic Sheet 4. The effect is that the most recent event stored is the second one read, etc. The 3K Debug PROM will continue the reading of the data until it encounters the first event stored marker (Bit 7 of the stored control information) or the appropriate number of user specified events entered from the system console.

4.7 Mapper/ICE Module

The M/ICE provides the circuitry used to interface the Emulation Subsystem logic to the user's prototype via a three (3) foot cable and terminator. This module depicted in block form by Figure 4-20 which will be used as a reference for the following subparagraphs.

Essentially, the Mapper/User Hardware Interface consists of an extension of the Z80 System bus with address, data and control fed to the user through tristate buffers allowing in-circuit emulation.

4.7.1 Address Decoder (Sheet 2)

The Z80 memory address space is normally assigned to exist internal to the system, as are I/O ports for stand-alone operation. When the user interface cable is in place, the address space of the target hardware can be allocated between internal, system RAM and ROM/RAM and I/O external to the ZDS-1/25. Memory mapping is implemented as a switch between internal and external bus accesses.

4.7.2 Memory Mapper (Sheet 2)

The system clock, originating on the CPU card, is fed directly to clock switch logic on this card, allowing the user to determine the source of system PHI. The external clock is monitored for integrity and will revert to system clock in the event of external clock failure. In order to preserve system integrity, monitor mode operations are conducted under system clock.

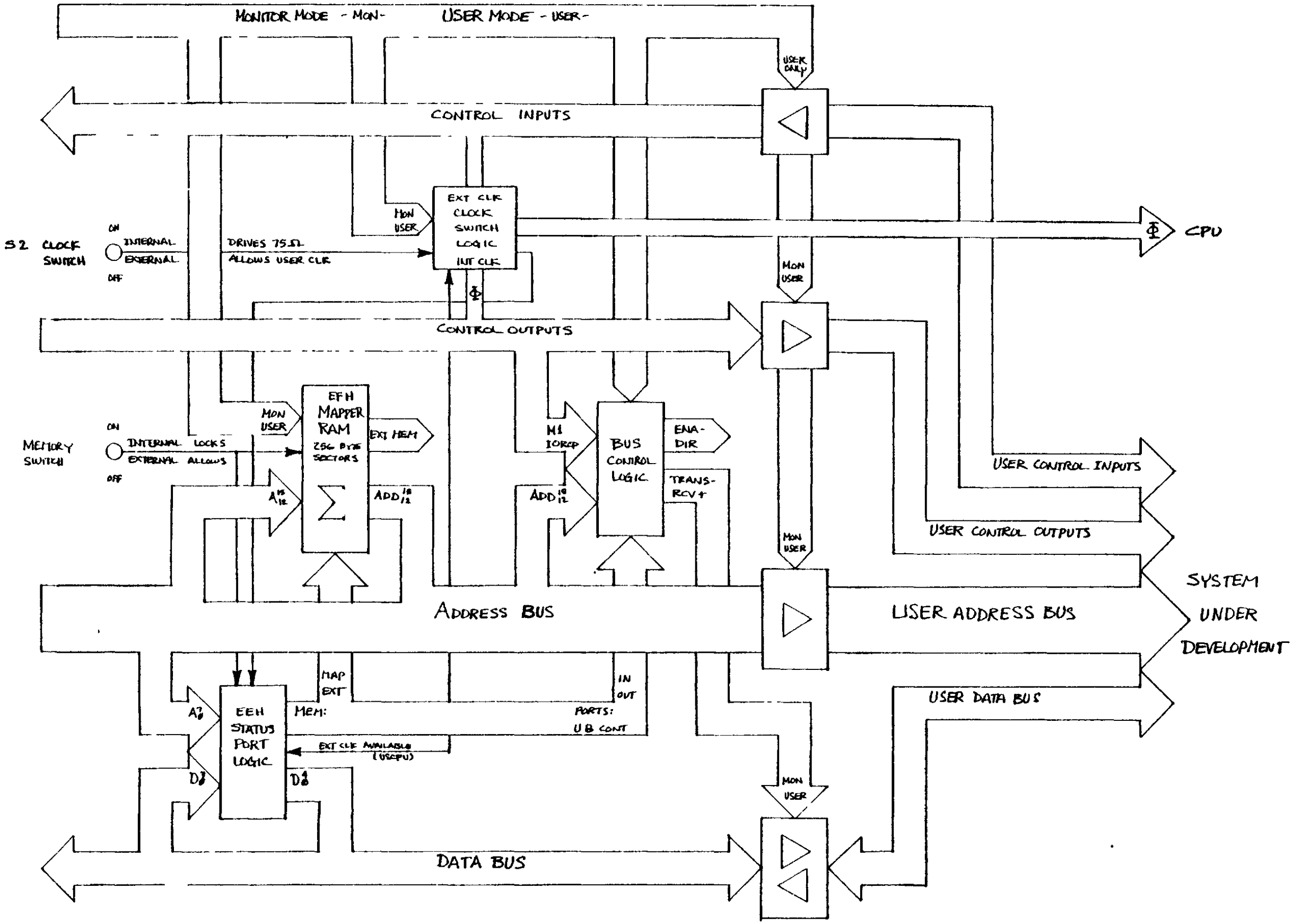


FIGURE 4-20. MAPPER/ICE BLOCK DIAGRAM JH 71017

4.7.3 Address Bus Drivers (Sheet 2)

Sheet 1 of the schematics contains receiver A02 for user-generated signals including NMI, INT, WAIT, BUSRQ, and external clock if selected by rear panel switch S2. Driver A12 supplies BUSAK, HALT, PHI, and system IEO to the cable connector in the event the user wishes to daisychain the development hardware. Also, in the absence of an external clock source, system clock can be supplied with 75 OHMs drive capability by selecting internal clock (S2 ON).

4.7.4 Output Control Bus (Sheets 1 and 3)

The logic of A23 and A24 comprise a synchronous clock dropout detector to insure CPU clock integrity. The 9316, driven by system PHI provides a ripple carry pulse to set Q1 every 16 clock periods. Meanwhile, the External clock being monitored is strobing a zero from D to Q1 on every falling edge. PHI divided by four then passes Q1 to XCON meaning external clock is on (active low). Should external clock fail XCOF (external clock off) is latched low until power on clear is asserted.

Clock selection is based on several inputs to the clock select logic. Power on clear or an external clock failure will force the selection of internal clock to the CPU. If S2 selects Extenal dlock, then the transistion to user mode in the ZDS-1/25 will be accompainied by the synchronous switch to user clock. USCPU mode (in which the user clock drives the CPU always) is selected by a Port Write to Port EE (PWEE) with data bit 7 low. This mode is useful when external hardware must remain synchronous to the CPU clock in monitor mode. (Jumper A18-015 to A07-006 to implement.) A 1K resistor provides line termination for the incoming clock.

4.7.5 Input Control Bus (Sheet 1)

Sheet 2 of the schematics contains bus control logic and buffering for the address and data busses. Drivers A3-A5 provide 16 address bits to the user (unless tristated by BUSAK+).

Adder A6 provides the monitor mode offset that makes the system PROM activity appear to take place between F000 and FFFF HEX (page 15). In user mode this offset is transparent to user addresses.

PROM addresses from page 15 are decoded by bus control PROM A21. Control outputs TRANS- and RCV+ regulate monitor mode

bus activity (e.g., RETI) from confusing external peripheral devices. Linking the internal and external daisychain would prevent similar side effects from RAM resident system software.

Another input is user bus control. Originating on the monitor card UB.CONT requests bus transceivers A7 and A8 to drive the system bus. This is contingent upon external port or memory selection via status Port EE.

4.7.6 Data Bus Buffers (Sheet 2)

Sheet 3 of the schematics show control bus buffer A1. The option of disabling UMRQ and UM1 is provided for memory interfaces whose bus control logic cannot tolerate M1 or MREQ if memory if that address is mapped elsewhere.

System IEO (IE*) is generated by A29 which OR's the individual IEO's from the CPU and peripheral cards. It is the term IE* that should be linked to user IEI to insure proper user interrupt handling.

4.7.7 Clock Synchronization Logic (Sheet 1)

Memory mapping is accomplished with bipolar static RAM A13. The eight most significant address bits are used to delineate 256 sector within the RAM. A logic one in any location represents a sector of internal memory. Zero represents a request for memory outside the ZDS-1/25. This information is available to buffer A28 for interrogation via D0 on the data bus, though it is intended for the user memory enable output by way of A32 and A33. Mapping is enabled via data bit D1 of status Port EE. External memory can be selected in its entirity by data bit D2 of Port EE. External ports are enabled by a zero to data bit 3 or Port EE.

4.7.8 External Memory

A situation arises when mode zero interrupts are occurring in external memory. By virtue of the fact that the CPU expects two additional memory read cycles in response to a call instruction during the mode 0 interrupt acknowledge cycle, the call vectors returned must be issued to the CPU during these memory reads. It is therefore necessary to insure that external memory is selected in such an event. Latch A36 is set by an external interrupt acknowledge, and is subsequently cleared by the resulting writes, caused by the PC being pushed

onto the the stack. Since this occurs for all modes of interrupts, regardless of mode.

4.7.9 External Clock

Data bit D4 represents the clock function: external clock available. Note that either S2=0N or an ext. clk. failure causes D4 = 1.

Programming the status port is done simply by selecting the function with active low bits (see table above). Once programmed the functions will remain selected until POWER ON CLEAR is asserted.

As a convenience, the option of all external bus can be invoked by a PWEE with data bit 0 low. This causes D1, D2, and D3 to be stored low in the status port, and all accesses are considered external.

TABLE 1

I. FEATURE OVERVIEW

*	Readable Clock Integrity Detector	PREE-D4
*	Select Internal/External Ports	PWEE-D3
*	Select Internal/External Memory	PWEE-D2
*	Disable/Enable Memory Map	PWEE-D1
*	Readable Memory Switch (S0)	PREE-D0
*	Readable Clock Status (S1)	PREE-D4
*	Readable Memory Map	PREF-D0
*	Mode 0 Interrupt Fix	Embedded
*	System IEO (IE*) Available	

II. FUNCTIONS

SWITCH	FUNCTION	STATES	BIT	PORT	READ	WRITE
S0 ON	Internal Bus	1=INT	D0	EE	1	X
S1 ON	Internal Clock	Drive	D4	EE	F.	X
S0 OFF	Ext Bus Environment		D0	EE	0	.E=EXT BUS
	Enable Mapper	0=ON	D1	EE	.C	.D
	Enable w/EXT Ports		D1,D3	EE	.4	.5
	EXT Memory	0=EXT	D2	EE	.A	.B
	EXT w/EXT Ports		D2,D3	EE	.2	.0
	EXT Ports	0=EXT	D3	EE	.6	.7
S1 OFF	EXT CLK Environment		D4	EE	E.	X
	CLK Integrity	0=OK	D4	EE	E.	X

TABLE 2

The bitmap implemented in this revision (09-0104-02 Rev. 4) of the Mapper/ICE is as follows:

	R		F		T			F	R				T			F
0000	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0010	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0020	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0030	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0040	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0050	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0060	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0070	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0080	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0090	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
00A0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
00B0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
00C0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
00D0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
00E0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
00F0	0C	0C	05	05	02	02	02	07	0C	05	0C	05	02	07	02	07
0100	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0110	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0120	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0130	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0140	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0150	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0160	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0170	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0180	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
0190	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
01A0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
01B0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
01C0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
01D0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
01E0	0C	0C	05	05	02	02	02	07	0C	0C	0C	0C	02	02	02	06
01F0	0C	0C	05	05	02	02	02	07	0C	05	0C	05	02	07	02	07

4.8 MONITOR MODULE

The Monitor Module provides several discrete functions for the system and plays a primary role in the control of the Emulation Subsystem. A block diagram is provided by Figure 4-21 which may be used as a reference.

4.8.1 Panel Interface (Sheet 1)

The Panel Interface logic is shown on Sheet 1. It consists of the MONITOR and USER, HALT and WAIT indicators located on the front panel of the system. The outputs from the MONITOR and USER latches are routed to the System Status Buffer (A27) and to the Mode Select Logic on Sheet 2.

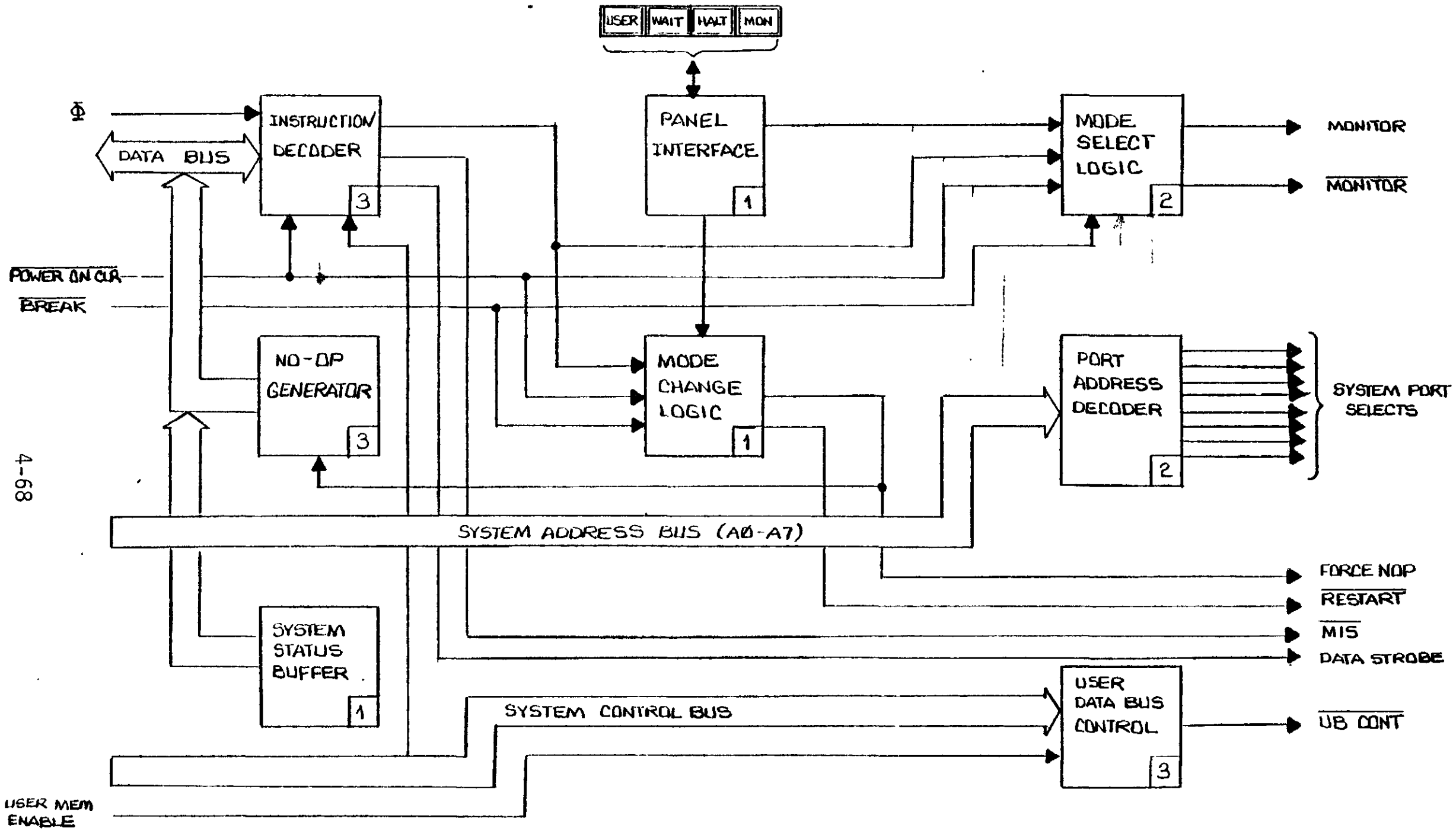


Figure 4-21 MONITOR MODULE - BLOCK DIAGRAM

4.8.2 Instruction Decoder (Sheet 3)

The Instruction Decoder serves to monitor the system data bus to insure that only a single M1 signal (M1S) is generated at the beginning of each instruction. During multi-byte instructions M1 is generated for each byte accessed from memory. This situation is undesirable for emulation control therefore the combination of A28, A1, A2, A3, A8, A9 and A16 provide the necessary logic to enable the generation of M1 (M1S) for the first opcode fetch of a double byte or triple byte instruction.

The resultant output (M1S active low) is routed to the Mode Change Logic (Sheet 1) and the Mode Select Logic (Sheet 2) to insure the transition from USER to MONITOR mode or vice versa occurs in a manner which synchronizes it with Z80-CPU instruction fetch.

4.8.3 Mode Change Logic (Sheet 1)

The Mode Change Logic provides for the mode transition synchronization caused by operator depression of the USER or MONITOR switches, or a Breakpoint (BREAK active low). The detection of the mode change is reflected immediately by A14 pin 5, then synchronized with M1S (previously described) to generate FORCE NOP.

Also generated, when the Z80-CPU reads the next instruction from the data bus, in NOP (active low) which gates a NOP (00H) onto the data bus to the Z80-CPU via A21 and part of A29 (Sheet 3). At this same time RESTART D (active low) is also routed to the RTSM to prevent the writing of the NOP into the RTSM. The CHANGE MODE CLR (active low) generates SYS RESET (active low) on Sheet 2 and SYS CLR, which resets the Mode Change Logic (A14-1).

4.8.4 NO-OP Generator (Sheet 3)

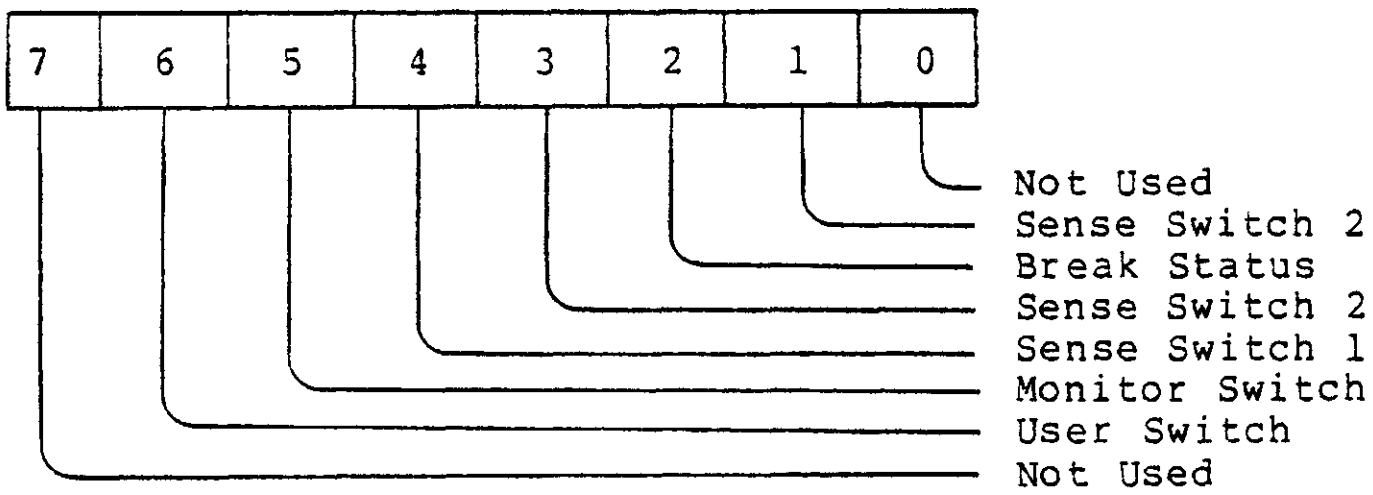
The NO-OP Generator serves to place an all zeroes byte (NOP) onto the data bus inputs to the Z80-CPU when a mode change or breakpoint occurs. The generator is merely a bus driver whose inputs are grounded and these are gated to the data bus when the NOP (active low) signal is generated by the Mode Change Logic.

4.8.5 Mode Select Logic (Sheet 2)

The Mode Select Logic is composed of two flip-flops (A18), a latch (A31) and associated gating logic (A10, A17). This serves to detect the depression of the MON or USER Mode by the 3K PROM firmware. Detection of one of the above conditions is reflected by the latch (A31) which is then synchronized by M1S to set A18-pin 5 followed by A18-pin 9 on the following M1S. The result is the generation of MONITOR (either active high or low) which is routed with its inverse to the system Breakpoint Module, CPU Module and Real Time Storage Module.

4.8.6 System Status Buffer (Sheet 1)

A status byte containing system status is provided by a buffer A27 on logic Sheet 1. This may be read by executing a Port Read command from I/O Port FEH. The status byte definition is shown below.



4.8.7 Port Address Decoder (Sheet 2)

The system I/O Port addresses are decoded (Sheet 2) by A30 and A32. This "centralized" decode function minimizes the number of select lines which must be routed to the various boards in the system. The port assignments for the system are shown in Table 4-3.

Table 4-3. System I/O Port Assignments

Port (HEX)	Device
F0	Counter-Timer Port 0
F1	Counter-Timer Port 1
F2	Counter-Timer Port 2
F3	Counter-Timer Port 3
F4	USART Data Port
F5	USART Control Port
F6	----
F7	----
F8	Disk Data Port
F9	Disk Control Port B
FA	Disk Control Port A
FB	Breakpoint
FC	RTSM
FD	System Reset or User Mode
FE	System Status Port
FF	Serial Latches

4.8.8 User Data Bus Control (Sheet 3)

Logic Sheet 3 contains the user data bus control signal which is applied to the User Interface Module to control the direction of the bidirectional data bus drivers for the data bus interface between the user's prototype and the development system. When the UB CONT signal is active low the data bus drivers are set to receive data from the user's prototype system, when high the drivers place data from the development system data bus onto the user's data bus in the prototype.

The UB CONT signal may be generated in one of three cases shown below.

USER MEMORY ACCESS (READ):

This event is signaled by USER MEM ENABLE (active low) from the memory mapper logic on the User Interface Module. The MREQ and RD signals further qualify the logic (A11 and A5) to generate UB CONT (low). It is important to note that the USER MEM ENABLE (low) serves to disable MRD (active low) preventing system memory access.

USER I/O PORT READ:

Whenever I/O Port Read (IORQ logical zero) is executed from any device other than Port addresses E0-FFH (DEV E+F logical zero) the UB CONT signal will be generated. This is also true for MONITOR mode but the MON DIS signal serves to disable the bidirectional bus drivers on the User Interface Module.

INTERRUPT ACKNOWLEDGE CYCLE:

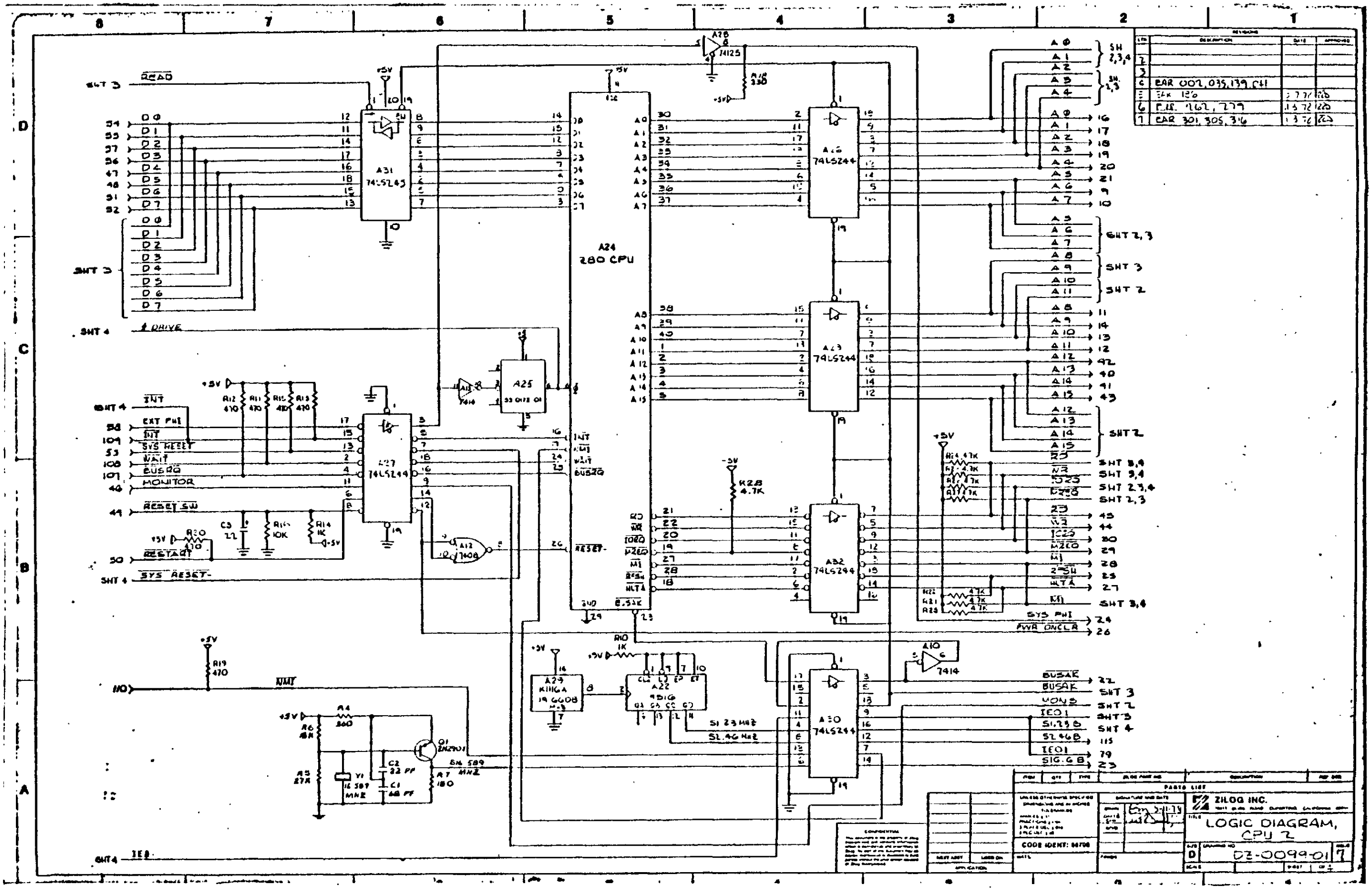
When the Z80-CPU enters an interrupt acknowledge cycle (IORQ and M1 active) the interrupting device can place an eight bit vector onto the data bus. These two signals are qualified by IE (from the lowest priority system device) to distinguish between user interrupts and system interrupts. The IE signal is derived from the IEO line of the lowest priority interrupt-driven device, usually the Counter-Timer Circuit on the SCON Module.

4.8.9 Console Interface Receivers/Drivers (Sheet 4)

The actual receiver and driver circuits for both the 20 ma. TTY console interface and the RS232C interface are shown on logic Sheet 4. This circuitry provides the transmit and receive signal interface between the SCON Module and the console connector on the rear of the system. Other pertinent RS232C signals are provided directly by the SCON since they are not used for 20 ma. current loop.

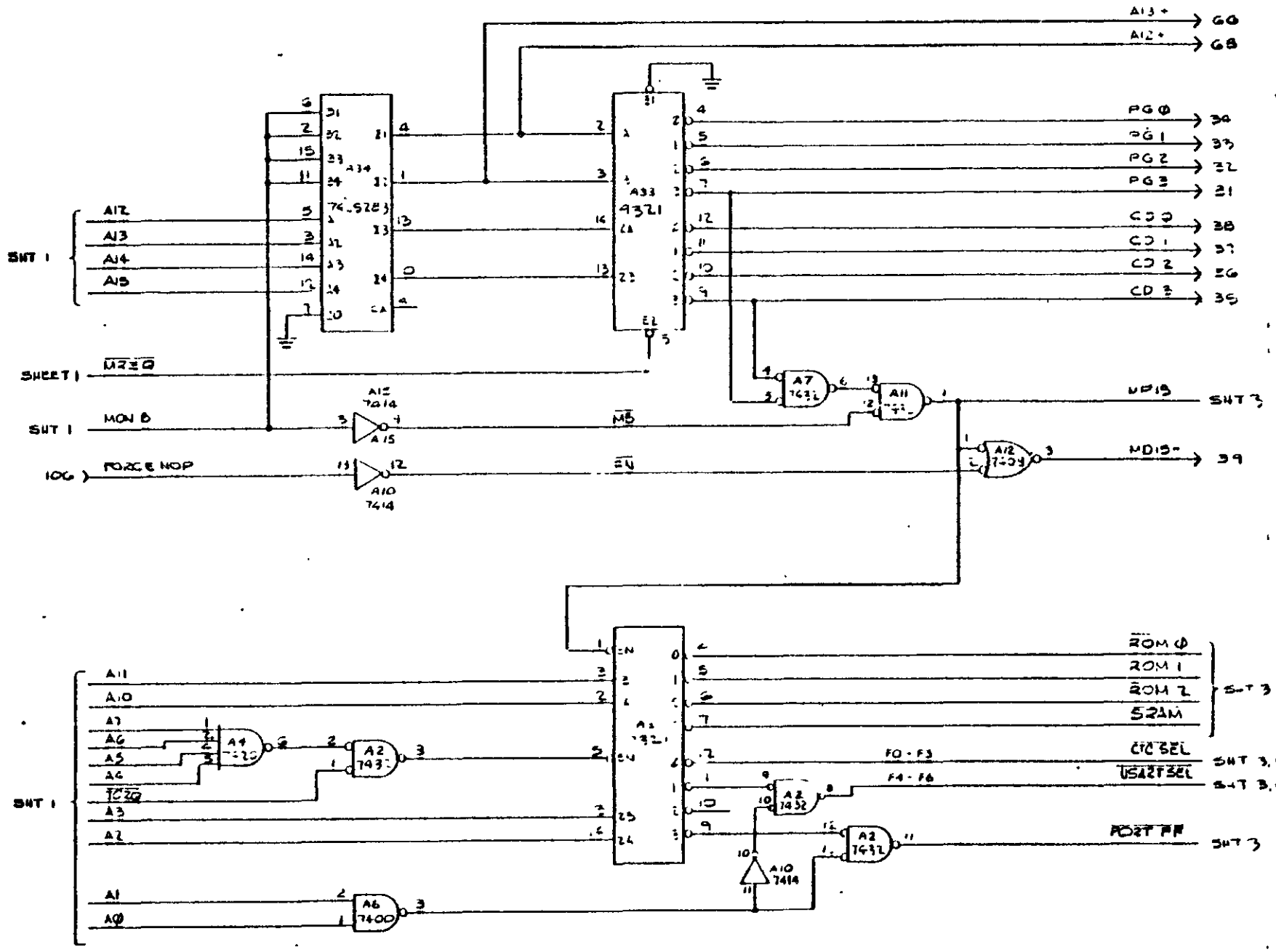
APPENDIX A

CPU SCHEMATICS



LTR	DESCRIPTION	DATE	APPROVED
2			
3			
4	EAR 002, 035, 139, 241		
5	EAR 126	3 7 76	[illegible]
6	EAR 162, 279	4 5 76	[illegible]
7	EAR 301, 305, 316	4 3 76	[illegible]

LTR	DESCRIPTION	DATE	APPROVED
7	SEE SHT 1	1.16.76	ZDD



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES
			PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/16
2 PLACE DEC ± .01
3 PLACE DEC ± .010

NEXT ASSY	USED ON
APPLICATION	

CODE IDENT: 04700

ZILOG INC.

LOGIC DIAGRAM, CPU 2

SIZE D | DRAWING NO Z-0099-01 | REV 7

SCALE | SHEET 2 OF 4

CONFIDENTIAL

LTR	DESCRIPTION	DATE	APPROVED
7	SEE SHT 1	11.3.78	

SHT 1: A0 A1 A2 A3 A4 A5 A6 A7 A8 A9

90 +12V
91 -5V

C31 33 .1 C34 36 .1

E3 E5 E4 R8 1K +5V

A17 2708 A18 2708 A19 2708 +5V

A13 2114 A14 2114 +5V

SHT 2: ROM 0 ROM 1 RCU 2 SRAM

SHT 1: D0 D1 D2 D3 D4 D5 D6 D7

A16 74LS245 EN

ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7 SHT 4

SHT 1: M1

SHT 2: MREQ

A11 7432 A7 7427 A1 7400 7414 M2D15 M1ORD

SHT 1: IORQ

SHT 1: IEO 1

SHT 2: CTC SEL USART SEL

A1 7400 A2 1K -5V A10 7414 M1D EN

GT: SYS MEM BUSAK

SHT 1: MREQ RD WR

SHT 2: ABORT FF

SHT 4: ST

A2 7402 M2D

A11 7432

A5 7403 A7 7427 GWR

A5 7403 IORQ A5 7432 PEOFF

A26 74LS5

READ SHT 1

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

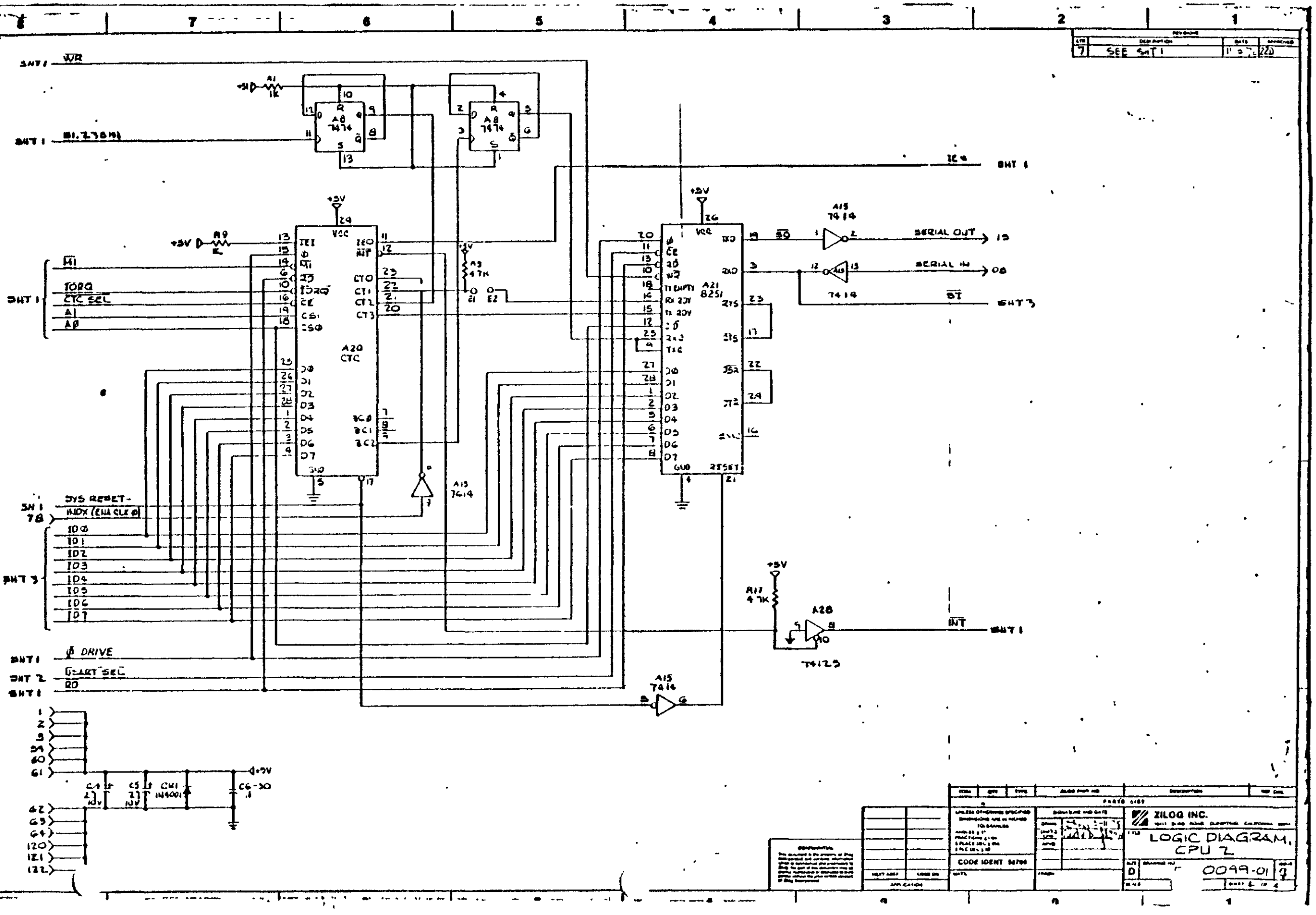
CODE IDENT: 56708

ZILOG INC.

TITLE: LOGIC DIAGRAM, CPU 2

SIZE: D DRAWING NO: 02-0099-01 REV: 7

SCALE: SHEET 3 OF 4


SHT 1 WR
SHT 1 M1, IORQ
+5V
A1 1K
A8 74174
SHT 1 IEO
+5V
R9 1K
SHT 1 M1
IORQ
CTC SEL
A1
A0
A20 CTC
D0 D1 D2 D3 D4 D5 D6 D7
CLK/TRG0 CLK/TRG1 CLK/TRG2
CTO CT1 CT2 CT3
+5V
R3 4.7K
A21 8251
SERIAL OUT
SERIAL IN
A15 74LS14
SHT 3
SYS RESET-
INDX (EMA CLK Ø)
SHT 3 ID0 ID1 ID2 ID3 ID4 ID5 ID6 ID7
SHT 1 Ø DRIVE
SHT 2 UART SEL
SHT 1 RD
A15 74LS14
+5V
R17 4.7K
A28 74125
INT
SHT 1
1 2 3 59 60 61
62 63 64 120 121 122
C4 .1 50V
C5 .1 50V
CR1 IN4001
+5V
C6 .1
ZILOG INC.
LOGIC DIAGRAM, CPU 2
CODE IDENT 56796
D
0099-01
9

SYM	REVISIONS DESCRIPTION	DATE	APPROVED
1	EAR = 225, 214		
2	EAR 186	10.17.78	JD
3	EAR 279, 162	11.3.78	JD
4	EAR 312	11.3.78	JD
5	EAR 301, 305, 306	11.3.78	JD

A21 280 CPU

A22 4516

A23 74LS244

A24 74LS244

A25 33-0122-01

A26 74LS244

A27 74LS244

A28 74125

A29 K1164A 19 6608

A30 74LS244

A31 AM8304B

A32 74LS244

A10 7414

A12 7408

Q1 2N2907

84.589 MHZ

51.23 MHZ

51.46 MHZ

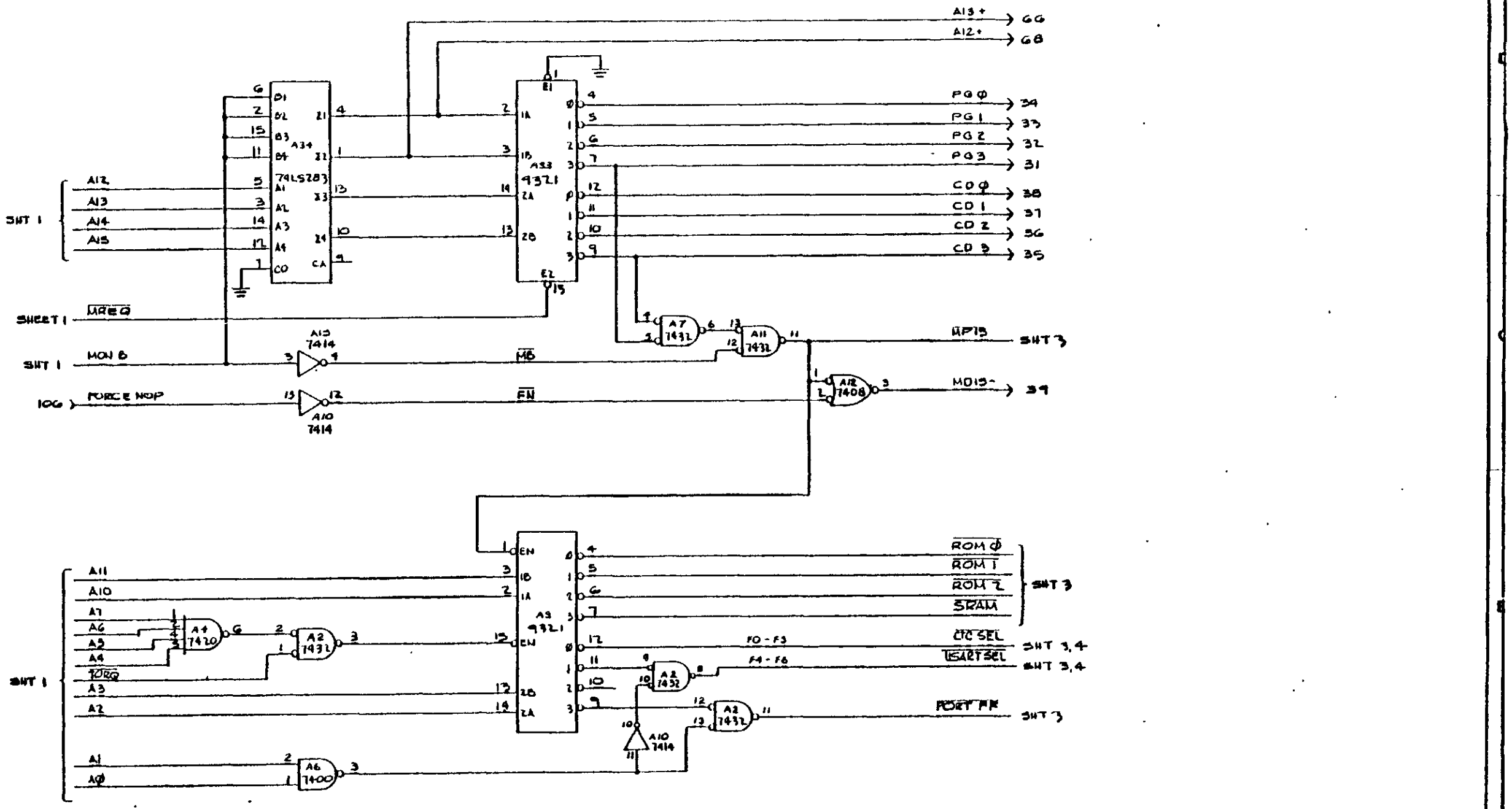
ZILOG INC.

LOGIC DIAGRAM, CPU 2

CODE IDENT. 56708

D 02-0099-02 5

LTR	DESCRIPTION	DATE	APPROVED
5	SEE SHT 1	11-3-78	RD



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES

FRACTIONS ± 1/64
2 PLACE DEC ± .01
3 PLACE DEC ± .010

CODE IDENT: 28756

MATL

SIGNATURE AND DATE

DRWN 5-11-78
CHKD
APVD
ENGR

NEXT ASSY | USED ON

APPLICATION

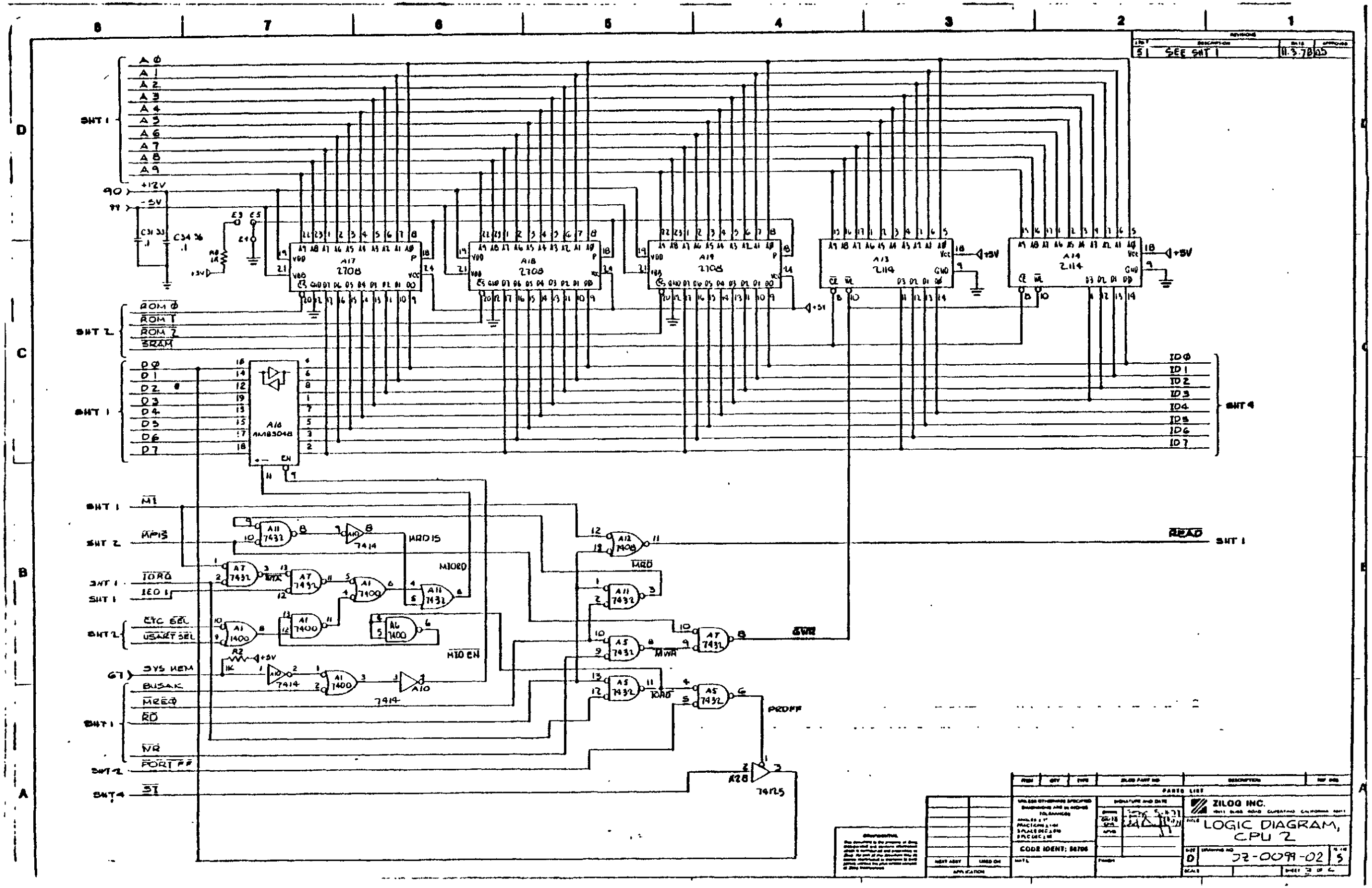
DO NOT SCALE THIS DRAWING

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM, CPU 2

SIZE D | DRAWING NO Z2-0099-02 | REV 5

SCALE | SHEET 2 OF 4



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
5	SEE SHT 1	11.3.78	DS

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES: .XX ±.01 .XXX ±.005 FRACTIONS ±1/64 ANGLES ±1° SURFACE FINISH ±.001

CODE IDENT: 84706

SIGNATURE AND DATE

ZILOG INC.

TITLE: LOGIC DIAGRAM, CPU 2

SIZE: D | DRAWING NO: 02-0099-02 | REV: 5

SCALE: | SHEET 3 OF 6

CONFIDENTIAL

NEXT ASSY | USED ON | APPLICATION

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHT 1	10-17-78	RD

SHT 1 WR

A1 1K

SHT 1 B1.2304 MHz

A8 74174

IEO SHT 1

+5V

A9 4.7K

R9 1K

SHT 1 M1 IORQ CTC SEL A1 A0

A20 CTC

SYS RESET

SHT 1 7B INDX (ENA CLK Ø)

SHT 3 ID Ø ID 1 ID 2 ID 3 ID 4 ID 5 ID 6 ID 7

SHT 1 Ø DRIVE

SHT 2 USART SEL

SHT 1 RD

A15 7414

A21 8251

SERIAL OUT 19

SERIAL IN 08

7414

ST SHT 3

R17 4.7K

A26 74125

INT SHT 1

1 2 3 59 60 61 +7V C4 22 15V C5 22 16V CR1 IN4001 C6 .1 62 63 64 120 121 122

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES

CODE IDENT: 05706

ZILOG INC.

TITLE LOGIC DIAGRAM, CPU 2

SIZE D DRAWING NO 02-0099-02 REV 5

SCALE SHEET 4 OF 4

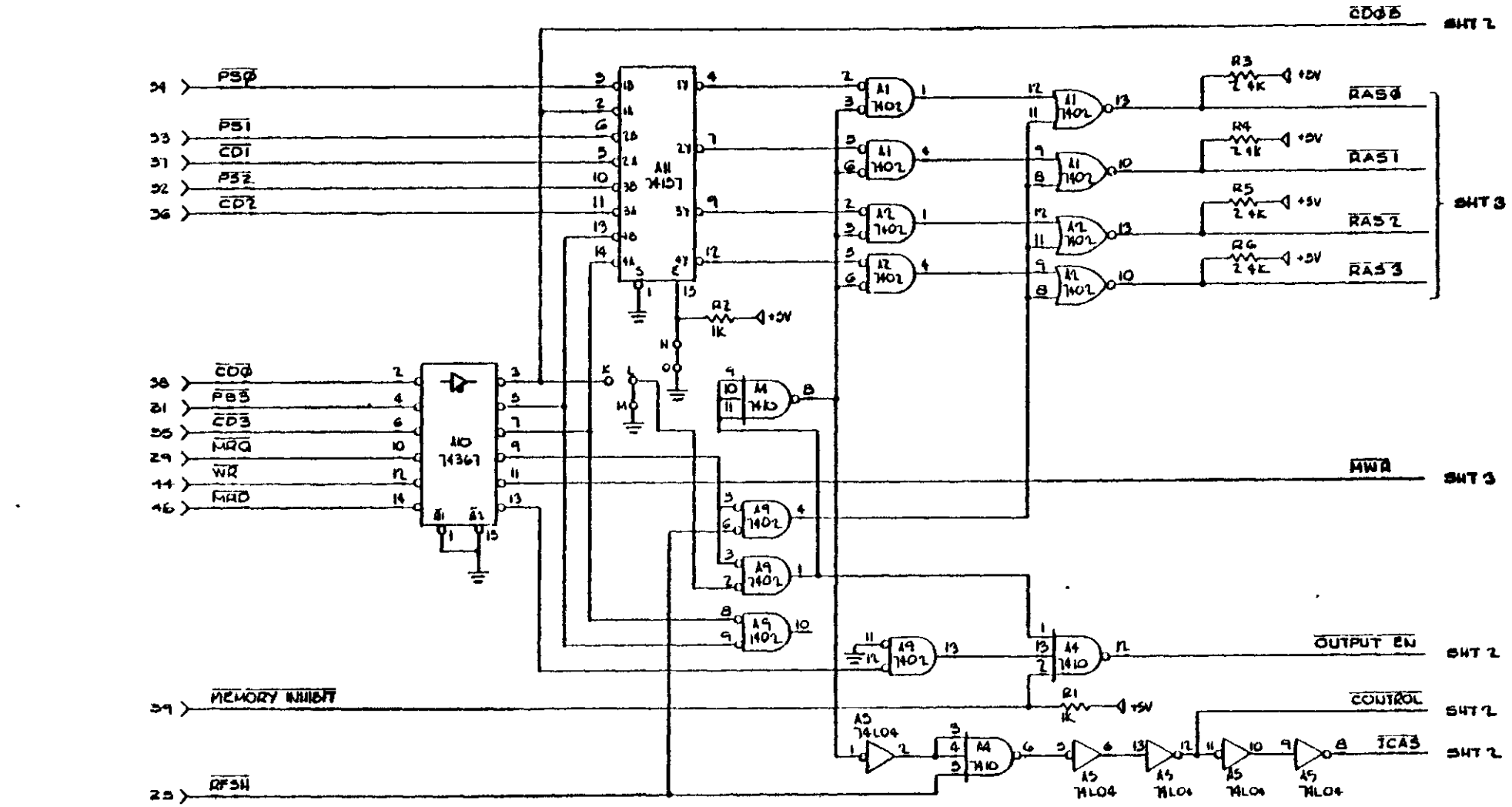
8 7 6 5 4 3 2 1

APPENDIX B

64K MEMORY MODULE SCHEMATICS

CONFIDENTIAL

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECN 00320	3-1-78	WF, JZ



NOTES. UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS 1/4 W, 5%
2. ALL CAPACITOR VALUES ARE IN MICROFARADS

REF DESIG	
LAST USED	UNUSED
A43	
C70	
R7	

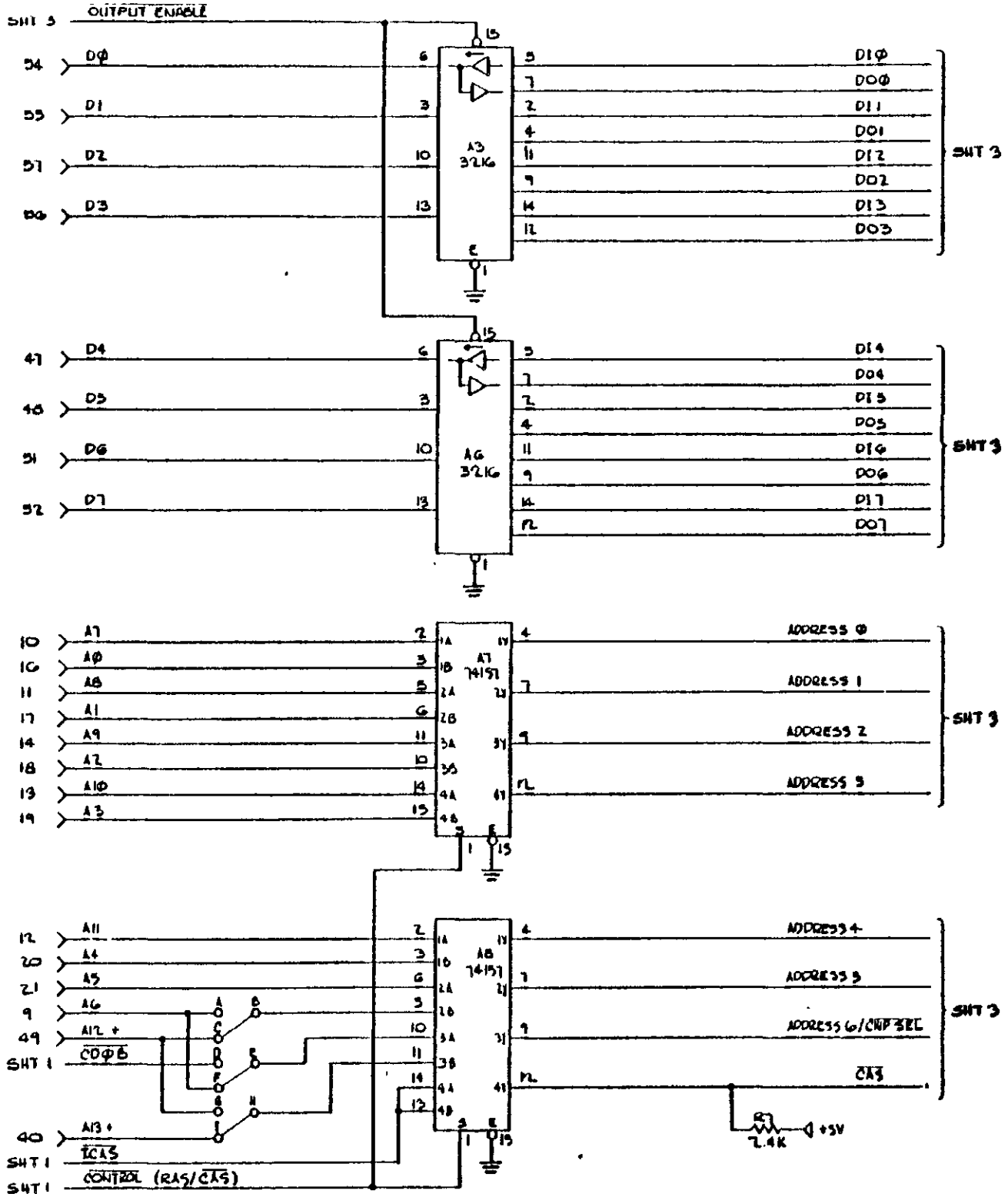
PARTS LIST

ZILOG INC

LOGIC DIAGRAM, MEMORY 25

SIZE D | DRAWING NO 02-0101-01 | REV A

SHEET 3 OF 3



ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES
PARTS LIST					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
2 PLACE DEC ± .010
3 PLACE DEC ± .005

SIGNATURE AND DATE	
DRAWN	[illegible] 4-78
CHK'D	LF 4/6
APVD	[illegible] 4/78

ZILOG INC.
[illegible] BUBB ROAD CUPERTINO CALIFORNIA [illegible]

TITLE: LOGIC DIAGRAM, MEMORY 2S

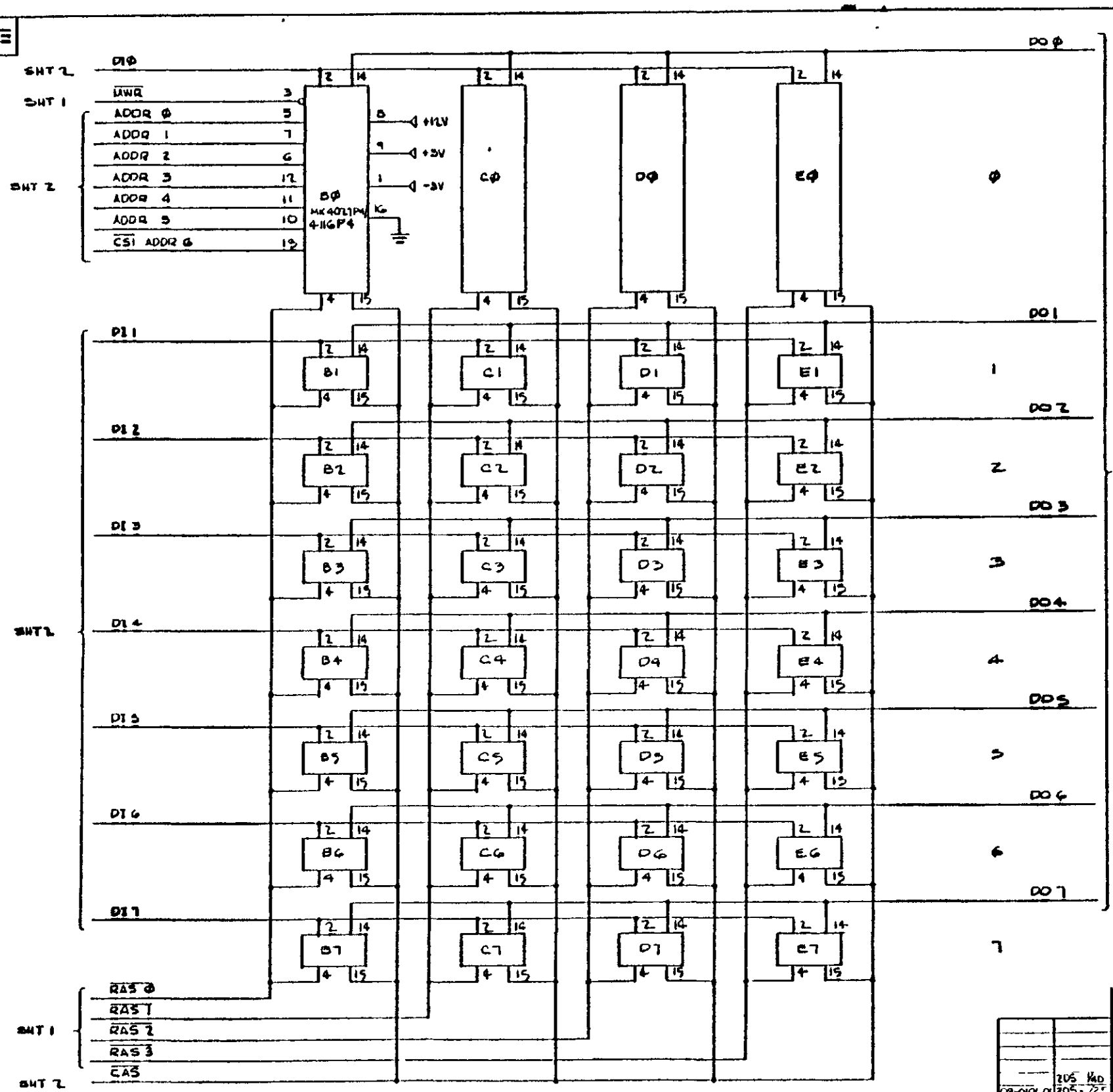
SIZE D | DRAWING NO Z2-0101-01 | REV A

SCALE | SHEET 2 OF 3

01-001-01	105-1/40	
NEXT ASSY	105-1/25	
APPLICATION	USED ON	

MATL ———

FINISH ———



ALL DEVICES ARE WIRE AS SHOWN ON DEVICE NO BΦ
FOR 16K x 8 USE MK4027P-4
FOR 64K x 8 USE MK4116P-4

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

09-0101 01	205 1/4D 205-725			ZILOG INC	
				LOGIC DIAGRAM, MEMORY 25	
				SIZE D	DRAWING NO Z-0101-01 REV A
					SHEET 3 OF 3

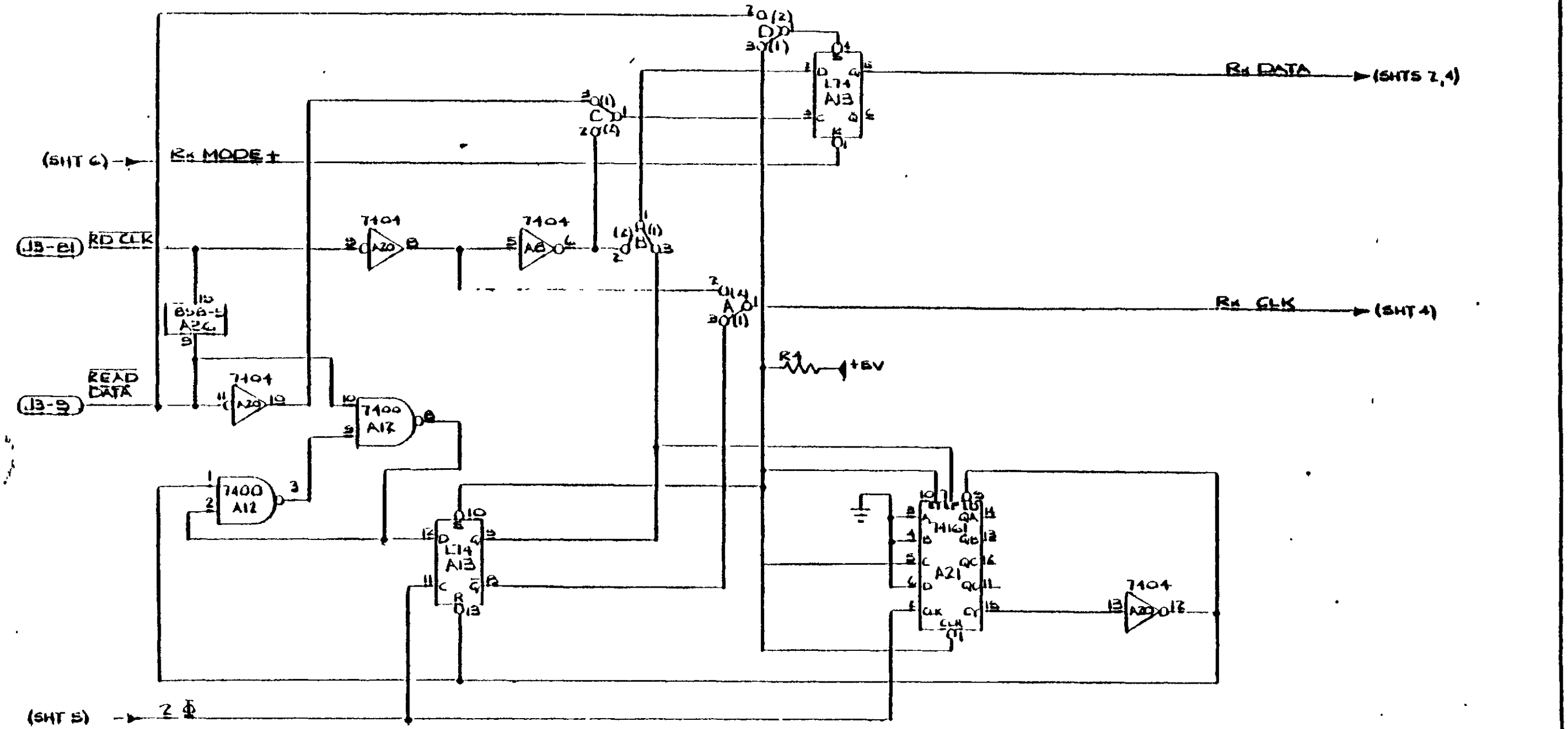
APPENDIX C

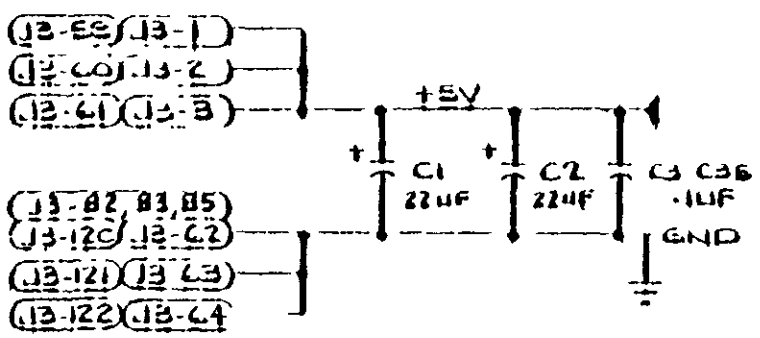
FLOPPY DISK CONTROLLER SCHEMATICS

( )

)

)





J-3

FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		Zilog
APPROVALS	DATE	CONFIDENTIAL
DRAWN N3	4-13-76	
CHECKED		SCALE NONE SIZE C DRAWING NO DZ-0004-01
		DO NOT SCALE DRAWING SHEET 1 OF 7

LTR	DESCRIPTION	DATE	APPROVED
C		1-26-79	

(SHT 3) ← R7B
R6B
R5B
R4B
R3B
R2B
R1B
(SHT 3) ← R0B

7495A A23 (MODE = 6)
A: 2, B: 2, C: 1, D: 15
1 D
2 C1
B C2
QA 13, QB 12, QC 11, QD 10

7495A A24 (MODE = 6)
A: 2, B: 3, C: 4, D: 15
1 D
2 C1
B C2
QA 13, QB 12, QC 11, QD 10

(SHT 1) ← RX DATA
(SHT 4) ← SHIFT CLK
(SHT 4) ← TX LOAD

TXD → (SHT 7)

RCV DATA → (SHT 7)

(SHT 3) ← READ CHAR
(SHT 4) ← RX BUFF LOAD

74173 A31
7 CLK, 15 CL
D1 14, D2 13, D3 12, D4 11
Q1 1, Q2 2, Q3 9, Q4 10
QA 3, QB 4, QC 5, QD 6

74173 A32
7 CLK, 15 CL
D1 14, D2 13, D3 12, D4 11
Q1 1, Q2 2, Q3 9, Q4 10
QA 3, QB 4, QC 5, QD 6

(SHT 3) ← D0
D1
D2
D3
D4
D5
D6
(SHT 3) ← D7

FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
± ± ±

APPROVALS	DATE
DRAWN Mills	1-18-79
CHECKED	

Zilog

CONFIDENTIAL

SCALE NONE | SIZE C | DRAWING NO 02 0004-01

DO NOT SCALE DR | SHEET 2 OF 7

BISHOP GRAPHICS/ACCUPRESS BLUNDELL A 27.0

(SHT 5) IOWR

(J3-118) DISK CONT B (DEV FA)

(SHT 5) → IORD

(J3-117) DISK CONT A (DEV F9)

(J3-116) DISK DATA (DEV FB)

7432 A14

7432 A14

7432 A14

7432 A14

7432 A16

74111 A15

WR CONT 1 → (SHT 6)

WR CHAR → (SHT 4,5)

READ CHAR → (SHT 2,5)

READ STATUS → (SHT 6)

WR CONT 2 → (SHT 6)

D7B
D6B
D5B
D4B
D3B
D2B
D1B
D0B
→ (SHT 3,6)
→ (SHT 2,6)

(J3-52) D1
(J3-51) D6
(J3-48) D5
(J3-47) D4
CPU

74173 A33

→ (SHT 2,6)
→ (SHT 2,6)
→ (SHT 2,6)
→ (SHT 2,6)
→ (SHT 2,6)
→ (SHT 2)
→ (SHT 2)

CPU
(J3-56) D3
(J3-57) D2
(J3-55) D1
(J3-54) D0

74173 A30

(SHT 5) → A

74125 A17

7404 A20

7420 A15

7420 A15

7400 A2

7406 A27

WR DATA → (J3-6)

7473A A18

7408 A4

Tx CLK → (SHT 4)

(SHT 7) → TxD B

FLOPPY CONTROLLER

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
APPROVALS	DATE		
DRAWN	4-3-79		
CHECKED			

Zilog

CONFIDENTIAL

SCALE NONE | SIZE C | DRAWING NO Z2-0004-01

DO NOT SCALE DRAWING | SHEET 3 OF 7

LTR	DESCRIPTION	DATE	APPROVED
C		14-18	

START BIT

(SHT 4) → WR MODE

(SHT 1) → Rx DATA

7408 A4

7474 A10

SHIFT CLK

7493A A11

7408 A4

7400 A12

7432 A3

Tx BUFF UNLOAD → (SHT 5,7)

7404 A8

7432 A3

Rx BUFF LOAD → (SHT 2,5)

(Rx t Tx) → (SHT 5)

Tx LOAD → (SHT 2)

(SHT 6) → Rx MODE 1

7486 A5

7404 A10

7451 A5

(SHT 1) → Rx CLK

(SHT 2) → Tx CLK

(SHT 4) → WR MODE 1

(SHT 6) → Rx MODE

7486 A5

7408 A4

(Rx CLK-) t (Tx CLK+)

SHIFT CLK → (SHT 2,7)

+5V

R2

7404 A20

7474 A6

7474 A6

(SHT 3) → WR CHAR

WRITE ENABLE → (SHT 7)

FLOPPY CONTROLLER

TOLERANCES UNLESS DIMENSIONS SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN MJ	4-15-7X
CHECKED	

Zilog

CONFIDENTIAL

SCALE NONE | SIZE C | DRAWING NO DZ-0004-01

DO NOT SCALE DRA | SHEET 4 OF 7

LTR	DESCRIPTION	DATE	APPROVED
C		1-24-78	

J3-16 RDY
J3-12 DOOR OPEN
J3-11 TRK Ø Ø
J3-10 TRK Ø 1
J3-13 WR PROT Ø
J3-8 WR PROT 1
J3-15 INDX Ø
J3-14 INDX 1

898-5 A36 — 898-5 A36 — 74157 A37 — 74361 A28

D7 → (SHT 3)
D6
D5
D4
D3 → (SHT 3)

INDX → J3-7 CTC

(SHT 7) → CRC ERR
(SHT 3) → READ STATUS

WR MODE1 → (SHT 4,7)

7406 A27

SEL Ø → J3-18
SEL 1 → J3-14
CURRENT → J3-17

(SHT 3) → WR CONT (FA)

74175 A26: SEL Ø, SEL 1, MOTOR Ø, MOTOR 1

7438 A34

WRITE GATE → J3-25
STEP → J3-28
DIRECTION → J3-27
LOAD HEAD Ø → J3-87
LOAD HEAD 1 → J3-19

7438 A35

STEP OUT 1 → J3-20
STEP IN 1 → J3-22
WRITE 1 → J3-21

(SHT 3) → D7B
D6B
D5B
D4B

74175 A25: WRITE, CURRENT, STEP IN, STEP OUT

D3B
D2B
D1B
DØB
(SHT 5) → WR CONT2 (F5)

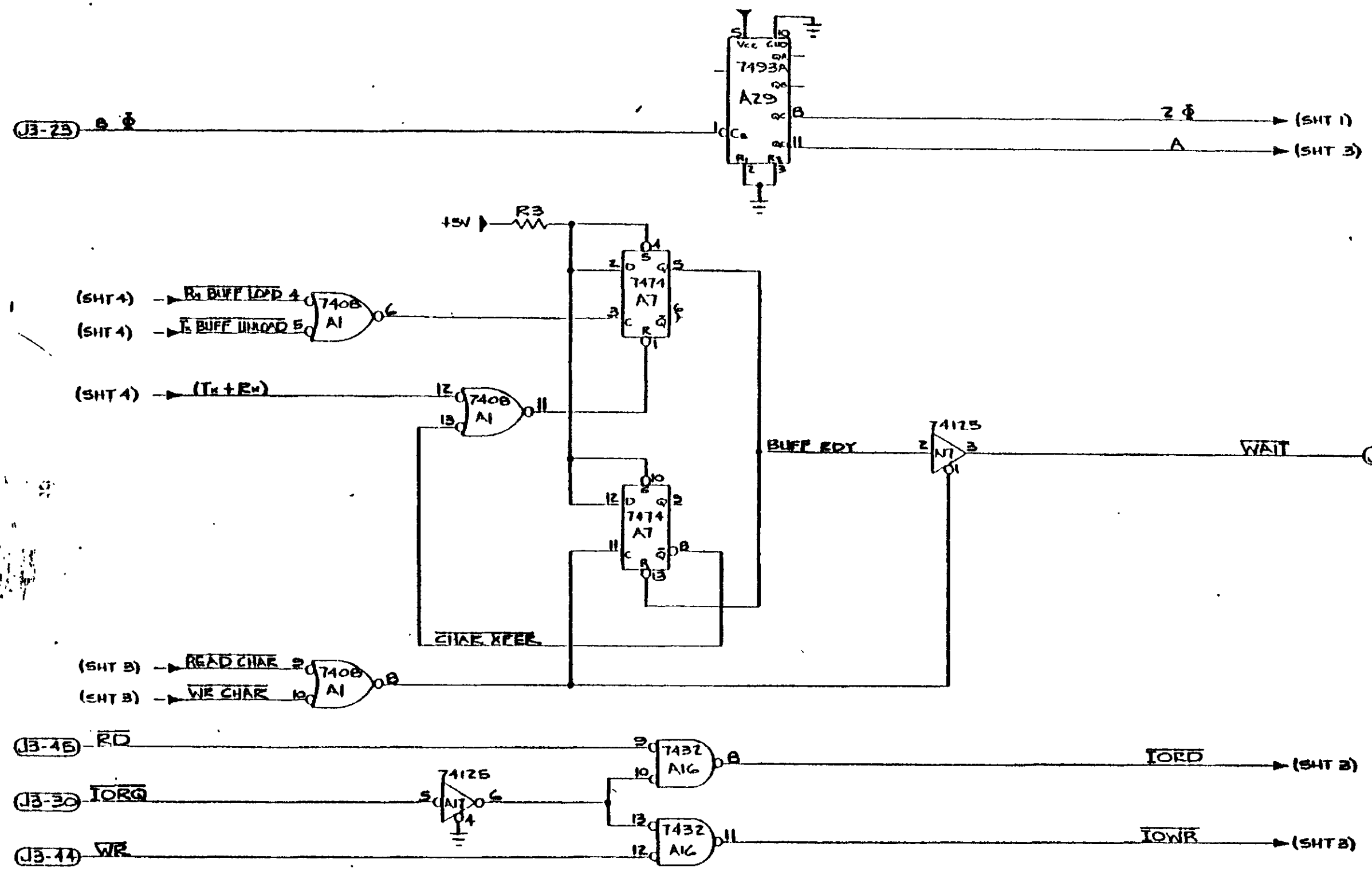
74175 A22: HEAD, RD MODE, CRC

WR MODE → (SHT 4)
RD MODE1 → (SHT 1,4,7)
CRC EN → (SHT 7)
RD MODE → SHT 4)

J3-53 SYS RESET — 74LS A17

FLOPPY CONTROLLER

TOLERANCES UNLESS DIMENSIONS SPECIFIED FRACTIONS DEC ANGLES			
APPROVALS	DATE	Zilog	
DRAWN Hipke	4-15-78		
CHECKED		SCALE NONE	SIZE C
		DRAWING NO 02-0004-01	
		DO NOT SCALE DRAWING	SHEET 6 OF 7



FLOPPY CONTROLLER

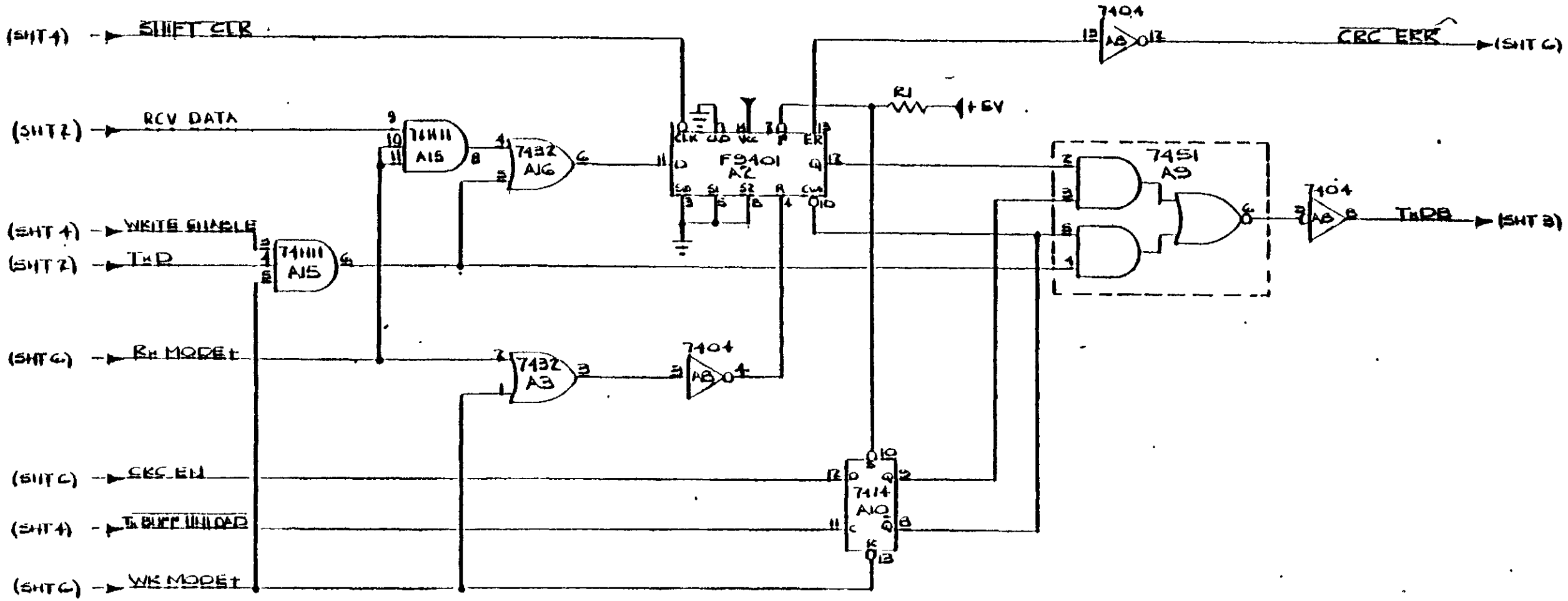
TOLERANCES UNLESS OTHERWISE SPECIFIED	
FRACTIONS DEC ANGLES	
.x ±.x .xx	
APPROVALS	DATE
DRAWN MAJ	4-15-81
CHECKED	

Zilog

CONFIDENTIAL

SCALE NONE | DRAWING NO Z2-0004-01

DO NOT SCALE | SHEET 5 OF 7

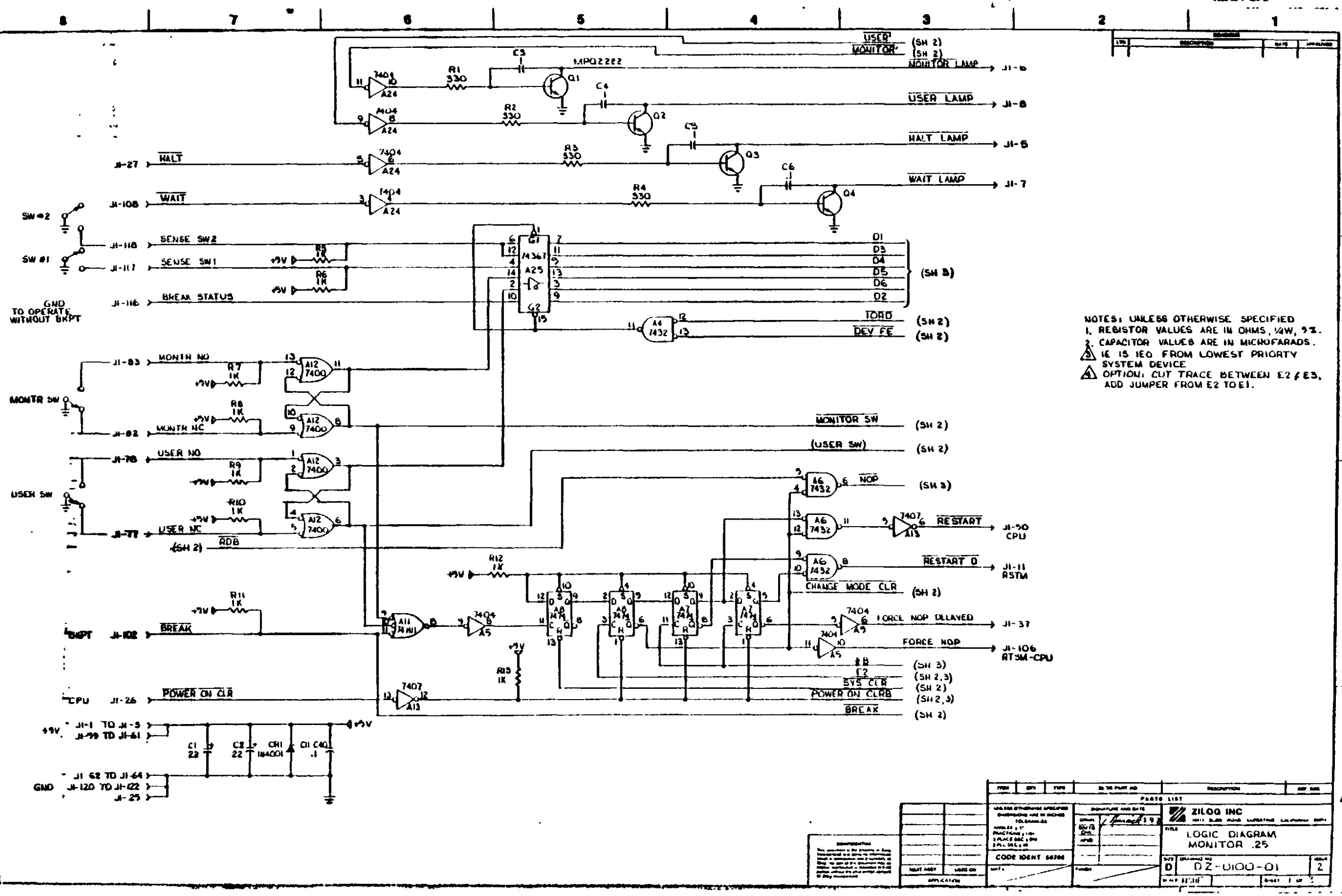


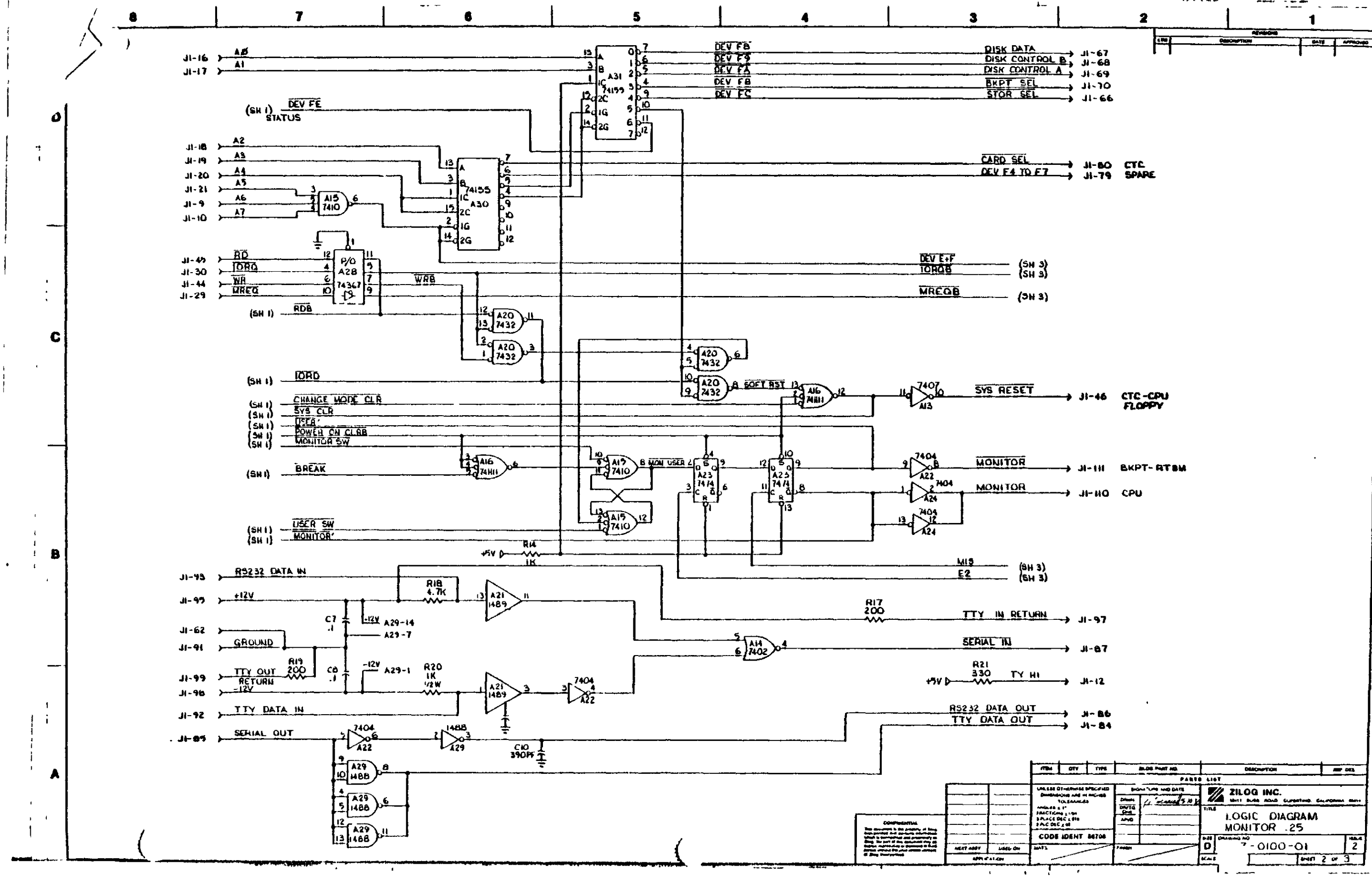
FLOPPY CONTROLLER

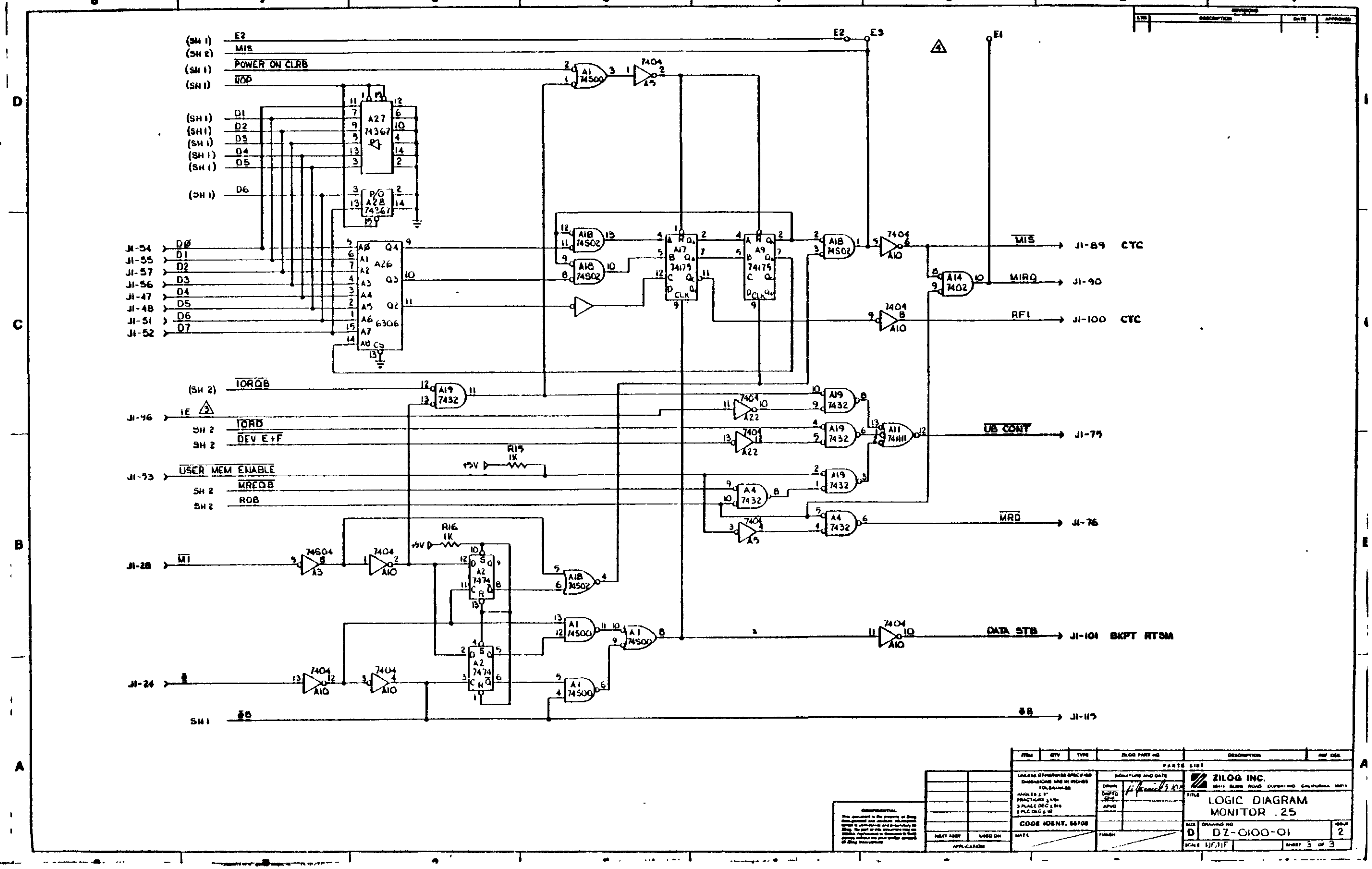
TOLERANCES UNLESS DIMENSIONS SPECIFIED FRACTIONS DEC ANGLES			
APPROVALS	DATE	Zilog	
DRAWN T.N.C.L.A.	4-15-X	CONFIDENTIAL	
CHECKED		SCALE NONE	SIZE C
		DRAWING NO Z-0001-01	
		DO NOT SCALE DRAWING	SHEET 7 OF 7

APPENDIX D

MONITOR SCHEMATICS


USER MONITOR (SH 2) (SH 2)
MONITOR LAMP J1-6
USER LAMP J1-8
HALT LAMP J1-5
WAIT LAMP J1-7
C3 MPQ2222 Q1
C4 Q2
C5 Q3
C6 Q4
R1 330
R2 330
R3 330
R4 330
7404 A24
J1-27 HALT
J1-108 WAIT
SW #2
SW #1
J1-118 SENSE SW2
J1-117 SENSE SW1
J1-116 BREAK STATUS
GND TO OPERATE WITHOUT BKPT
R5 1K
R6 1K
+5V
74367 A25
D1 D3 D4 D5 D6 D2 (SH 3)
A4 7432
TORD DEV FE (SH 2)
J1-83 MONTR NO
MONTR SW
J1-82 MONTR NC
J1-78 USER NO
USER SW
J1-77 USER NC
R7 1K
R8 1K
R9 1K
R10 1K
A12 7400
MONITOR SW (SH 2)
(USER SW) (SH 2)
ADB (SH 2)
A6 7432
NOP (SH 3)
7407 A13
RESTART J1-50 CPU
RESTART D J1-11 RSTM
CHANGE MODE CLR (SH 2)
R12 1K
R13 1K
A8 74H74
A7 74H74
A11 74H11
7404 A5
FORCE NOP DELAYED J1-37
FORCE NOP J1-106 AT&M-CPU
&B (SH 3)
&2 (SH 2,3)
SYS CLR (SH 2)
POWER ON CLR (SH 2,3)
BREAK (SH 2)
J1-102 BREAK
J1-26 POWER ON CLR
R11 1K
+9V J1-1 TO J1-5 J1-99 TO J1-61
GND J1-120 TO J1-122 J1-25
C1 22
C2 22
CR1 IN4001
D1 C40 .1
+5V
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITOR VALUES ARE IN MICROFARADS.
3 IE IS IEO FROM LOWEST PRIORITY SYSTEM DEVICE
4 OPTION: CUT TRACE BETWEEN E2 & E3, ADD JUMPER FROM E2 TO E1.
PARTS LIST
ZILOG INC
TITLE LOGIC DIAGRAM MONITOR .25
CODE IDENT 66706
SIZE D DZ-0100-01 ISSUE 2


8
7
6
5
4
3
2
1
REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
J1-16 A0
J1-17 A1
(SH 1) DEV FE
STATUS
A31 74155
J1-18 A2
J1-19 A3
J1-20 A4
J1-21 A5
J1-9 A6
J1-10 A7
A15 7410
A30 74155
J1-45 RD
J1-30 IORQ
J1-44 WR
J1-29 MREQ
P/O A28 74367
(SH 1) RDB
WRB
A20 7432
A20 7432
A20 7432
A20 7432
(SH 1) IORD
(SH 1) CHANGE MODE CLR
(SH 1) SYS CLR
(SH 1) DSEA'
(SH 1) POWER ON CLAB
(SH 1) MONITOR SW
(SH 1) BREAK
A16 74H11
A17 7410
A15 7410
MON USER
A23 74174
A25 74174
SOFT RST
A16 74H11
7407 A13
7404 A22
7404 A24
7404 A24
(SH 1) USER SW
(SH 1) MONITOR'
+5V R14 1K
J1-95 RS232 DATA IN
J1-97 +12V
J1-62
J1-91 GROUND
J1-99 TTY OUT RETURN
J1-98 -12V
J1-92 TTY DATA IN
J1-85 SERIAL OUT
R18 4.7K
A21 1489
C7 .1
-12V A29-14
A29-7
R19 200
C8 .1
-12V A29-1
R20 1K 1/2W
A21 1489
7404 A22
1488 A29
C10 390PF
A29 1488
A29 1488
A29 1488
A14 7402
R17 200
R21 330
+5V TY HI
DEV FB
DEV F9
DEV FA
DEV F8
DEV FC
DEV E+F
IORQB
MREQB
DISK DATA J1-67
DISK CONTROL B J1-68
DISK CONTROL A J1-69
BKPT SEL J1-70
STOR SEL J1-66
CARD SEL J1-80 CTC
DEV F4 TO F7 J1-79 SPARE
(SH 3)
(SH 3)
(SH 3)
SYS RESET J1-46 CTC-CPU FLOPPY
MONITOR J1-111 BKPT-RTSM
MONITOR J1-110 CPU
MI5 (SH 3)
E2 (SH 3)
TTY IN RETURN J1-97
SERIAL IN J1-87
TY HI J1-12
RS232 DATA OUT J1-86
TTY DATA OUT J1-84
ITEM
QTY
TYPE
ZILOG PART NO.
DESCRIPTION
MFR DES.
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
CODE IDENT 98708
ZILOG INC.
TITLE
LOGIC DIAGRAM
MONITOR .25
SIZE D
DRAWING NO 7-0100-01
ISSUE 2
SHEET 2 OF 3
CONFIDENTIAL


(SH 1) E2
(SH 2) MIS
(SH 1) POWER ON CLRB
(SH 1) NOP
(SH 1) D1
(SH 1) D2
(SH 1) D3
(SH 1) D4
(SH 1) D5
(SH 1) D6
A27 74367
P/O A28 74367
J1-54 D0
J1-55 D1
J1-57 D2
J1-56 D3
J1-47 D4
J1-48 D5
J1-51 D6
J1-52 D7
A26 6306
E2
E3
E1
A1 74S00
7404 A5
A18 74S02
A17 74175
A9 74175
7404 A10
MIS
J1-89 CTC
A14 7402
MIRQ
J1-90
RFI
J1-100 CTC
(SH 2) IORQB
J1-96 1E
SH 2 IORD
SH 2 DEV E+F
A19 7432
7404 A22
A11 74H11
UB CONT
J1-75
R15 1K
+5V
J1-93 USER MEM ENABLE
SH 2 MREQB
SH 2 RDB
A4 7432
MRD
J1-76
R16 1K
J1-28 M1
74S04 A3
A2 7474
A18 74S02
A1 74S00
DATA STB
J1-101 BKPT RTSM
J1-24
SH 1 SS
J1-115
ZILOG INC.
LOGIC DIAGRAM
MONITOR .25
D
DZ-0100-01
2
SHEET 3 OF 3
CODE IDENT. 56708

APPENDIX E

USER INTERFACE/MAPPER SCHEMATICS

LTR	DESCRIPTION	DATE	APPROVED
1		8 X 78	[illegible]
2	EAR # 132, 142	9 12 78	[illegible]
3	EAR # 266	10 9 78	[illegible]
4	EAR # 278, 302	10 19 78	[illegible]

72 UBST-
46 MONITOR
69 UNMI-
7 UINT-
8 UWAIT-
71 UBREQ-
A18 1K
+5V 1K A18-5
A11 74125
A15 7414
220 330 A19.1
RESTART- → 50
MONITOR B SHT 2
NMI- SHT 2
NMI- → 110
INT- → 109
WAIT- → 108
BUSRQ → 107
A2 74367
SENSE SW 2+
SW 2
SENSE SW 2+ → 115
SENSE SW 2- (ON)
SHT 5
A19 220
0.1UF
A15 7414
SW EXT CLK-
SHT 2
112 IE 0
SHT 3 BUSAK-
22 BUSAK-
27 HALT-
24
A12 74367
UIE → 49
UBUSAK- → 103
UHALT- → 101
SW EXT CLK- → 105
84
85
A11 74125
UPWB
A19 7414
EXT CLK/ INCOMING
INT CLK/ OUTGOING
U8 → 102
A18 1K
A10 1K
X-CON- SHT 3
A24 9316
A23 7474
A23 7474
XCON- → NOT USED
XCOF- → NOT USED
8.246 MHz
Φ/4
A36 1400
59 8.246 MHz INCOMING
SHT 3 POWER ON CLR-
SHT 3 USCPUN-
A33 1405
A33 1405
A30 1432
INT CLK CLR-
A22 7474
A10 74S00
A10 74S00
A10 74S00
A34 74S10
A22 7474
A34 74S10
A44 74S10
A10 74S00
EXT PHI → 66
64
A18 1K +5V
+5V 220 A19 330
ITEM QTY TYPE ZILOG PART NO DESCRIPTION REV DES
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES
CODE IDENT 56700
SIGNATURE AND DATE
DRWN
CHKD
APVD
ZILOG INC
10185 ROAD CUPERTINO CALIFORNIA
TITLE LOGC DIAGRAM, USER INTERFACE/MAPPER
SIZE D DRAWING NO 02 0104 02 REV 4
SCALE SHEET 1 OF 3
CONFIDENTIAL
NEXT ASSY ZDS-1/25 USED ON
APPLICATION
8 7 6 5 4 3 2 1

LTR	DESCRIPTION	DATE	APPROVED
4	SEE SHEET 1	10 19 78	[illegible]

SHT 3 BUSAK+

SHT 3 A02 A01 A00 A20
16 A01
17 A02
18 A03
19 A04
20 A05
21 A03
SHT 3 A04 A05
9 A06
10 A07
11 A08
14 A09
13 A10
12 A11
SHT 3 A06 A07 A08 A09 A10 A11
42 A12
40 A13
41 A14
43 A15

A3 74367 → UA00 74, UA01 75, UA02 76, UA03 87, UA04 86, UA05 88
A4 74367 → UA06 90, UA07 91, UA08 31, UA09 32, UA10 92, UA11 93
A5 74367 → UA12 35, UA13 36, UA14 96, UA15 97
A6 74LS283
NMI- SHT 1
ADD12, ADD13, ADD14, ADD15 SHT 3

'BREAK' BUTTON
0.1UF
113 BNMI SW
+5V
A18 1K
A14 7414
A14 7414

ROM 512 x 4

SHT 1 MONITOR B
SHT 3 PORTS OUT-
111 UB CONT-
SHT 3 IORQ-
SHT 3 D0 D1
SHT 3 54 D0
55 D1
57 D2
56 D3
SHT 3 D2
SHT 3 D3
47 D4
48 D5
51 D6
52 D7
SHT 3 D4
SHT 3 D7

A8 74LS245 → UDB 0 104, UDB 1 100, UDB 2 98, UDB 3 37
A7 74LS245 → UDB 4 58, UDB 5 94, UDB 6 95, UDB 7 33
RCV+
TRANS-

A21 82S151 → 12 ENA, 11 DIR, 10, 9, 13

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES
PARTS LIST					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
3 PLACE DEC ± .010
2 PLACE DEC ± .02

SIGNATURE AND DATE
DRAWN
CHK'D
APVD

NEXT ASSY | USED ON
APPLICATION

ZILOG INC.
10460 BUBB ROAD CUPERTINO CALIFORNIA

TITLE LOGIC DIAGRAM, USER INTERFACE/MAPPER

SIZE D | DRAWING NO DZ-0104-02 | ISSUE 4
SCALE NONE | SHEET 2 OF 3

LTR	DESCRIPTION	DATE	APPROVED
4	SEE SHEET 1	2.19.78	

IORQ-
IORQ- 30
RFSH- 25
MRQ- 29
M1- 28
BUSAK- SHT 1
A15 7414
A30 7432
A1 74367
+5V
ADD15
ADD14
ADD13
ADD12
A11
A10
A09
A08
SHT 2
A13 2705 OR 9334
A18 1K
MAPDAT
A28 74125
PWEF-
IEO 1 81
IEO 2 87
IEO 3 89
A29 7410
A14 7414
A31 7432
INTA-
A36 7400
A33 7408
A32 7432
IMD TRAP-
D0 SHT 2
MAPDAT 73
IEK SHT 1
A07
A06
A05
A04
A03
A02
A01
A00
SHT 2
A16 7430
A17 74155
PREF-
PWEE-
PWEE+
D1 SHT 2
D2 SHT 2
D3 SHT 2
RD- 45
WR- 44
SHT 1 SENSE SW 2-
SHT 2 XCON-
A19 74367
A20 74LS175
D7 SHT
D4 SHT
USCPUN- SHT 1
MAPEN-
MAPOUT-
PORTS OUT- SHT 2
SYS MEM (ON)
MEMORY SW SW1
EXTERNAL
220
330
SENSE SW.1 117
SENSE.SW MEM- 106
(SENSE FB D4)
PWR ON CLR- 26
SHT 1
PORTS OUT-

ITEM	QTY	TYPE	ZILOG PART NO	DESCRIPTION	REF DES
PARTS LIST					

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ± 1°
FRACTIONS ± 1/64
2 PLACE DEC ± .010
3 PLACE DEC ± .005

CODE IDENT: 80708

SIGNATURE AND DATE
DRAWN Jerr 2-19-78
CHECKED
APVD JC Hunter 2-19-78

NEXT ASSY | USED ON | APPLICATION

ZILOG INC.
10123 BUBB ROAD CUPERTINO CALIFORNIA 95014

TITLE LOGIC DIAGRAM, USER INTERFACE / MAPPER

SIZE D | DRAWING NO D2-0104-02 | REV 4

SCALE | SHEET 3 OF 3

8 7 6 5 4 3 2 1

APPENDIX F

BREAKPOINT SCHEMATICS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	ECN 00315	4-18-8	AV

(J10-54) D0
(J10-55) D1
(J10-57) D2
(J10-56) D3
(J10-47) D4
(J10-48) D5
(J10-51) D6
(J10-52) D7
(MONITOR) (J10-111) MONITOR
(MONITOR) (J10-114) DATA STB

74367 A29
74367 A30

74175 A22
74175 A23

7486 A15
7486 A16

D1B → (SHTS 2,3,5)
D2B → (SHTS 2,3,5)
D3B → (SHTS 2,3,5)
D4B → (SHTS 2,4,5)
D5B → (SHTS 2,4,5)
D0B → (SHTS 2,3,5)
D6B → (SHTS 2,4,5)
D7B → (SHTS 2,4,5)
MONITOR B → (SHT 2,4)

$\overline{D0\ EQ}$ → (SHT 5)
$\overline{D1\ EQ}$ → (SHT 5)
$\overline{D2\ EQ}$ → (SHT 5)
$\overline{D3\ EQ}$ → (SHT 5)
$\overline{D4\ EQ}$ → (SHT 5)
$\overline{D5\ EQ}$ → (SHT 5)
$\overline{D6\ EQ}$ → (SHT 5)
$\overline{D7\ EQ}$ → (SHT 5)

(SHT 4) → $\overline{LOAD\ DATA}$
(SHT 5) → DATA BITS EQ
(SHT 3) → $\overline{CONTROL\ EQ}$

R1 1K +5V

7474 A10

DATA EQ → (SHT 4)
A → (SHT 2)

(J10 59) (J10-1)
(J10-60) (J10-2)
(J10-61) (J10-3)
(J10-120) (J10-62)
(J10-121) (J10-63)
(J10-122) (J10-64)

+5V
C1 22uf
C2 22uf
C3-C34 .1UF
GND

J-10

BREAKPOINT

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC ± ANGLES ±		
APPROVALS	DATE	
DRAWN Matin	4-12-76	
CHECKED		
J.C. Hater	4/13/76	

Zilog

SCALE	SIZE	DRAWING NO
NONE	C	DZ-0003-02
DO NOT SCALE DRAWING		SHEET 1 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A			

(SHT 3) → EN ADDR LSB

+5V — R3 470Ω

7404 A4

7485 A26 — 7485 A27 — 7485 A24 — 7485 A25

7400 A11 — 7400 A11 — 7408 A5

J10-10 A7
J10-9 A6
J10-21 A5
J10-20 A4
J10-19 A3
J10-18 A2
J10-17 A1
J10-16 AØ
J10-43 A15
J10-41 A14
J10-40 A13
J10-42 A12
J10-12 A11
J10-13 A10
J10-14 A9
J10-11 A8

(SHT4) → LOAD ADDR UPPER
(SHT4) → LOAD ADDR LOWER

74175 A19 — 74175 A20 — 74175 A17 — 74175 A18

+5V — R1 1K (REF) — +5V — R1 1K (REF)

EQUAL

(SHT 1) → D7B, D6B, D5B, D4B, D3B, D2B, D1B, DØB → (SHT 1)

7474 A3 — ADDR EQ → (SHT 4)

(SHT3) → CONTROL EQ

7408 A5

7414 A3 — B → (SHT 4)

(SHT 1) → A

(SHT3) → CONTROL EQ

(SHT 1) → MONITOR B

7485 (TYP)

BREAKPOINT

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS ±	DEC ±	ANGLES ±

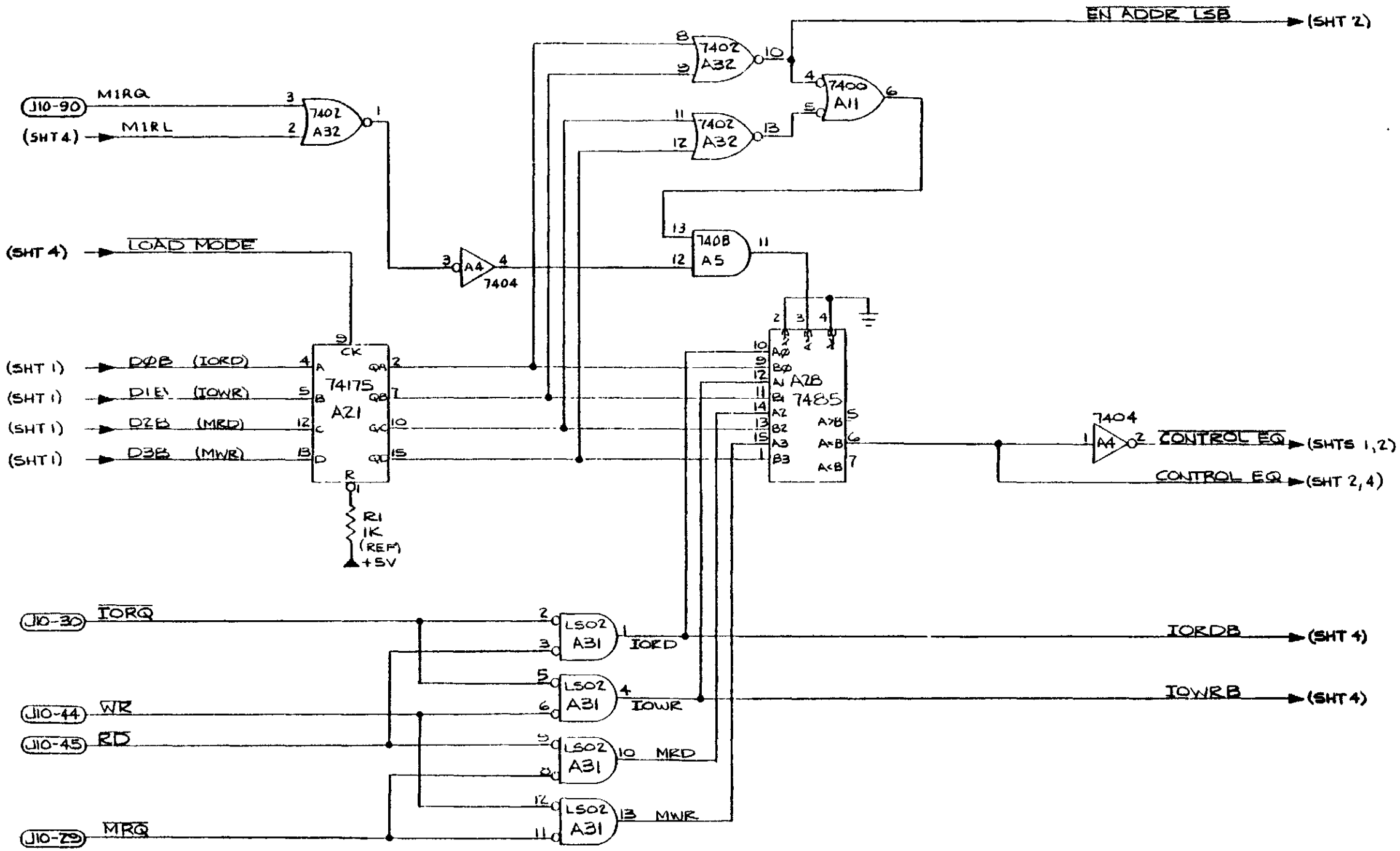
APPROVALS	DATE
DRAWN Malie	4-12-76
CHECKED	
JC Hayter	4/14/78

Zilog

SCALE	SIZE	DRAWING NO
NONE	C	02-0003-02

DO NOT SCALE DRAWING — SHEET 2 OF 5

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A			



BREAKPOINT

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN Mulia	4-12-76
CHECKED JC Hauser	4/19/78

Zilog

SCALE	SIZE	DRAWING NO
NONE	C	DZ-0003-02

DO NOT SCALE DRAWING — SHEET 3 OF 5

M

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A			

1 = Interrupt active

(SHT 3) → CONTROL EQ
(SHT 2) → ADDR EQ
(SHT 1) → DATA EQ
(SHT 2) → E

74151 A13

P/O A30
74367
BREAK → J10-100 MONITOR

7404 A4
SYNC → J10-101

7400 A11
7400 A6
7400 A6
7408 A5
7404 A4
BREAK STATUS → J10-85 MONITOR

J10-76 POWER ON CLR
CPU

(SHT 1) → DSB (SYNC/BK)
(SHT 1) → D6B (DATA)
(SHT 1) → D7B (ADDR-STB)
(SHT 1) → D4B

74175 A12

M1RL → (SHT 3)

+5V → R1 1K (REF)

(SHT 1) → MONITOR B

7402 A32
J10-15 BKPT SEL (DEV FB)
MONITOR

74161 A7

7442 A14

LOAD MODE → (SHT 3)
LOAD DATA → (SHT 1)
LOAD ADDR LOWER → (SHT 2)
LOAD ADDR UPPER → (SHT 2)
LOAD MASK → (SHT 5)

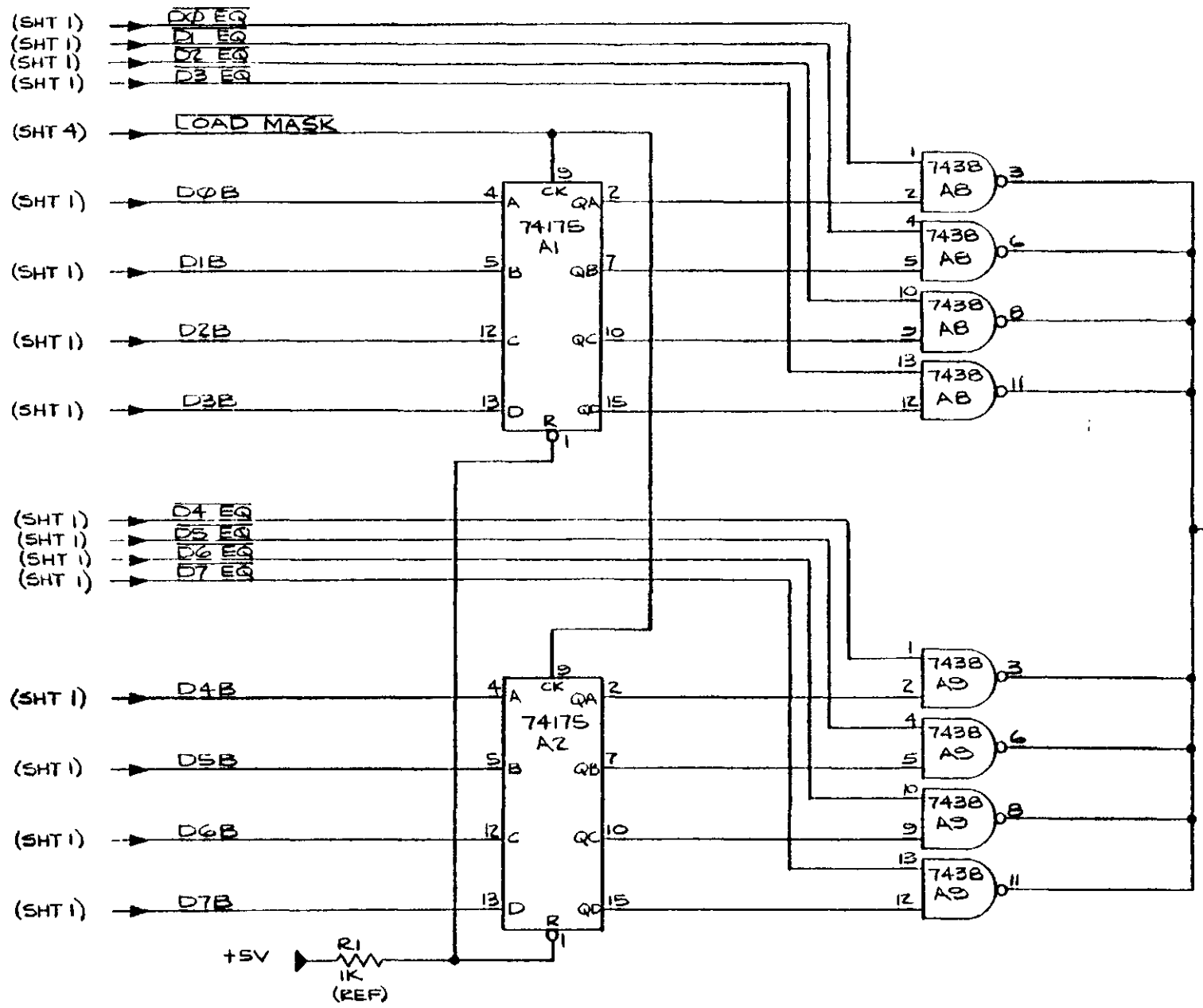
7400 A6
(SHT 3) → IOWRB

7400 A6
(SHT 3) → IORDB

BREAKPOINT

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± ± ±		Zilog
APPROVALS	DATE	CONFIDENTIAL This document is the property of Zilog Incorporated and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced or disclosed to third parties without the prior written consent of Zilog Incorporated
DRAWN Mallu	4-12-76	
CHECKED JC Hruler	4/19/76	SCALE NONE · SIZE C · DRAWING NO OZ-0003-02
		DO NOT SCALE DRAWING · SHEET 4 OF 5

REVISIONS			
LTR	DESCRIPTION	DA	APPROVED
A			



BREAKPOINT

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN Malia	4-13-76
CHECKED	
JC Walker	9/19/78

Zilog

SCALE	SIZE	DRAWING NO
NONE	C	DZ-0003-02

DO NOT SCALE DRAWING — SHEET 5 of 5

M

APPENDIX G

REAL TIME STORAGE MODULE SCHEMATICS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

(SHT 4) RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0 (SHT 4)

2101-1 A3 · 2101-1 A6 · 2101-1 A4 · 2101-1 A5

D7B D6B D5B D4B D3B D2B D1B D0B → (SHT 2)

(SHT 3) RD ADDR MSB
(SHT 3) RD ADDR LSB
+5V R1 1K REF
(SHT 3) WR DATA
(SHT 3) DATA STB B

74174 A11 · 74174 A12 · 74174 A13 (+5V, R2 1K)

J11-43 A15
J11-41 A14
J11-40 A13
J11-42 A12
J11-12 A11
J11-13 A10
J11-14 A9
J11-11 A8
J11-10 A7
J11-9 A6
J11-21 A5
J11-20 A4
J11-19 A3
J11-18 A2
J11-17 A1
J11-16 A0

J11-59 J11-1
J11-60 J11-2
J11-61 J11-3
J11-120 J11-62
J11-121 J11-63
J11-122 J11-64

C27 C26 C1-C25 .1UF +5V GND

74174 (TYP) CLR CK

2101-1 (TYP) DI1 DI2 DI3 DI4 DO1 DO2 DO3 DO4 CE2 CE1 R/W

GND - 8
Vcc - 22

RTSM J-11

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS ±	DEC ±	ANGLES ±

APPROVALS	DATE
DRAWN	4-19-76
CHECKED	

Zilog

SCALE	SIZE	DRAWING NO
NONE	C	DZ-0002-01

DO NOT SCALE DRAWING — SHEET 1 OF 4

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

(SHT 4) RA7 RA6 RA5 RA4 RA3 RA2 RA1 RA0 (SHT 4)

(SHT 1) D7B D6B D5B D4B D3B D2B D1B D0B (SHT 1)

2101-1 A1 · 2101-1 A8 · 2101-1 A2 · 2101-1 A7

D7B D6B D5B D4B D3B D2B D1B D0B → (SHT 3)

(SHT 3) RD DATA
(SHT 3) RD CONTROL

R1 1K +5V

(SHT 3) WR DATA

D3L D2L D1L D0L → (SHT 3)

(SHT 3) DATA STB B

R-3 1K +5V

74175 A18 · 74175 A23

7474 A14 · 7474 A14

R2 1K +5V

(SHT 3) D7 D6 D5 D4 D3 D2 D1 D0 IORDB IOWRB MRDB MWRB BUSAKB M1B

(SHT 2) J11-27 HALT A

(SHT 3) MONITOR B

2101-1 TYP

GND Vcc

RTSM

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS ± DEC ± ANGLES ±

APPROVALS	DATE
DRAWN Mario	4-19-76
CHECKED	

Zilog

CONFIDENTIAL
This document is the property of Zilog, Inc. and contains information which is confidential and proprietary to Zilog. No part of this document may be copied, reproduced, or disclosed to third parties without the prior written consent of Zilog, Incorporated.

SCALE NONE | SIZE C | DRAWING NO DZ-0002 01

DO NOT SCALE DRAWING | SHEET 2 OF 4

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

J11-50 RE RT
MONITOR

(SHT 2) D0L (IORD)
D1L (IOWR)
D2L (MRD)
(SHT 2) D3L (MWR)

74175 A19 — R-3 1K +5V

7400 A20 ×4 — 7430 A21 — 7400 A27 — WR DATA → (SHT 2,4)

BUSAK B → (SHT 2,4)

J11-22 BUSAK
J11-29 MRQ
J11-30 IORQ
J11-45 RD
J11-44 WR
J11-28 MI

74368 A24 — 7408 A25 ×4 — 7400 A27

MWR
MRD
IORD
IOWR
INT ACK

74175 A26 — R-4 1K +5V

MRW B → (SHT 2)
MRD B
IORD B
IOWR B
MIB → (SHT 2)

MONITOR
J11-111 MONITOR
J11-114 DATA STB
MONITOR

P/O 74367 A17

MONITOR B → (SHT 2,4)
DATA STB B → (SHT 1,2)

R-5 1K +5V

74161 A22 — 74155 A15

RD ADDR LSB → (SHT 1)
RD ADDR MSB → (SHT 1)
RD DATA → (SHT 2)
RD CONTROL → (SHT 2)

J11-66 STOR SEL (DEV PC)
MONITOR

7402 A28 — 7400 A27 ×2 — 7402 A28

READ → (SHT 4)

(SHT 2) D7B
D6B
D5B
D4B
D3B
D2B
D1B
(SHT 2) D0B

74367 P/O A17 — 74367 A16

D7	(SHT 2)	J11-52
D6	(SHT 2)	J11-51
D5	(SHT 2)	J11-48
D4	(SHT 2)	J11-47
D3	(SHT 2)	J11-56
D2	(SHT 2)	J11-57
D1	(SHT 2)	J11-55
D0	(SHT 2)	J11-54

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

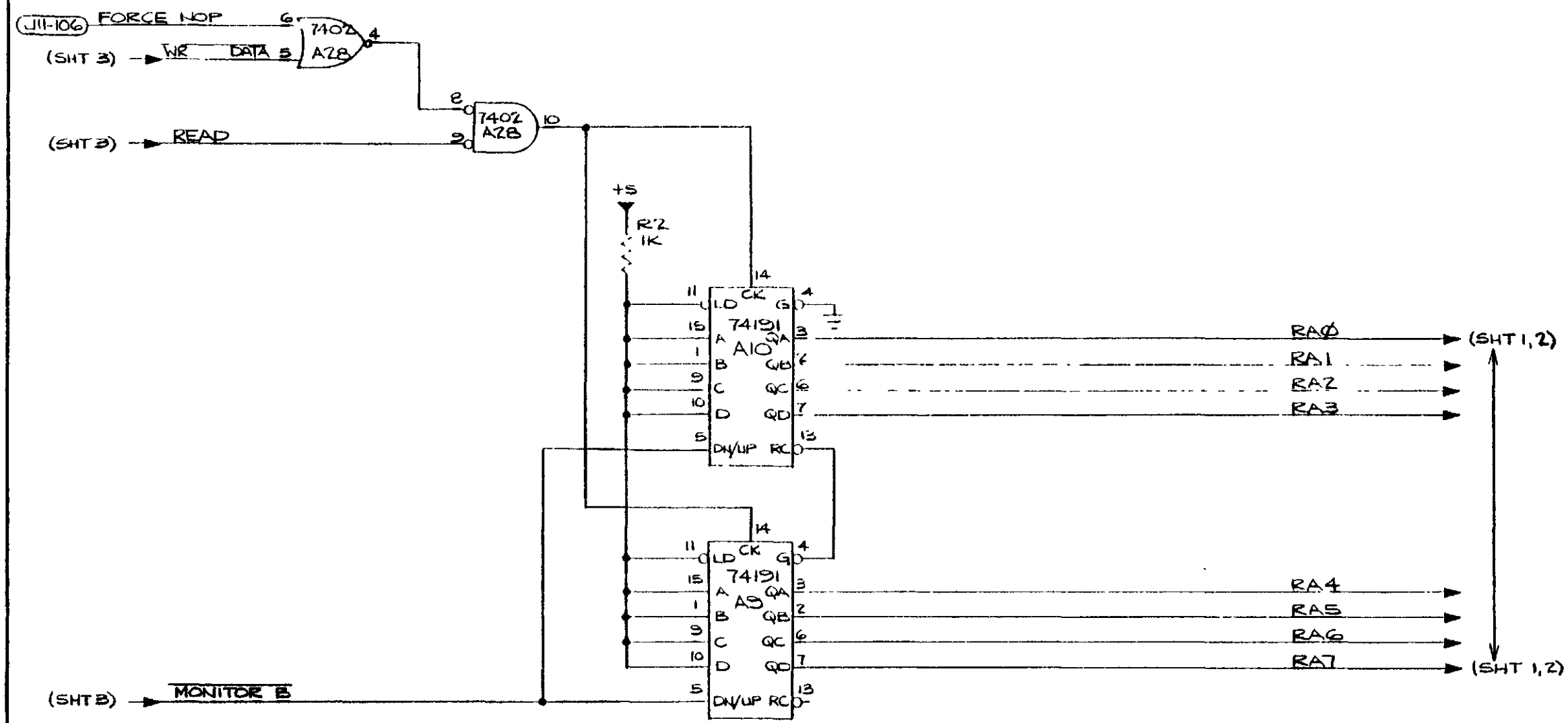
APPROVALS	DATE
DRAWN Mahir	4-21-76
CHECKED	

RTSM Zilog

SCALE	SIZE	DRAWING NO
NONE	C	DZ-0003-01

DO NOT SCALE DRAWING — SHEET 3 OF 4

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



RTSM

TOLERANCED UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN Linda L.	4-21-76
CHECKED	

Zilog

SCALE	SIZE	DRAWING NO
NONE	C	02-0002-01

DO NOT SCALE DRAWING — SHEET 4 OF 4

APPENDIX H

PCB LOCATIONS FOR THE ZDS-1/25

PCB LOCATION FOR THE ZDS-1/25

REVISION 1 9-1-78

CONNECTOR	PRINTED CIRCUIT BOARDS	
J01	09-0104-02	MAPPER-ICE
J02	09-0100-01	MONITOR.25
J03	09-0004-01	FLOPPY CONTROLLER
J04	09-0003-02	BREAKPOINT2
J05	09-0002-01	RTSM
	09-0109-01	RTSM2
J06	09-0099-01	CPU2
J07	09-0010-04	60K DYNAMIC RAM
	09-0101-04	60K MEMORY.25
	09-0045-01	16K STATIC RAM (CARD 0)
J08	09-0108-01	ZDSP
	09-0020-01	CIB
	09-0045-01	16K STATIC RAM (CARD 1)
J09	09-0108-01	ZDSP
	09-0031-02	PPB
	09-0070-01	PPB16
	09-0112-01	RXB
	09-0045-01	16K STATIC RAM (CARD 2)

I/O CONNECTORS

J13	FLOPPY DRIVE CABLE (50 PINS)
J14	CONSOLE CABLE
J15	AUXILIARY SERIAL CABLE
J16	USER INTERFACE CABLE #2
J17	USER INTERFACE CABLE #1
J18	SPARE (USER DEFINABLE)
J19	PROLOG PROM PROGRAMMER CABLE
J20	LINE PRINTER CABLE (ZDSP)
J21	FRONT PANEL CABLE
J25	POWER CABLE
J26	REMEX PUNCH-READER CABLE (50 PINS)

PCB Locations (cont.)

REAR PANEL CONNECTORS

J100	SYNC PULSE PLUG (BNC)
J101	REMEX PUNCH
J102	REMEX READER
J103	LINE PRINTER (ZDSP)
J104	PROLOG PROM PROGRAMMER
J105	USER INTERFACE CABLE #1
J106	USER INTERFACE CABLE #2
J107	AUXILIARY SERIAL PORT
J108	TERMINAL

INTERRUPT DAISY CHAIN

IEO.1	J06	CPU2 (CTC)
(IEO.1,2,3)	JO1	MAPPER-ICE
IEO.2	J08	CIB, ZDSP.1 (PIO PIO, CTC)
IEO.3	J09	ZDSP.2, PPB (PIO, CTC)

APPENDIX I

BACKPLANE DEFINITION FOR THE ZDS-1/25

BACKPLANE DEFINITION FOR THE ZDS-1/25

13-1084-02 REV. 1 9-1-78

```
SYSTEM=ZDS.1/25
GEOMETRY=10-0047.(ZDS-1/25)
SLOTS=

        J01     MICE.PIN

        J02     MONITOR.25.PIN

        J03     FLOPPY.PIN

        J04     BKPT2.PIN

        J05     RTSM2.PIN

        J06     CPU2.PIN

        J07     MEMORY.25.PIN           STATIC.MEMORY.PIN CARD=0

        J08     ZDSP.1.PIN              STATIC.MEMORY.PIN CARD=1
                REMEX.PIN               CIB.PIN         PIB.PIN

        J09     ZDSP.2.PIN              STATIC.MEMORY.PIN CARD=2
                PROM.PROG.DS.PIN

        J13     FLOPPY.CABLE.PIN

        J14     TTY.CABLE.PIN

        J15     ZDSP.CABLE.PIN

        J16     M.ICE.CABLE.2.PIN

        J17     M.ICE.CABLE.1.PIN

        J18     ZDSP.2.CABLE.PIN

        J19     PROLOG.CABLE.PIN

        J20     LP.CABLE.PIN

        J21     FRONT.PANEL.CABLE.PIN

        J25     POWER.CABLE.PIN
```

Backplane Definition (cont.)

```
        J26     REMEX.CABLE.PIN
                (REMEX.READER.CABLE.PIN)
                (REMEX.PUNCH.CABLE.PIN)
```

BACKPLANE DEFINITION FOR THE ZDS-1/25

13-1084-02 REV. 1 9-1-78

```
SYSTEM=ZDS.1/25
GEOMETRY=ZDS.1.GEO
NETS=

+05V.1.060
                J01-060
                J21-009
                J21-010

+05V.1.061
                J01-061
                J21-007
                J21-008

+12V.1
                J07-090
                J07-091
                J07-092
                J25-007

+12V.2
                J07-093
                J07-094
                J07-095
                J25-008

+12V.3
                J02-095
                J06-090
                J08-090
                J09-090
                J25-009

-05V.1
                J07-068
                J07-069
                J25-001

-05V.2
                J07-083
                J07-084
                J07-085
                J25-002
```

-5V.12

J02-098
J06-099
J08-107
J09-107
J25-003

8.PHI

J01-023
J03-023
J06-023

A00

J01-016
J02-016
J04-016
J05-016
J06-016
J07-016
J08-016
J09-016

A01

J01-017
J02-017
J04-017
J05-017
J06-017
J07-017
J08-017
J09-017

A02

J01-018
J02-018
J04-018
J05-018
J06-018
J07-018
J08-018
J09-018

Backplane Definition (Wire List) (cont.)

A03

J01-019
J02-019
J04-019
J05-019
J06-019
J07-019
J08-019
J09-019

A04

J01-020
J02-020
J04-020
J05-020
J06-020
J07-020
J08-020
J09-020

A05

J01-021
J02-021
J04-021
J05-021
J06-021
J07-021
J08-021
J09-021

A06

J01-009
J02-009
J04-009
J05-009
J06-009
J07-009
J08-009
J09-009

A07

J01-010
J02-010
J04-010
J05-010
J06-010
J07-010
J08-010
J09-010

A08

J01-011
J04-011
J05-011
J06-011
J07-011
J08-011
J09-011

A09

J01-014
J04-014
J05-014
J06-014
J07-014
J08-014
J09-014

A10

J01-013
J04-013
J05-013
J06-013
J07-013
J08-013
J09-013

A11

J01-012
J04-012
J05-012
J06-012
J07-012
J08-012
J09-012

A12

J01-042
J04-042
J05-042
J06-042

A12+

J06-068
J07-042

Backplane Definition (Wire List) (cont.)

A13

J01-040
J04-040
J05-040
J06-040

A13+

J06-066
J07-040

A14

J01-041
J04-041
J05-041
J06-041

A15

J01-043
J04-043
J05-043
J06-043

AA0.LP.RX

J08-073
J20-009
J26-011

AA1.LP.RX

J08-081
J20-010
J26-010

AA2.LP.RX

J08-078
J20-012
J26-032

AA3.LP.RX

J08-077
J20-013
J26-033

AA4.LP.RX

J08-076
J20-023
J26-012

AA5.LP.RX
- J08-075
- J20-024
- J26-013

AA6.RX
- J08-074
- J26-026

AA7.RX
- J08-087
- J26-027

AB0.D1.LP.RX
- J08-065
- J20-001
- J26-001

AB1.D2.LP.RX
- J08-066
- J20-002
- J26-002

AB2.D3.LP.RX
- J08-067
- J20-003
- J26-003

AB3.D4.LP.RX
- J08-068
- J20-004
- J26-004

AB4.D5.LP.RX
- J08-069
- J20-005
- J26-005

AB5.D6.LP.RX
- J08-070
- J20-006
- J26-006

AB6.D7.LP.RX
- J08-071
- J20-007
- J26-007

```
AB7.D8.LP.RX
                J08-072
                J20-008
                J26-008

ABS.LP
                J08-082
                J20-011

BA0.DIN.1.PP.RX
                J08-104
                J19-019
                J26-038

BA0.DOUT.1.PP
                J08-093
                J19-011

BA1.DIN.2.PP.RX
                J08-105
                J19-020
                J26-039

BA1.DOUT.2.PP
                J08-094
                J19-012

BA2.DIN.3.PP.RX
                J08-106
                J19-017
                J26-040

BA2.DOUT.3.PP
                J08-095
                J19-007

BA3.DIN.4.PP.RX
                J08-110
                J19-018
                J26-041

BA3.DOUT.4.PP
                J08-096
                J19-009

BA4.DIN.5.PP.RX
                J08-111
                J19-023
                J26-042
```

```
BA4.DOUT.5.PP
                J08-097
                J19-010

BA5.DIN.6.PP.RX
                J08-113
                J19-024
                  J26-043

BA5.DOUT.6.PP
                J08-098
                J19-013

BA6.DIN.7.PP.RX
                J08-114
                J19-021
                J26-044

BA6.DOUT.7.PP
                J08-099
                J19-006

BA7.DIN.8.PP.RX
                J08-115
                J19-022
                J26-045

BA7.DOUT.8.PP
                J08-101
                J19-008

BAR.PP.RX
                J08-119
                J19-002
                J26-047

BB0.PP.RX
                J08-117
                J19-015
                J26-046

BB1.PP.RX
                J08-118
                J19-014
                J26-014

BB2.PP
                J08-116
                J19-016
```

BB5.PP.RX
J08-102
J19-003
J26-015

BB6.PP.RX
J08-103
J19-005
J26-016

BB7.RX
J08-058
J26-017

BKPT.SEL-
J02-070
J04-015

BNMI.SW-
J01-113
J21-018

BREAK-
J02-102
J04-100

BREAK.STATUS
J02-116
J04-085

BREAK.SYNC
J04-101
J21-003

BUSAK-
J01-022
J05-022
J06-022

BUSRQ-
J01-107
J06-107

CARRIER.DETECT
J08-040
J15-008

CARRIER.DETECT.2
J09-040
J18-008

CD.0-

J06-038
J07-038

CD.1-

J06-037
J07-037
J08-038

CD.2-

J06-036
J07-036
J09-038

CD.3-

J06-035
J07-035

D0

J01-054
J02-054
J03-054
J04-054
J05-054
J06-054
J07-054
J08-054
J09-054

D1

J01-055
J02-055
J03-055
J04-055
J05-055
J06-055
J07-055
J08-055
J09-055

D2

J01-057
J02-057
J03-057
J04-057
J05-057
J06-057
J07-057
J08-057
J09-057

D3

J01-056
J02-056
J03-056
J04-056
J05-056
J06-056
J07-056
J08-056
J09-056

D4

J01-047
J02-047
J03-047
J04-047
J05-047
J06-047
J07-047
J08-047
J09-047

D5

J01-048
J02-048
J03-048
J04-048
J05-048
J06-048
J07-048
J08-048
J09-048

D6

J01-051
J02-051
J03-051
J04-051
J05-051
J06-051
J07-051
J08-051
J09-051

D7
J01-052
J02-052
J03-052
J04-052
J05-052
J06-052
J07-052
J08-052
J09-052

DATA.STB
J02-101
J04-114
J05-114

DIRECTION.F
J03-027
J13-042

DISK.CONTROL.A.PORT-
J02-069
J03-117

DISK.CONTROL.B.PORT-
J02-068
J03-118

DISK.DATA.PORT-
J02-067
J03-116

EXT.PHI
J01-066
J06-058

FORCE.NOP
J02-106
J05-106
J06-106

FORCE.NOP.DLYD
J02-037
J05-037

GND.1.062
J01-062
J16-024
J16-025
J17-025

Backplane Definition (Wire List) (cont.)

GND.1.063
- J01-063
- J16-022
- J16-023

GND.1.064
- J01-064
- J16-020
- J16-021

GND.1.120
- J01-084
- J01-085
- J01-120
- J21-024

GND.1.121
- J01-121
- J21-006
- J21-013

GND.1.122
- J01-122
- J21-001
- J21-002

GND.2.062
- J02-025
- J16-019

GND.2.120
- J02-120
- J15-007
- J18-007

GND.2.121
- J02-121
- J19-025
- J20-020

GND.2.122
- J02-122
- J20-018
- J20-019

GND.3.062
- J03-062
- J13-021
- J13-022
- J13-023
- J13-024
- J13-025

GND.3.063
- J03-063
- J13-016
- J13-017
- J13-018
- J13-019
- J13-020

GND.3.064
- J03-064
- J13-011
- J13-012
- J13-013
- J13-014
- J13-015

GND.4.062
- J04-062
- J26-024
- J26-025

GND.4.063
- J04-063
- J26-028
- J26-029

GND.4.064
- J04-064
- J26-030
- J26-037

GND.5.062
- J05-062
- J26-050

GND.5.063
- J05-063
- J26-049

GND.5.064
- J05-064
- J26-048

HALT-
J01-027
J02-027
J05-027
J06-027

HALT.LAMP-
J02-005
J21-020

IE*
J01-112
J02-096

IEO.1
J01-081
J06-079
J08-088

IEO.2
J01-082
J08-112
J09-088

IEO.3
J01-083
J09-112

INDX
J03-007
J06-078

INDX.0-
J03-015
J13-035

INT-
J01-109
J06-109
J08-109
J09-109

IORQ-
J01-030
J02-030
J03-030
J04-030
J05-030
J06-030
J08-030
J09-030

LOCAL.MODE
J08-092
J15-010

LOCAL.MODE.2
J09-092
J18-010

M1-
J01-028
J02-028
J04-028
J05-028
J06-028
J08-028
J09-028

M1RQ
J02-090
J04-090

MDIS-
J06-039
J07-039
J08-039
J09-039

MONITOR
J01-046
J02-110
J06-046

MONITOR-
J02-111
J04-111
J05-111

MONITOR.LAMP-
J02-006
J21-022

MONTR.NC
J02-082
J21-026

MONTR.NO
J02-083
J21-025

MRD-
J02-076
J07-046
J08-046
J09-046

MRQ-
J01-029
J02-029
J04-029
J05-029
J06-029
J07-029
J08-029
J09-029

NMI-
J01-110
J06-110

ORIGINATE.MODE
J08-091
J15-009

ORIGINATE.MODE.2
J09-091
J18-009

PHI
J01-024
J02-024
J06-024
J08-024
J09-024

POWER.ON.CLR-
J01-026
J02-026
J04-026
J06-026
J08-026
J09-026

PS.0-
J06-034
J07-034
J08-034
J09-034

PS.1-
J06-033
J07-033
J08-033
J09-033

PS.2-
J06-032
J07-032
J08-032
J09-032

PS.3-
J06-031
J07-031
J08-031
J09-031

RCV.CLK
J06-006
J06-007

RCVR.OUT-
J06-004
J06-077

RD-
J01-045
J02-045
J03-045
J04-045
J05-045
J06-045
J08-045
J09-045

RDY-
J03-016
J13-036

READ.DATA-
J03-009
J13-048

REFRESH-
J01-025
J06-025
J07-025

RESET.SW-
J06-049
J21-019

RESTART-
J01-050
J02-050
J06-050

RESTART.D-
J02-011
J05-050

RING.IND
J08-089
J15-022

RING.IND.2
J09-089
J18-022

RS232.DATA.IN
J02-093
J14-002

RS232.DATA.OUT
J02-086
J14-003

RS232.RETURN
J02-091
J14-007

S2.46MHZ
J01-058
J06-115

SEL.0-
J03-018
J13-038

SEL.1-
J03-084
J13-039

SENSE.SW.1+
J01-116
J21-004

SENSE.SW.1-
J01-117
J21-015

SENSE.SW.2+
J01-114
J21-016

SENSE.SW.2-
J01-115
J21-014

SENSE.SW.CLK
J01-105
J02-118

SENSE.SW.MEM
J01-106
J02-117

SERIAL.IN
J02-087
J06-008

SERIAL.OUT
J02-085
J06-015

STEP-
J03-028
J13-043

STOR.SEL-	
	J02-066
	J05-066
SYNC	
	J08-049
	J15-024
SYNC.2	
	J09-049
	J18-024
SYS.RESET-	
	J02-046
	J03-053
	J06-053
	J08-053
TCTS	
	J08-007
	J15-005
TCTS.2	
	J09-007
	J18-005
TDSR	
	J08-008
	J15-006
TDSR.2	
	J09-008
	J18-006
TDTR	
	J08-050
	J15-020
TDTR.2	
	J09-050
	J18-020
TERM.BUSY	
	J08-025
	J15-025
TERM.BUSY.2	
	J09-025
	J18-025

TRK.00-
J03-011
J13-046

TRTS
J08-006
J15-004

TRTS.2
J09-006
J18-004

TRXD
J08-005
J15-003

TRXD.2
J09-005
J18-003

TTXD
J08-004
J15-002

TTXD.2
J09-004
J18-002

TTY.DATA.IN
J02-092
J14-010

TTY.DATA.OUT
J02-084
J14-016

TTY.IN.RETURN
J02-097
J14-005
J14-006
J14-008
J14-024

TTY.OUT.RETURN
J02-099
J14-017

UA00
J01-074
J17-001

UA01	
	J01-075
	J17-014
UA02	
	J01-076
	J17-002
UA03	
	J01-087
	J17-015
UA04	
	J01-086
	J17-003
UA05	
	J01-088
	J17-016
UA06	
	J01-090
	J17-004
UA07	
	J01-091
	J17-017
UA08	
	J01-031
	J17-005
UA09	
	J01-032
	J17-018
UA10	
	J01-092
	J17-006
UA11	
	J01-093
	J17-019
UA12	
	J01-035
	J17-007

UA13
J01-036
J17-020

UA14
J01-096
J17-008

UA15
J01-097
J17-021

UB.CONT-
J01-111
J02-075

UBREQ-
J01-071
J16-014

UBUSAK-
J01-103
J16-003

UDB0
J01-104
J17-009

UDB1
J01-100
J17-022

UDB2
J01-098
J17-010

UDB3
J01-037
J17-023

UDB4
J01-038
J17-011

UDB5
J01-094
J17-024

UDB6
J01-095
J17-012

UDB7
J01-033
J17-013

UHALT-
J01-101
J16-016

UIE
J01-049
J16-015

UINT-
J01-007
J16-018

UIORQ-
J01-065
J16-012

UM1-
J01-068
J16-017

UMEM-
J01-073
J16-001

UMRQ-
J01-004
J16-011

UNMI-
J01-069
J16-005

UPHI
J01-102
J16-013

URD-
J01-005
J16-010

URFSH-
J01-067
J16-004

URST-
J01-072
J16-007

USER.LAMP-
J02-008
J21-021

USER.MEM.ENABLE-
J01-070
J02-053

USER.NC
J02-077
J21-012

USER.NO
J02-078
J21-011

UWAIT-
J01-008
J16-006

UWR-
J01-006
J16-009

WAIT-
J01-108
J02-108
J03-108
J06-108

WAIT.LAMP-
J02-007
J21-023

```
WR-
                    J01-044
                    J02-044
                    J03-044
                    J04-044
                    J05-044
                    J06-044
                    J07-044
                    J08-044
                    J09-044

WR.DATA-
                    J03-006
                    J13-044

WR.PROT.0-
                    J03-013
                    J13-047

WRITE.GATE-
                    J03-025
                    J13-045
```

APPENDIX J

PINOUT CHARTS

CONTENTS

PINOUT FOR "MICE" BOARD - #09-0104-02

J01

PIN #	SIGNAL NAME
001	(+05V.1.001)
002	(+05V.1.002)
003	(+05V.1.003)
004	UMRQ-
005	URD-
006	UWR-
007	UINT-
008	UWAIT-
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	BUSAK-
023	8.PHI
024	PHI
025	REFRESH-
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	UA08
032	UA09
033	UDB7
034	.
035	UA12
036	UA13
037	UDB3
038	UDB4
039	.
040	A13
041	A14
042	A12

Pinout for MICE Board (cont.)

043	A15
044	WR-
045	RD-
046	MONITOR
047	D4
048	D5
049	UIE
050	RESTART-
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	S2.46MHZ
059	(+05V.1.059)
060	+05V.1.060
061	+05V.1.061
062	GND.1.062
063	GND.1.063
064	GND.1.064
065	UIORQ-
066	EXT.PHI
067	URFSH-
068	UM1-
069	UNMI-
070	USER.MEM.ENABLE-
071	UBREQ-
072	URST-
073	UMEM-
074	UA00
075	UA01
076	UA02
077	.
078	.
079	.
080	.
081	IEO.1
082	IEO.2
083	IEO.3
084	GND.1.120
085	GND.1.120
086	UA04
087	UA03
088	UA05
089	.
090	UA06
091	UA07
092	UA10

Pinout for MICE Board (cont.)

093	UA11
094	UDB5
095	UDB6
096	UA14
097	UA15
098	UDB2
099	.
100	UDB1
101	UHALT-
102	UPHI
103	UBUSAK-
104	UDB0
105	SENSE.SW.CLK (OUTPUT LEVEL)
106	SENSE.SW.MEM (OUTPUT LEVEL)
107	BUSRQ-
108	WAIT-
109	INT-
110	NMI-
111	UB.CONT-
112	IE*
113	BNMI.SW- (NMI OR "BREAK" BUTTON)
114	SENSE.SW.2+ (ENABLE SW.EXTERNAL CLOCK)
115	SENSE.SW.2- (ENABLE SW.INTERNAL CLOCK)
116	SENSE.SW.1+ (ENABLE SW.EXTERNAL MEMORY)
117	SENSE.SW.1- (ENABLE SW.INTERNAL MEMORY)
118	.
119	.
120	GND.1.120
121	GND.1.121
122	GND.1.122

PINOUT FOR "MONITOR.25" BOARD - #09-0100-01

J02

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	HALT.LAMP-
006	MONITOR.LAMP-
007	WAIT.LAMP-
008	USER.LAMP-
009	A06
010	A07
011	RESTART.D-
012	(TY.HI)
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	GND.2.062
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	FORCE.NOP.DLYD
038	.
039	.
040	.
041	.
042	.
043	.

```
044     WR-
045     RD-
046     SYS.RESET-
047     D4
048     D5
049     .
050     RESTART-
051     D6
052     D7
053     USER.MEM.ENABLE-
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     (GND.2.062)
063     (GND.2.063)
064     (GND.2.064)
065     .
066     STOR.SEL-
067     DISK.DATA.PORT-
068     DISK.CONTROL.B.PORT-
069     DISK.CONTROL.A.PORT-
070     BKPT.SEL-
071     .
072     .
073     .
074     .
075     UB.CONT-
076     MRD-
077     USER.NC
078     USER.NO
079     (SPARE.SEL-)
080     (CTC.CARD.SEL-)
081     .
082     MONTR.NC
083     MONTR.NO
084     TTY.DATA.OUT
085     SERIAL.OUT
086     RS232.DATA.OUT
087     SERIAL.IN
088     .
089     (M1S-)
090     M1RQ (M1 ^ MREQ)
091     RS232.RETURN
092     TTY.DATA.IN
093     RS232.DATA.IN
```

094	.
095	+12V.3
096	IE*
097	TTY.IN.RETURN
098	-5V.12
099	TTY.OUT.RETURN
100	(RFI)
101	DATA.STB
102	BREAK-
103	.
104	.
105	.
106	FORCE.NOP
107	.
108	WAIT-
109	.
110	MONITOR
111	MONITOR-
112	.
113	.
114	.
115	(PHI.B.CLOCK.BUFFERED)
116	BREAK.STATUS
117	SENSE.SW.MEM (PORT FE D4)
118	SENSE.SW.CLK (PORT FE D1,D3)
119	.
120	GND.2.120
121	GND.2.121
122	GND.2.122

PINOUT FOR "FLOPPY.PIN" BOARD - #09-0004-01

J03

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	WR.DATA-
007	INDX
008	(WR.PROT.1-)
009	READ.DATA-
010	(TRK.01-)
011	TRK.00-
012	(DOOR.OPEN-)
013	WR.PROT.0-
014	(INDX.1-)
015	INDX.0-
016	RDY-
017	(CURRENT-)
018	SEL.0-
019	(LOAD.HEAD.1-)
020	(STEP.OUT.1-)
021	(WRITE.1-)
022	(STEP.IN.1-)
023	8.PHI.(8X.SYSTEM.CLOCK)
024	.
025	WRITE.GATE-
026	.
027	DIRECTION.F
028	STEP-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.

044	WR-
045	RD-
046	.
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	SYS.RESET-
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	GND.3.062
063	GND.3.063
064	GND.3.064
065	.
066	.
067	.
068	.
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	(GND)
083	(GND)
084	SEL.1-
085	(GND)
086	.
087	(LOAD.HEAD.0-)
088	.
089	.
090	.
091	.
092	.
093	.

```
094       .
095       .
096       .
097       .
098       .
099       .
100       .
101       .
102       .
103       .
104       .
105       .
106       .
107       .
108       WAIT-
109       .
110       .
111       .
112       .
113       .
114       .
115       .
116       DISK.DATA.PORT-
117       DISK.CONTROL.A.PORT-
118       DISK.CONTROL.B.PORT-
119       .
120       (GND.3.120)
121       (GND.3.121)
122       (GND.3.122)
```

PINOUT FOR "BREAKPOINT2" BOARD - #09-0003-02

J04

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	BKPT.SEL-
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	.
025	.
026	POWER.ON.CLR-
027	.
028	M1-
029	MRQ-
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	A13
041	A14
042	A12
043	A15

```
044     WR-
045     RD-
046     .
047     D4
048     D5
049     .
050     .
051     D6
052     D7
053     .
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     GND.4.062
063     GND.4.063
064     GND.4.064
065     .
066     .
067     .
068     .
069     .
070     .
071     .
072     .
073     .
074     .
075     .
076     .
077     .
078     .
079     .
080     .
081     .
082     .
083     .
084     .
085     BREAK.STATUS
086     .
087     .
088     .
089     .
090     M1RQ (M1 ^ MREQ FROM MONITOR)
091     .
092     .
093     .
```

```
094     .
095     .
096     .
097     .
098     .
099     .
100     BREAK-
101     BREAK.SYNC
102     .
103     .
104     .
105     .
106     .
107     .
108     .
109     .
110     .
111     MONITOR-
112     .
113     .
114     DATA.STB
115     .
116     .
117     .
118     .
119     .
120     (GND.4.120)
121     (GND.4.121)
122     (GND.4.122)
```

PINOUT FOR "RTSM2" BOARD - #09-0109-01

J05

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	BUSAK-
023	.
024	.
025	.
026	.
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	FORCE.NOP.DLYD
038	.
039	.
040	A13
041	A14
042	A12
043	A15

044	WR-
045	RD-
046	.
047	D4
048	D5
049	.
050	RESTART.D-
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	GND.5.062
063	GND.5.063
064	GND.5.064
065	.
066	STOR.SEL-
067	.
068	.
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	.
083	.
084	.
085	.
086	.
087	.
088	.
089	.
090	.
091	.
092	.
093	.

```
094     .
095     .
096     .
097     .
098     .
099     .
100     .
101     .
102     .
103     .
104     .
105     .
106     FORCE.NOP
107     .
108     .
109     .
110     .
111     MONITOR-
112     .
113     .
114     DATA.STB
115     .
116     .
117     .
118     .
119     .
120     (GND.5.120)
121     (GND.5.121)
122     (GND.5.122)
```

PINOUT FOR "CPU2.PIN" - 09-0099-01

J06

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	RCVR.OUT-
005	(SERIAL.OUT CPU0)
006	RCV.CLK
007	RCV.CLK (XMIT.CLK)
008	SERIAL.IN
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	SERIAL.OUT
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	BUSAK-
023	8.PHI.(8X.SYSTEM.CLOCK)
024	PHI.(SYSTEM.CLOCK)
025	REFRESH-
026	POWER.ON.CLR-
027	HALT-
028	M1-
029	MRQ-
030	IORQ-
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	CD.3-
036	CD.2-
037	CD.1-
038	CD.0-
039	MDIS-
040	A13
041	A14
042	A12
043	A15

044	WR-
045	RD-
046	MONITOR
047	D4
048	D5
049	RESET.SW-
050	RESTART-
051	D6
052	D7
053	SYS.RESET-
054	D0
055	D1
056	D3
057	D2
058	EXT.PHI.(EXTERNAL.SYSTEM.CLOCK)
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.6.062)
063	(GND.6.063)
064	(GND.6.064)
065	.
066	A13+
067	(SYSTEM.MEMORY)
068	A12+
069	.
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	RCVR.OUT-
078	INDX. (EN-CLK0)
079	IEO.1
080	.
081	.
082	.
083	(GND)
084	(GND)
085	(GND)
086	(GND)
087	(GND)
088	.
089	.
090	+12V.3
091	.
092	.
093	.

094	.
095	.
096	.
097	.
098	.
099	-5V.12
100	.
101	.
102	.
103	.
104	.
105	.
106	FORCE.NOP
107	BUSRQ-
108	WAIT-
109	INT-
110	NMI-
111	.
112	.
113	.
114	.
115	S2.46MHZ
116	.
117	.
118	.
119	.
120	(GND.6.120)
121	(GND.6.121)
122	(GND.6.122)

PINOUT FOR <MEMORY.25.PIN> 09-0101-04

J07

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	.
025	REFRESH-
026	.
027	.
028	.
029	MRQ-
030	.
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	CD.3-
036	CD.2-
037	CD.1-
038	CD.0-
039	MDIS-
040	A13+
041	.
042	A12+
043	.

044	WR-
045	.
046	MRD-
047	D4
048	D5
049	.
050	.
051	D6
052	D7
053	.
054	D0
055	D1
056	D3
057	D2
058	.
059	(+05V.PRINTED.DISTRIBUTION)
060	(+05V.PRINTED.DISTRIBUTION)
061	(+05V.PRINTED.DISTRIBUTION)
062	(GND.7.062)
063	(GND.7.063)
064	(GND.7.064)
065	.
066	.
067	.
068	-05V.1
069	-05V.1
070	.
071	.
072	.
073	.
074	.
075	.
076	.
077	.
078	.
079	.
080	.
081	.
082	.
083	-05V.2
084	-05V.2
085	-05V.2
086	.
087	.
088	.
089	.
090	+12V.1
091	+12V.1
092	+12V.1
093	+12V.2

094	+12V.2
095	+12V.2
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	.
108	.
109	.
110	.
111	.
112	.
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.7.120)
121	(GND.7.121)
122	(GND.7.122)

PINOUT FOR "STATIC.MEMORY.PIN" BOARD - 09-0045-01

J07 (S0) J08 (S1) J09 (S2)

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	A08
012	A11
013	A10
014	A09
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	.
025	.
026	.
027	.
028	.
029	MRQ-
030	.
031	PS.3-
032	PS.2-
033	PS.1-
034	PS.0-
035	.
036	.
037	.
038	CD.[#CARD]-.(ONE.OF.CD.0-.TO.CD.3-)
039	MDIS-
040	.
041	.
042	.
043	.

```
044     WR-
045     .
046     MRD-
047     D4
048     D5
049     .
050     .
051     D6
052     D7
053     .
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     (GND.8.062)
063     (GND.8.063)
064     (GND.8.064)
065     .
066     .
067     .
068     .
069     .
070     .
071     .
072     .
073     .
074     .
075     .
076     .
077     .
078     .
079     .
080     .
081     .
082     .
083     .
084     .
085     .
086     .
087     .
088     .
089     .
090     .
091     .
092     .
093     .
```

```
094     .
095     .
096     .
097     .
098     .
099     .
100     .
101     .
102     .
103     .
104     .
105     .
106     .
107     .
108     .
109     .
110     .
111     .
112     .
113     .
114     .
115     .
116     .
117     .
118     .
119     .
120     (GND.8.120)
121     (GND.8.121)
122     (GND.8.122)
```

PINOUT FOR "ZDSP" BOARD - 09-0108-01

J09

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	TTXD
005	TRXD
006	TRTS
007	TCTS
008	TDSR
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	TERM.BUSY
026	POWER.ON.CLR-
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	CARRIER.DETECT
041	.
042	.
043	.

```
044     WR-
045     RD-
046     .
047     D4
048     D5
049     SYNC
050     TDTR
051     D6
052     D7
053     .
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.4.PRINTED.DISTRIBUTION)
062     (GND.9.062)
063     (GND.9.063)
064     (GND.9.064)
065     AB0.D1.LP.RX  (LP.DATA.1  RXP.DATA.1)
066     AB1.D2.LP.RX
067     AB2.D3.LP.RX
068     AB3.D4.LP.RX
069     AB4.D5.LP.RX
070     AB5.D6.LP.RX
071     AB6.D7.LP.RX
072     AB7.D8.LP.RX
073     AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
074     .
075     AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
076     AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
077     AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
078     AA2.LP.RX (LP.FAULT- RXP.ERROR)
079     .
080     .
081     AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
082     ABS.LP (LP ACKNOWLEDGE-)
083     .
084     .
085     .
086     .
087     .
088     IEO.1 (BOARD IEI)
089     RING.IND
090     +12V.3
091     ORIGINATE.MODE
092     LOCAL.MODE
093     .
```

094	.
095	.
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	-5V.12
108	.
109	INT-
110	.
111	.
112	IEO.2 (BOARD IEO)
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.9.120)
121	(GND.9.121)
122	(GND.9.122)

PINOUT FOR "ZDSP.2" BOARD - 09-0108-01

J09

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	TTXD.2
005	TRXD.2
006	TRTS.2
007	TCTS.2
008	TDSR.2
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	TERM.BUSY.2
026	POWER.ON.CLR-
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	CARRIER.DETECT.2
041	.
042	.
043	.

```
044     WR-
045     RD-
046     .
047     D4
048     D5
049     SYNC.2
050     TDTR.2
051     D6
052     D7
053     .
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.4.PRINTED.DISTRIBUTION)
062     (GND.9.062)
063     (GND.9.063)
064     (GND.9.064)
065     (AB0.D1.LP.RX   (LP.DATA.1   RXP.DATA.1)
066     (AB1.D2.LP.RX
067     (AB2.D3.LP.RX
068     (AB3.D4.LP.RX
069     (AB4.D5.LP.RX
070     (AB5.D6.LP.RX
071     (AB6.D7.LP.RX
072     (AB7.D8.LP.RX
073     (AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
074     .
075     (AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
076     (AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
077     (AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
078     (AA2.LP.RX (LP.FAULT- RXP.ERROR)
079     .
080     .
081     (AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
082     (ABS.LP (LP ACKNOWLEDGE-)
083     .
084     .
085     .
086     .
037     .
088     IEO.2 (BOARD IEI)
089     RING.IND.2
090     +12V.3
091     ORIGINATE.MODE.2
092     LOCAL.MODE.2
093     .
```

094	.
095	.
096	.
097	.
098	.
099	.
100	.
101	.
102	.
103	.
104	.
105	.
106	.
107	-5V.12
108	.
109	INT-
110	.
111	.
112	IEO.3 (BOARD IEO)
113	.
114	.
115	.
116	.
117	.
118	.
119	.
120	(GND.9.120)
121	(GND.9.121)
122	(GND.9.122)

PINOUT FOR "CIB" BOARD - 09-0020-01

J08

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.

```
044     .
045     RD-
046     .
047     D4
048     D5
049     .
050     .
051     D6
052     D7
053     SYS.RESET-
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     (GND.9.062)
063     (GND.9.063)
064     (GND.9.064)
065     AB0.D1.LP.RX  (LP.DATA.1  RXP.DATA.1)
066     AB1.D2.LP.RX
067     AB2.D3.LP.RX
068     AB3.D4.LP.RX
069     AB4.D5.LP.RX
070     AB5.D6.LP.RX
071     AB6.D7.LP.RX
072     AB7.D8.LP.RX
073     AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
074     AA6.RX (RXP.INPUT.MODE.SELECT)
075     AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
076     AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
077     AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
078     AA2.LP.RX (LP.FAULT- RXP.ERROR)
079     (ABR)
080     .
081     AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
082     ABS.LP (LP.ACKNOWLEDGE-)
083     (AAR)
084     (AAS)
085     .
086     .
087     AA7.RX (RXP.OUTPUT.MODE.SELECT)
088     IEO.1 (CARD IEI)
089     .
090     .
091     .
092     .
093     BA0.DOUT.1.PP (PROLOG.DATA.OUT.1)
```

```
094     BA1.DOUT.2.PP
095     BA2.DOUT.3.PP
096     BA3.DOUT.4.PP
097     BA4.DOUT.5.PP
098     BA5.DOUT.6.PP
099     BA6.DOUT.7.PP
100     .
101     BA7.DOUT.8.PP
102     BB5.PP.RX (PROLOG.MODE RXR.EXTERNAL.INHIBIT)
103     BB6.PP.RX (PROLOG.INTERLOCK RXR.DRIVE.RIGHT)
104     BA0.DIN.1.PP.RX (PROLOG.DATA.IN.1  RXB.DATA.IN.1
105     BA1.DIN.2.PP.RX
106     BA2.DIN.3.PP.RX
107     .
108     .
109     INT-
110     BA3.DIN.4.PP.RX
111     BA4.DIN.5.PP.RX
112     IEO.2 (CARD IEO)
113     BA5.DIN.6.PP.RX
114     BA6.DIN.7.PP.RX
115     BA7.DIN.8.PP.RX
116     BB2.PP (PROLOG.RESPONSE)
117     BB0.PP.RX (PROLOG.ADDRESS RXR.DATA.READY)
118     BB1.PP.RX (PROLOG.ERROR RXR.RDR.RDY)
119     BAR.PP.RX (PROLOG.TRANSFER RXR.OUTPUT.MODE)
120     (GND.9.120)
121     (GND.9.121)
122     (GND.9.122)
```

PINOUT FOR "PIB" BOARD - 09-0020-02

J08

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.

```
044     .
045     RD-
046     .
047     D4
048     D5
049     .
050     .
051     D6
052     D7
053     SYS.RESET-
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     (GND.9.062)
063     (GND.9.063)
064     (GND.9.064)
065     AB0.D1.LP.RX   (LP.DATA.1   RXP.DATA.1)
066     AB1.D2.LP.RX
067     AB2.D3.LP.RX
068     AB3.D4.LP.RX
069     AB4.D5.LP.RX
070     AB5.D6.LP.RX
071     AB6.D7.LP.RX
072     AB7.D8.LP.RX
073     AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
074     AA6.RX (RXP.INPUT.MODE.SELECT)
075     AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
076     AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
077     AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
078     AA2.LP.RX (LP.FAULT- RXP.ERROR)
079     (ABR)
080     .
081     AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
082     ABS.LP (LP.ACKNOWLEDGE-)
083     (AAR)
084     (AAS)
085     .
086     .
087     AA7.RX (RXP.OUTPUT.MODE.SELECT)
088     IEO.1 (CARD IEI)
089     .
090     .
091     .
092     .
093     BA0.DOUT.1.PP (PROLOG.DATA.OUT.1)
```

```
094     BA1.DOUT.2.PP
095     BA2.DOUT.3.PP
096     BA3.DOUT.4.PP
097     BA4.DOUT.5.PP
098     BA5.DOUT.6.PP
099     BA6.DOUT.7.PP
100     .
101     BA7.DOUT.8.PP
102     BB5.PP.RX (PROLOG.MODE RXR.EXTERNAL.INHIBIT)
103     BB6.PP.RX (PROLOG.INTERLOCK RXR.DRIVE.RIGHT)
104     BA0.DIN.1.PP.RX (PROLOG.DATA.IN.1  RXB.DATA.IN.1
105     BA1.DIN.2.PP.RX
106     BA2.DIN.3.PP.RX
107     .
108     .
109     INT-
110     BA3.DIN.4.PP.RX
111     BA4.DIN.5.PP.RX
112     IEO.2 (CARD IEO)
113     BA5.DIN.6.PP.RX
114     BA6.DIN.7.PP.RX
115     BA7.DIN.8.PP.RX
116     BB2.PP (PROLOG.RESPONSE)
117     BB0.PP.RX (PROLOG.ADDRESS RXR.DATA.READY)
118     BB1.PP.RX (PROLOG.ERROR RXR.RDR.RDY)
119     BAR.PP.RX (PROLOG.TRANSFER RXR.OUTPUT.MODE)
120     (GND.9.120)
121     (GND.9.121)
122     (GND.9.122)
```

PINOUT FOR "REMEX.PIN" BOARD - 09-0112-01

J08

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.

```
044     .
045     RD-
046     .
047     D4
048     D5
049     .
050     .
051     D6
052     D7
053     .
054     D0
055     D1
056     D3
057     D2
058     BB7.RX (RXR.DRIVE.LEFT)
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     (GND.9.062)
063     (GND.9.063)
064     (GND.9.064)
065     AB0.D1.LP.RX  (LP.DATA.1  RXP.DATA.1)
066     AB1.D2.LP.RX
067     AB2.D3.LP.RX
068     AB3.D4.LP.RX
069     AB4.D5.LP.RX
070     AB5.D6.LP.RX
071     AB6.D7.LP.RX
072     AB7.D8.LP.RX
073     AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
074     AA6.RX (RXP.INPUT.MODE.SELECT)
075     AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
076     AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
077     AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
078     AA2.LP.RX (LP.FAULT- RXP.ERROR)
079     (ABR)
080     .
081     AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
082     ABS.LP (LP.ACKNOWLEDGE-)
083     (AAR)
084     (AAS)
085     .
086     .
087     AA7.RX (RXP.OUTPUT.MODE.SELECT)
088     IEO.1 (CARD IEI)
089     .
090     .
091     .
092     .
093     BA0.DOUT.1.PP (PROLOG.DATA.OUT.1)
```

```
094     BA1.DOUT.2.PP
095     BA2.DOUT.3.PP
096     BA3.DOUT.4.PP
097     BA4.DOUT.5.PP
098     BA5.DOUT.6.PP
099     BA6.DOUT.7.PP
100     .
101     BA7.DOUT.8.PP
102     BB5.PP.RX (PROLOG.MODE RXR.EXTERNAL.INHIBIT)
103     BB6.PP.RX (PROLOG.INTERLOCK RXR.DRIVE.RIGHT)
104     BA0.DIN.1.PP.RX (PROLOG.DATA.IN.1  RXB.DATA.IN.1
105     BA1.DIN.2.PP.RX
106     BA2.DIN.3.PP.RX
107     .
108     .
109     INT-
110     BA3.DIN.4.PP.RX
111     BA4.DIN.5.PP.RX
112     IEO.2 (CARD IEO)
113     BA5.DIN.6.PP.RX
114     BA6.DIN.7.PP.RX
115     BA7.DIN.8.PP.RX
116     BB2.PP (PROLOG.RESPONSE)
117     BB0.PP.RX (PROLOG.ADDRESS RXR.DATA.READY)
118     BB1.PP.RX (PROLOG.ERROR RXR.RDR.RDY)
119     BAR.PP.RX (PROLOG.TRANSFER RXR.OUTPUT.MODE)
120     (GND.9.120)
121     (GND.9.121)
122     (GND.9.122)
```

PINOUT FOR "PROM PROGRAMMER" BOARD - 09-0031-02

J09

PIN #	SIGNAL NAME
001	(+05V.PRINTED.DISTRIBUTION)
002	(+05V.PRINTED.DISTRIBUTION)
003	(+05V.PRINTED.DISTRIBUTION)
004	.
005	.
006	.
007	.
008	.
009	A06
010	A07
011	.
012	.
013	.
014	.
015	.
016	A00
017	A01
018	A02
019	A03
020	A04
021	A05
022	.
023	.
024	PHI.(SYSTEM.CLOCK)
025	.
026	.
027	.
028	M1-
029	.
030	IORQ-
031	.
032	.
033	.
034	.
035	.
036	.
037	.
038	.
039	.
040	.
041	.
042	.
043	.

```
044     .
045     RD-
046     .
047     D4
048     D5
049     .
050     .
051     D6
052     D7
053     .
054     D0
055     D1
056     D3
057     D2
058     .
059     (+05V.PRINTED.DISTRIBUTION)
060     (+05V.PRINTED.DISTRIBUTION)
061     (+05V.PRINTED.DISTRIBUTION)
062     (GND.PRINTED.DISTRIBUTION)
063     (GND.PRINTED.DISTRIBUTION)
064     (GND.PRINTED.DISTRIBUTION)
065     .
066     .
067     .
068     .
069     .
070     .
071     .
072     .
073     .
074     .
075     .
076     .
077     .
078     .
079     .
080     .
081     .
082     .
083     .
084     .
085     .
086     .
087     .
088     (IEI)
089     .
090     .
091     .
092     .
093     .
```

```
094      .
095      .
096      .
097      .
098      .
099      .
100      .
101      .
102      .
103      .
104      .
105      .
106      .
107      .
108      .
109      (INT-)
110      .
111      .
112      (IEO)
113      .
114      .
115      .
116      .
117      .
118      .
119      .
120      (GND.PRINTED.DISTRIBUTION)
121      (GND.PRINTED.DISTRIBUTION)
122      (GND.PRINTED.DISTRIBUTION)
```

PINOUT FOR I/O CONNECTOR "FLOPPY.CABLE.PIN"

J13

PIN #	SIGNAL NAME
001	.
002	.
003	.
004	.
005	.
006	.
007	.
008	.
009	.
010	.
011	GND.3.064
012	GND.3.064
013	GND.3.064
014	GND.3.064
015	GND.3.064
016	GND.3.063
017	GND.3.063
018	GND.3.063
019	GND.3.063
020	GND.3.063
021	GND.3.062
022	GND.3.062
023	GND.3.062
024	GND.3.062
025	GND.3.062
026	.
027	.
028	.
029	.
030	.
031	.
032	.
033	.
034	.
035	INDX.0-
036	RDY-
038	SEL.0-
039	SEL.1-
040	.
041	.
042	DIRECTION.F
043	STEP-
044	WR.DATA-

```
045     WRITE.GATE-
046     TRK.00-
047     WR.PROT.0-
048     READ.DATA-
049     .
050     .
```

PINOUT FOR I/O CONNECTOR "TTY.CABLE"

J14

PIN #	SIGNAL NAME
001	.
002	RS232.DATA.IN
003	RS232.DATA.OUT
004	.
005	TTY.IN.RETURN
006	TTY.IN.RETURN
007	RS232.RETURN
008	TTY.IN.RETURN
009	.
010	TTY.DATA.IN
011	.
012	.
013	.
014	.
015	.
016	TTY.DATA.OUT
017	TTY.OUT.RETURN
018	.
019	.
020	.
021	.
022	.
023	.
024	TTY.IN.RETURN
025	.

PINOUT FOR I/O CONNECTOR "ZDSP.CABLE.PIN"

J15

PIN #	SIGNAL NAME
001	.
002	TTXD
003	TRXD
004	TRTS
005	TCTS
006	TDSR
007	GND.2.120
008	CARRIER.DETECT
009	ORIGINATE.MODE
010	LOCAL.MODE
011	.
012	.
013	.
014	.
015	.
016	.
017	.
018	.
019	.
020	TDTR
021	.
022	RING.IND
023	.
024	SYNC
025	TERM.BUSY

PINOUT FOR "M.ICE.CABLE.2.PIN"

J16

PIN #	SIGNAL NAME
001	UMEM-
002	.
003	UBUSAK-
004	URFSH-
005	UNMI-
006	UWAIT-
007	URST-
008	.
009	UWR-
010	URD-
011	UMRQ-
012	UIORQ-
013	UPHI
014	UBREQ-
015	UIE
016	UHALT-
017	UM1-
018	UINT-
019	GND.2.062
020	GND.1.064
021	GND.1.064
022	GND.1.063
023	GND.1.063
024	GND.1.062
025	GND.1.062

PINOUT FOR "M.ICE.CABLE.1.PIN"

J17

PIN #	SIGNAL NAME
001	UA00
002	UA02
003	UA04
004	UA06
005	UA08
006	UA10
007	UA12
008	UA14
009	UDB0
010	UDB2
011	UDB4
012	UDB6
013	UDB7
014	UA01
015	UA03
016	UA05
017	UA07
018	UA09
019	UA11
020	UA13
021	UA15
022	UDB1
023	UDB3
024	UDB5
025	GND.1.062

PINOUT FOR I/O CONNECTOR "ZDSP.2.CABLE.PIN"

J18

PIN #	SIGNAL NAME
001	.
002	TTXD.2
003	TRXD.2
004	TRTS.2
005	TCTS.2
006	TDSR.2
007	GND.2.120
008	CARRIER.DETECT.2
009	ORIGINATE.MODE.2
010	LOCAL.MODE.2
011	.
012	.
013	.
014	.
015	.
016	.
017	.
018	.
019	.
020	TDTR.2
021	.
022	RING.IND.2
023	.
024	SYNC.2
025	TERM.BUSY.2

PINOUT FOR I/O CONNECTOR "PROLOG.CABLE.PIN"

J19

PIN #	SIGNAL NAME
001	.
002	BAR.PP.RX (PROLOG.TRANSFER RXR.OUTPUT.MODE)
003	BB5.PP.RX (PROLOG.MODE RXR.EXTERNAL.INHIBIT)
004	.
005	BB6.PP.RX (PROLOG.INTERLOCK RXR.DRIVE.RIGHT)
006	BA6.DOUT.7.PP
007	BA2.DOUT.3.PP
008	BA7.DOUT.8.PP
009	BA3.DOUT.4.PP
010	BA4.DOUT.5.PP
011	BA0.DOUT.1.PP (PROLOG.DATA.OUT.1)
012	BA1.DOUT.2.PP
013	BA5.DOUT.6.PP
014	BB1.PP.RX (PROLOG.ERROR RXR.ERROR)
015	BB0.PP.RX (PROLOG.ADDRESS RXR.DATA.READY)
016	BB2.PP (PROLOG.RESPONSE)
017	BA2.DIN.3.PP.RX
018	BA3.DIN.4.PP.RX
019	BA0.DIN.1.PP.RX (PROLOG.DATA.IN.1 RXB.DATA.I
020	BA1.DIN.2.PP.RX
021	BA6.DIN.7.PP.RX
022	BA7.DIN.8.PP.RX
023	BA4.DIN.5.PP.RX
024	BA5.DIN.6.PP.RX
025	GND.2.121

PINOUT FOR I/O CONNECTOR "LP.CABLE"

J20

PIN #	SIGNAL NAME
001	AB0.D1.LP.RX (LP.DATA.1 RXP.DATA.1)
002	AB1.D2.LP.RX
003	AB2.D3.LP.RX
004	AB3.D4.LP.RX
005	AB4.D5.LP.RX
006	AB5.D6.LP.RX
007	AB6.D7.LP.RX
008	AB7.D8.LP.RX
009	AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
010	AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
011	ABS.LP (LP.ACKNOWLEDGE-)
012	AA2.LP.RX (LP.FAULT- RXP.ERROR)
013	AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
014	.
015	.
016	.
017	.
018	GND.2.122
019	GND.2.122
020	GND.2.121
021	.
022	.
023	AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
024	AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
025	.

PINOUT FOR I/O CONNECTOR "FRONT.PANEL.CABLE"

J21

PIN #	SIGNAL NAME
001	GND.1.122
002	GND.1.122
003	BREAK.SYNC
004	SENSE.SW.1+
005	.
006	GND.1.121
007	+05V.1.061
008	+05V.1.061
009	+05V.1.060
010	+05V.1.060
011	USER.NO
012	USER.NC
013	GND.1.121
014	SENSE.SW.2-
015	SENSE.SW.1-
016	SENSE.SW.2+
017	.
018	BNMI.SW-
019	RESET.SW-
020	HALT.LAMP-
021	USER.LAMP-
022	MONITOR.LAMP-
023	WAIT.LAMP-
024	GND.1.120
025	MONTR.NO
026	MONTR.NC

PINOUT FOR I/O CONNECTOR "POWER CABLE"

J25

PIN #	SIGNAL NAME
001	-05V.1
002	-05V.2
003	-5V.12
004	(-12V.1)
005	(-12V.2)
006	(-12V.3)
007	+12V.1
008	+12V.2
009	+12V.3
010	(+05V.PRINTED.DISTRIBUTION)
011	(GND.PRINTED.DISTRIBUTION)

PINOUT FOR I/O CONNECTOR "REMEX.CABLE"

J26

PIN #	SIGNAL NAME
001	AB0.D1.LP.RX (LP.DATA.1 RXP.DATA.1)
002	AB1.D2.LP.RX
003	AB2.D3.LP.RX
004	AB3.D4.LP.RX
005	AB4.D5.LP.RX
006	AB5.D6.LP.RX
007	AB6.D7.LP.RX
008	AB7.D8.LP.RX
009	.
010	AA1.LP.RX (LP.INPUT.PRIME- RXP.DIRECTION)
011	AA0.LP.RX (LP.DATA.STROBE- RXP.PUNCH.COMMAND)
012	AA4.LP.RX (LP.BUSY RXP.PUNCH.READY)
013	AA5.LP.RX (LP.SELECT RXP.PUNCH.SYSTEM.READY)
014	BB1.PP.RX (PROLOG.ERROR RXR.RDR.RDY)
015	BB5.PP.RX (PROLOG.MODE RXR.EXTERNAL.INHIBIT)
016	BB6.PP.RX (PROLOG.INTERLOCK RXR.DRIVE.RIGHT)
017	BB7.RX (RXR.DRIVE.LEFT)
018	.
019	.
020	.
021	.
022	.
023	.
024	GND.4.062
025	GND.4.062
026	AA6.RX (RXP.INPUT.MODE.SELECT)
027	AA7.RX (RXP.OUTPUT.MODE.SELECT)
028	GND.4.063
029	GND.4.063
030	GND.4.064
031	.
032	AA2.LP.RX (LP.FAULT- RXP.ERROR)
033	AA3.LP.RX (LP.PAPER.EMPTY RXP.TAPE.LOW)
034	.
035	.
036	.
037	GND.4.064
038	BA0.DIN.1.PP.RX (PROLOG.DATA.IN.1 RXB.DATA.IN.1
039	BA1.DIN.2.PP.RX
040	BA2.DIN.3.PP.RX
041	BA3.DIN.4.PP.RX
042	BA4.DIN.5.PP.RX
043	BA5.DIN.6.PP.RX

```
044     BA6.DIN.7.PP.RX
045     BA7.DIN.8.PP.RX
046     BB0.PP.RX (PROLOG.ADDRESS RXR.DATA.READY)
047     BAR.PP.RX (PROLOG TRANSFER RXR.OUTPUT.MODE)
048     GND.5.064
049     GND.5.063
050     GND.5.062
```

Zilog

10340 Bubb Road
Cupertino, California 95014
Telephone: (408) 446-4666
TWX. 910-338-7621